Handout 17

by Dr Sheikh Sharif Iqbal

Memory Unit and Read Only Memories

Objective:

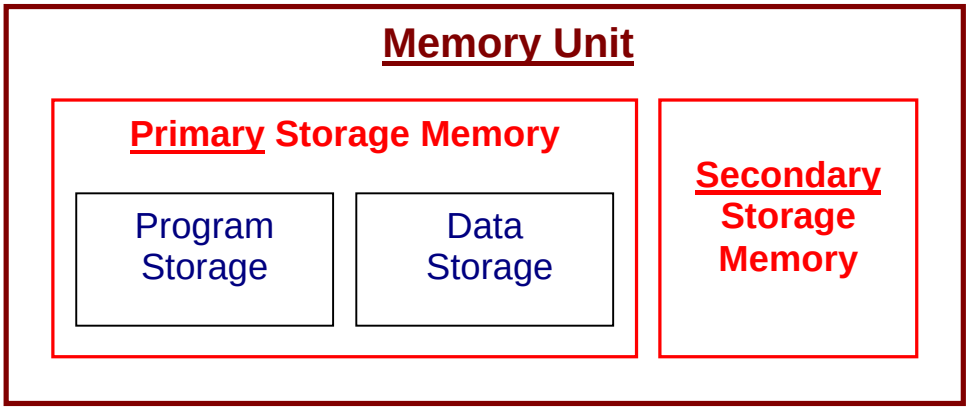
- To discuss different types of memories used in 80x86 systems for storing digital information.

- To learn the electronic circuits associated with different types of Read Only Memories (ROM's)

Slide 1: **Memory Unit of 80x86 based systems:**

- Memory units of a computer system provide the ability to store and retrieve digital information.

- Typically the memory unit is partitioned into a primary storage and secondary storage sections, as shown if figure below:



Slide 2: **Secondary Memory storage:**

- Secondary storage is used for storing information that is not in active use by the microprocessor.

- This class of external storage is usually slower than the primary or internal storage, but also almost always has higher storage capacity.

- The non–volatile secondary memories are mostly made of magnetic (Floppy, Hard-disk, Magnetic tapes), optical (CD, DVD) and electrical (Flash) devices.

- Large secondary storages are formatted according to file system (FAT, NTFS), to ease the access of stored information.

Slide 3: **Primary Memory storage:**

- Primary storage is used to store information that is likely to be in active use by the processor (CPU).

- These semiconductor memories consists of high speed but relatively smaller internal devices, such as ROM and RAM..

Note: ***The storage mechanism and electronics related to ROM and RAM will be discussed in later slides.***

- Primary memory is further subdivided into Program storage and Data storages. Program storage consists of non-volatile (***BIOS***) and volatile (programs that are executed) memories, whereas Data storage consist of volatile (processed by CPU) memories

BIOS *is Basic Input Output System**.** The primary function of the BIOS is to prepare the machine so that programs stored on various media (such as hard drives, floppies, and CDs) can load, execute, and assume control of the PC. This process is known as booting up.*

Slide 4: **Types of Basic Primary Memories:**

- ROM (Read Only Memory)
  - ROM is non-volatile or does not lose its contents when power is turned off.

- PROM (Programmable or one-time programmable Memory)
  - Information to be programmed by permanently blowing the internal fuses of the device.
  - Special equipment is needed to program the ROM

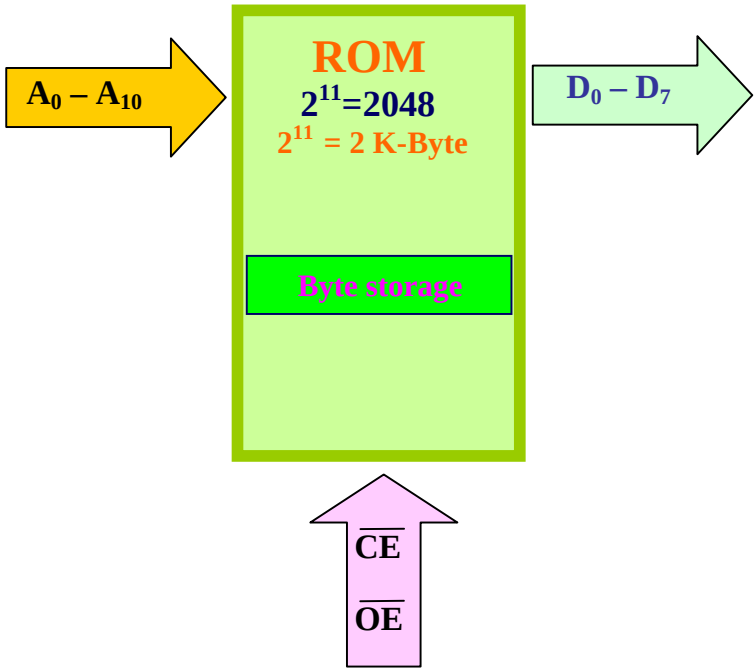
- EPROM (Erasable Programmable ROM)
  - Allowed reprogramming is limited by 2000 times.
  - As ultraviolet (UV) radiation is used to bulk erase the contents. So this classes of ROM is called UV-EPROM

- EEPROM (Electrically Erasable ROM)
  - Method of erasure is electrical and re-programming is limited by 500000 times. Thus, more expensive.
  - Allows the erasure of individual data bytes

Slide 5: **Primary storage: Read Only Memory (ROM):**

- ROM is a non-volatile memory and used to store firmware (embedded software's required for hardware operation: BIOS)

- The block diagram of a 2 K-Byte ROM is shown below. Its memory interface circuits are presented in previous lectures.



- Note that the Data Bus (blink $D_0 - D_7$ and Byte storage) determines the width of the stored data in each memory location. Here each location stores an 8-bit or Byte wide data and can be outputted using $D_0 - D_7$.

- The width of the Address Bus (blink $A_0 - A_{10}$) determines the capacity of the storage. Here 11-bit address bus can access 2^{11}=2048 Byte-wide memory locations.

- The control bus (blink CE and OE) is mainly used to control the reading process by enabling the ROM chip and its output circuitry.

Slide 6: **Electronics related to MASK programmable ROMs:**

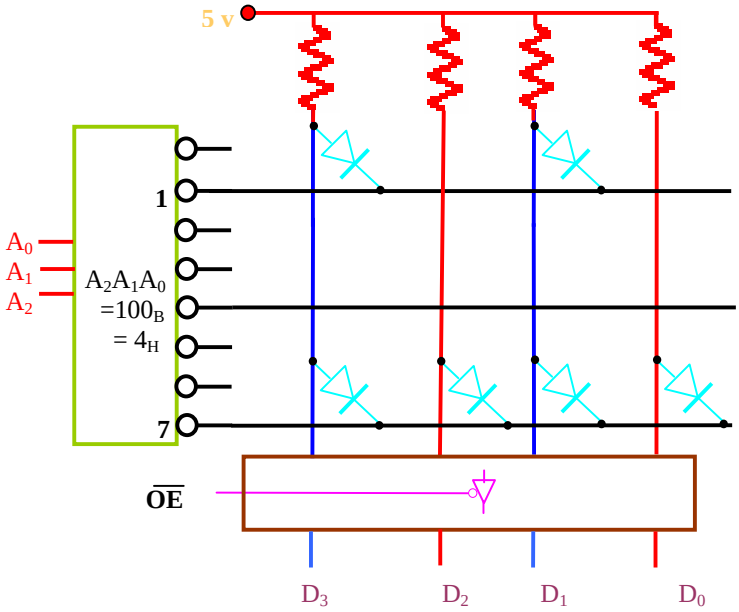
- Used by industry for mass production of ROM

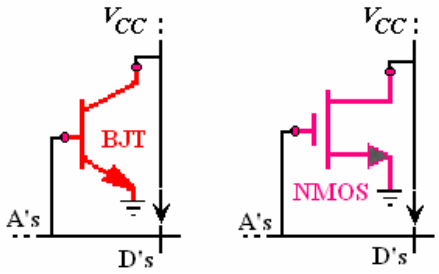
- Factory programmed according to truth-table

- Contains an address decoder, a program-able logic array and a set of output switches. ***Note 1***

- To improve noise-margin, speed, compactness and fabrication process, diodes are later replaced BJT and MOS ***Note 2***

- (MOS)t_{acc}≈10*(BJT)t_{acc} ***Note 3***





Note 1:

- Note when the decoder activates a line, say line 1, it outputs logic 0 and turns the diodes on. Consequently, logic 0 is outputted via diode connected output lines. Thus, for $A_2A_1A_0$=001, the decoder selects line 1 and the related output is: **D_0='logic 1' , D_1='logic** 0' , **D_2='logic 1' and D_3='logic** 0' . But remember this output is only send out if the output-switch is activated by proper "OE bar" input. *(blink the logic levels in the figure)*

Note 2:

- The required connections for BJT and MOS devices are: *(Make the BJT and FET figure appear in screen*

Note 3:

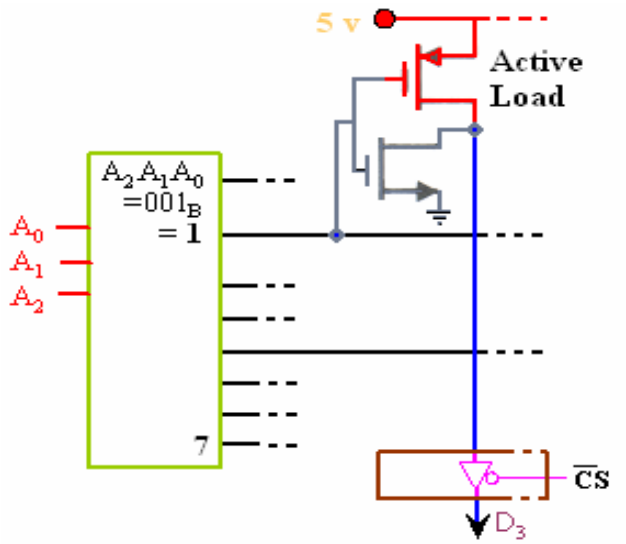
- Note that the access times (t_{acc}) of MOS devices are much slower compared to that of BJT devices.

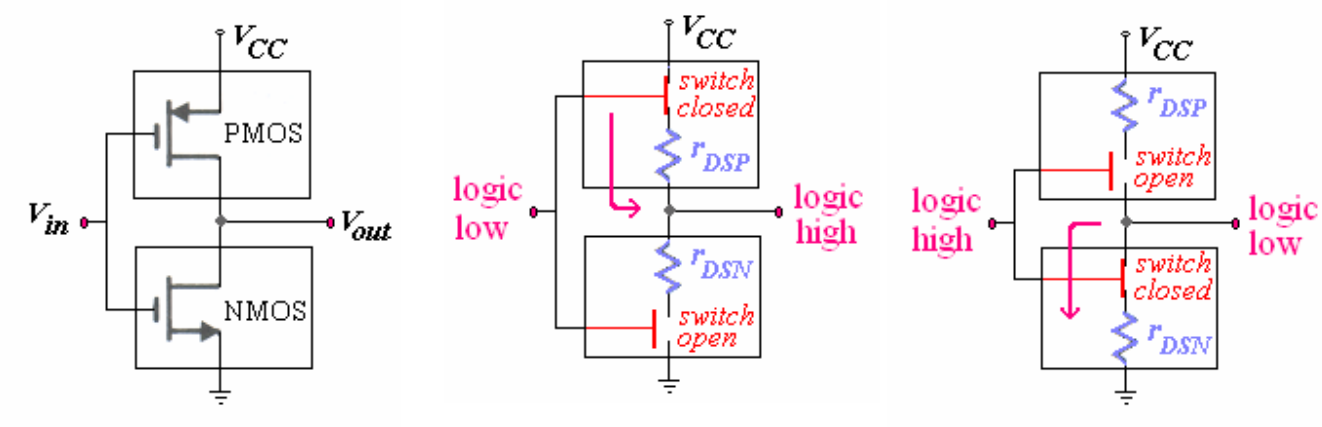
Slide 7: **CMOS based MASK programmable ROM's:**

- To further reduce power requirements and size, CMOS switches are applied, as shown.

- Note that PMOS and NMOS behave like an active load and a switch, respectively.

- Want to see the working of CMOS switches? CLICK HERE





- Note that for logic low or 0 input, the NMOS behaves like a open switch and the PMOS acts as a active load, which pulls the output up to logic high level.

- Whereas for logic high input the PMOS behaves like a open switch and the NMOS pulls the output down to logic low level.

Slide 8: **<u>One time programmable ROM (OT-PROM):</u>**

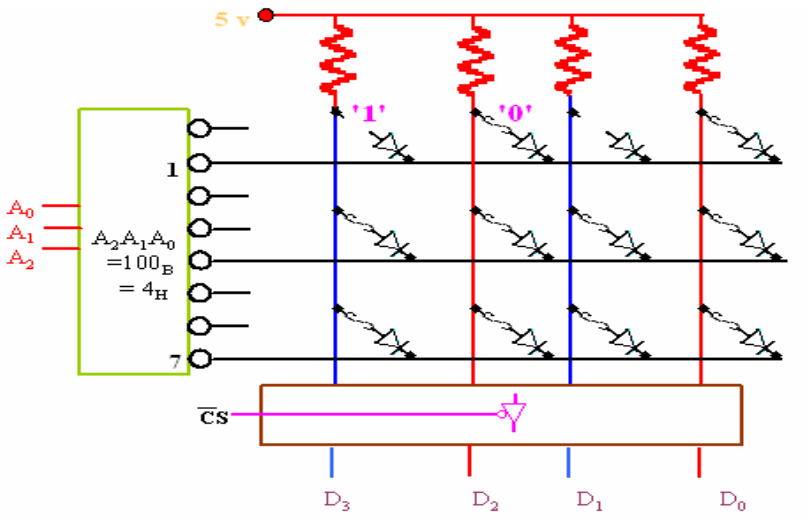
- In PROM, the manufacturer attach a series low current fusible link with each diode of the OTP memory array.

- During programming, current pulses are used to burn the desired fuse (nichrome) to store '**1**'. Paths with unburned fuse stores 'logic 0'

- <u>Remember:</u>

Initially all the storage locations are programmed to store ‘logic 0’, as the fuses remains intact.

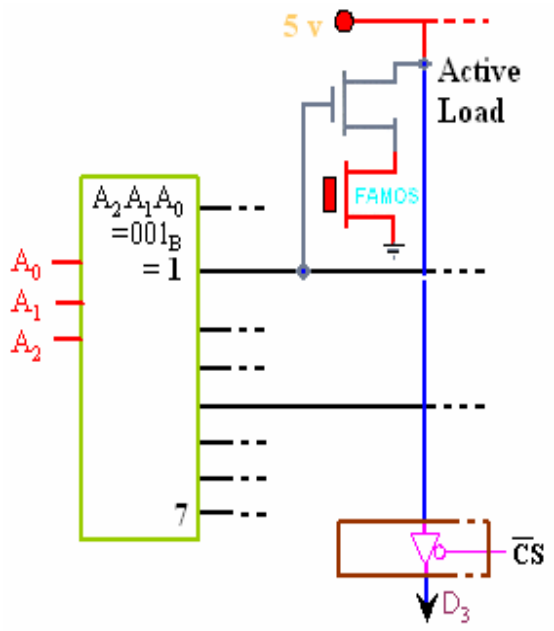
Once burned, the junctions are thought of storing ‘logic 1’



Slide 9: **Erasable Programmable ROM (UV-EPROM):**

- A floating-gate-avalanche-MOS (FAMOS) with insulated floating gate is used in class of EPROM.

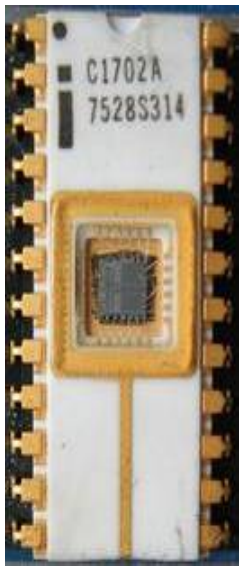
- To program, a large voltage pulse is applied to the drain of the MOS, which allows the insulated gate to store charges. These stored charges causes the FAMOS to remain on and allow current to flow via both MOS's.



- Thus, if the address decoder activates the MOS with pre-stored charges, the data line become GNDed and 'logic 0' is outputted.

Slide 10: **Erasable Programmable ROM (Cont'd):**

- Due to FAMOS gate insulation, stored charges are removed by illuminating the gate with UV radiation via **quartz** window. The injected photons deliver enough energy to the trapped electrons to reverse the programming process.



- Some Disadvantages of UV_EPROM:
  - Has to be removed from the circuit-board to be erased
  - Quartz-window package is expensive
  - Bulk erase is not possible.

- EPROM chips and programmers can be found in following URL's:

  http://www.arlabs.com/page1.htm

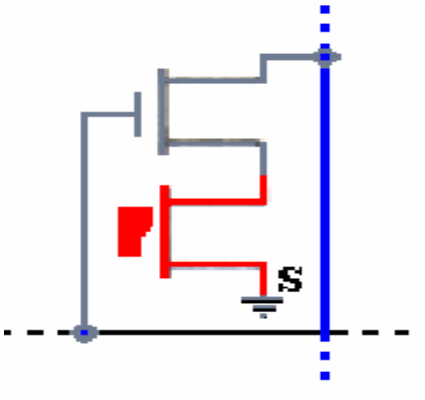
  http://www.futurlec.com/ICEPROM.shtml

Slide 11: **Electrically Erasable Programmable ROM (EE-PROM):**

- EE-PROM chips are used in computers, microcontrollers and other devices to store configuration data, where their operation depents on the electrical interfaces to EEPROM (serial bus or parallel bus).

- Parallel EEPROM is simple and fast compared to serial EEPROM, but due to its large size it is becoming more and more unpopular.

- EEPROM also uses FAMOS, where the gate oxide is made very thin over the drain. Consequently, tunneling phenomena is used to trap charges in the insulated gate (*required to store 'logic 0'*), as shown in figure.



- To discharges the insulated gate, a positive voltage is applied in the drain.

Slide 12: **Electrically Erasable Programmable ROM (Cont'd):**

- Microcontrollers use integrated EE-PROM storage devices.

- With repeated use the read/write cycle causes some charges to be permanently trapped in gate and restricts the lifetime of EEPROM

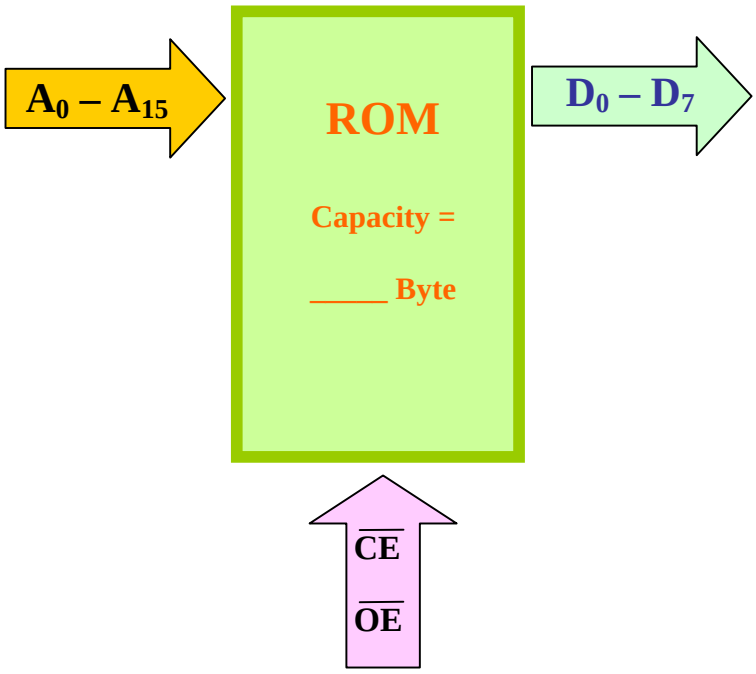
- Advantages over EPROM: (1) Unlike UV-EPROM; Expensive quartz-window package is not required and do not have to be removed from the circuit-board to erase stored data. (2) Read cycle looses very small charges

Useful URL's for EEPROM chip's and programmer:

http://www.futurlec.com/ICEEPROM.shtml
http://www.eetools.com/index.cfm?fuseaction=product.display&Product_ID=9

Slide 13: **Example 1:**

QUESTION: For the given ROM, find the total storage capacity.



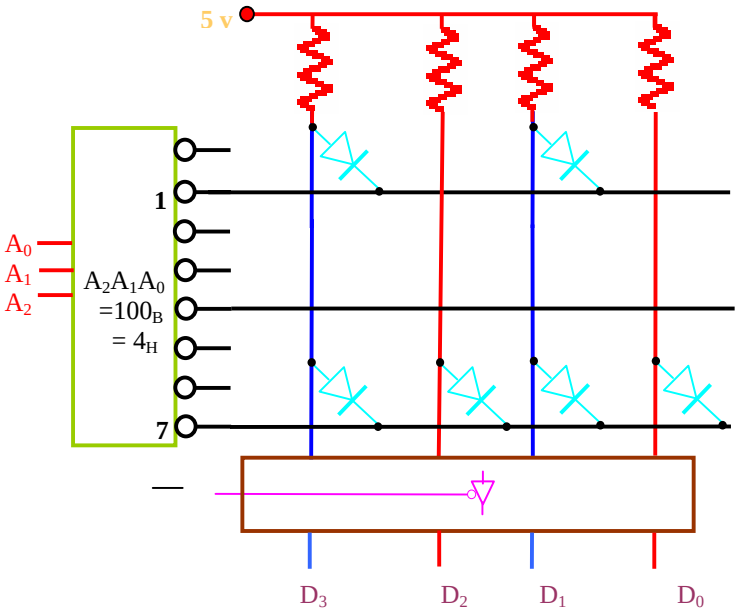
SOLUTION: It is clear that from the data lines that each memory location stores 8-bits or 1-byte of data. So the number of bytes should be equal to the number of memory location. Thus,

Number of memory location = 2^{15} = 32768 = 32 K
Total Storage capacity in bytes = 32 k-Bytes
Total storage capacity in Bits = 32768 X 8 = 262144 Bits

Slide 14: **Example 2:**

QUESTION: What is the function of $\overline{OE}$ and $\overline{CE}$ control pins?

SOLUTION: Every ROM circuit, as shown in figure, has an output control circuit that is enabled by output-enable ($\overline{OE}$) pin. Since total read only memory contains multiple ROM IC's, chip enable ($\overline{CE}$) pin enables and disables these IC's as needed.



QUESTION: Summarize the read-cycle of a EPROM.
SOLUTION: (1) Apply the appropriate control signals
(2) Apply the valid physical address to EPROM
(3) The EPROM requires some time, called access time (t_{acc}), to decode, locate and access the desired storage location
(4) Data will be outputted via data-bus

QUESTION: Which programmable ROM is erased using ultraviolet?
SOLUTION: UV-EPROM