Handout 4 for EE-203

Digital Logic Circuits

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**(Ref: Text book and
KFUPM Online course of EE-203)**

(Remember to solve all the related examples, exercises problems as given in the Syllabus)

5.3.4 & 5.10: Bipolar Junction Transistor (BJT) Switches:

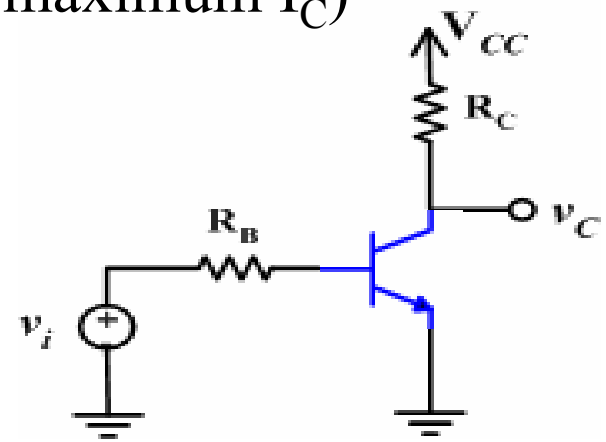
Reference: *"Microelectronic Circuits by Sedra/Smith* and *EE-203 Online course, KFUPM*

- In chapter 5, BJT operating in active mode is used to design Amplifier. Now we will concentrate on the other two modes. At one extreme BJT operates in cutoff region (BJT ➔ OFF or $I_C \approx 0$) and at other extreme BJT operates in saturation region (BJT ➔ ON, maximum I_C)

- If $v_i < 0.5$ volt, the EBJ is reverse biased (R.B). Since CBJ is also reverse biased (*as V_{cc} is '+'*)

  ➔ BJT is OFF or operating in cutoff mode

  Thus, $I_B=0$, $I_C=0$, $I_E=0$, $V_C=V_{CC}$



- If $v_i \geq 0.7$ volt, the EBJ is forward biased. If CBJ is still reverse biased (if $V_C > 0.7$) ➔ BJT is ON but in Active region (*can't be used as a switch*)

- With ↑ v_i ; I_B ↑ resulting an ↑ V_B and ↑ I_C. Thus, V_C will ↓ and when $V_C < V_B$ by 0.5v, CBJ will be F.B. As EBJ is still F.B➔ BJT is Saturated

Thus, $V_{BE}= 0.7$, $V_{BC}= 0.5$, $V_{CEsat}= 0.2$, $I_{Csat}= (V_{CC} - V_{CESat}) / R_C$ *and* $I_B= I_C / \beta_{Sat}$

BJT Switches (cont'd.):

- If due to some reason (i.e. temperature change), the base current is reduced than the transistor will enter the active mode from the edge of saturation. So the base current is designed to be higher than the edge of saturation value, by a factor of 2 to 10. This is called overdrive factor.

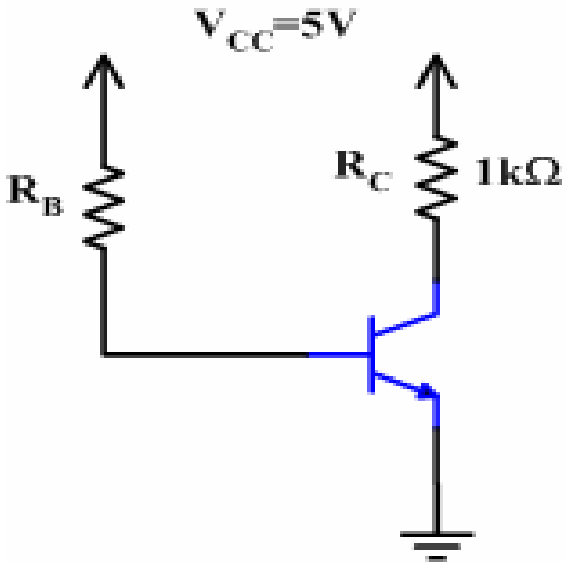
- Example: For the circuit shown, select a value for R_B so that transistor saturates with an overdrive factor of 10. The BJT have a minimum β=30 and V_{CEsat}=0.2V. What is the resulted value of forced β?

- Solution:

$I_C = (5 - 0.2) / 1\text{ k} = 4.8\text{ mA}$; $I_B = I_C / \beta = 0.16\text{ mA}$;

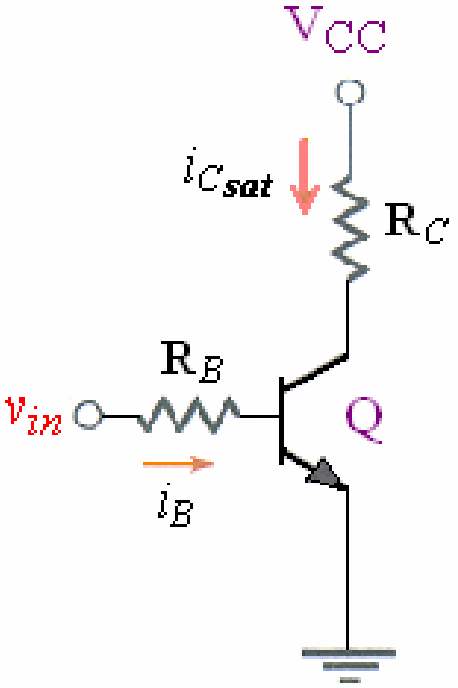
So, $10\, I_B = (V_{CC} - V_{BE}) / R_B$; $R_B = 2.7\text{ k}$

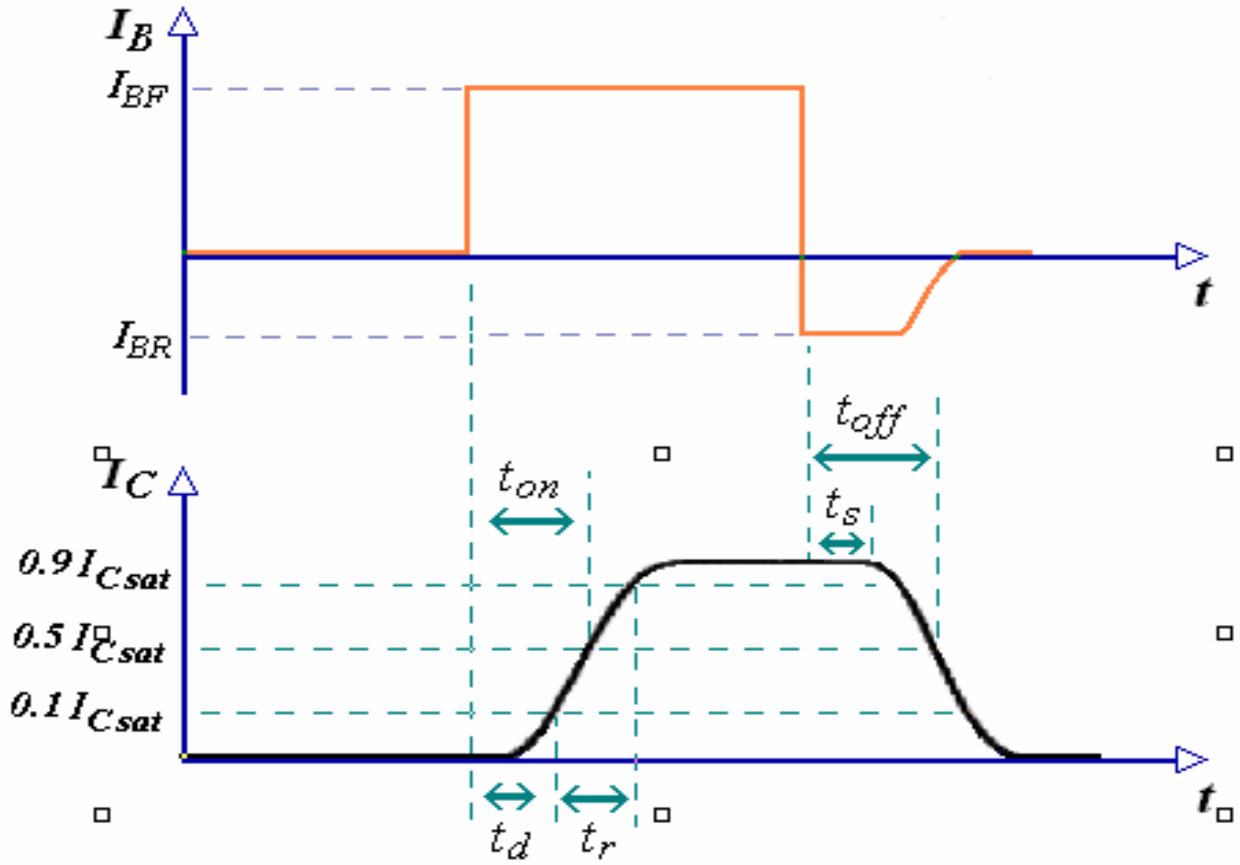
and $\beta_F = I_C / I_{BF} = 3$



BJT Switches Parameters:

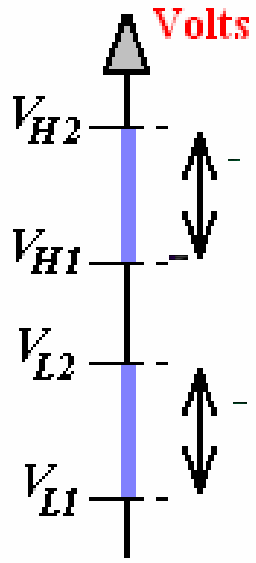
- Internal capacitance of BJT introduces a time delay between the application of i_B and the flow of i_C. The measure of BJT's switching speed depends on its delay-time (t_d ,n-sec), rise-time (t_r ,*n-sec*), turn-on-time (t_{on}), storage-time (t_s) *and* turn-off-time (t_{off}). Often larger **ts** constitute the limiting factor on S/W





Chapter 10 ➔ 10.1 Digital Logic Circuits:

- In this slide, logic level specification of digital circuits are presented.
- Analog systems uses continuous property of electrical signals, whereas in digital systems, electrical signals represent numbers. Typically in binary digital circuits, it is customary to choose two predetermined DC voltage levels to represent logic high ‘1’ or low ‘0’.



- However, in order to allow for the inevitable component tolerances and other effects that change the signal voltage levels, two distinct voltage ranges are usually used instead of two voltage values
- Thus, in digital circuits, if the signal voltage lies in the range V_{L1} to V_{L2}, the signal is interpreted as logic low or '0'. But if signal voltage lies in the range V_{H1} to V_{H2}, the signal is interpreted as logic high or '1'. Note, the undefined region voltages are never used.

10.1: Characteristics of Digital Logic circuits:

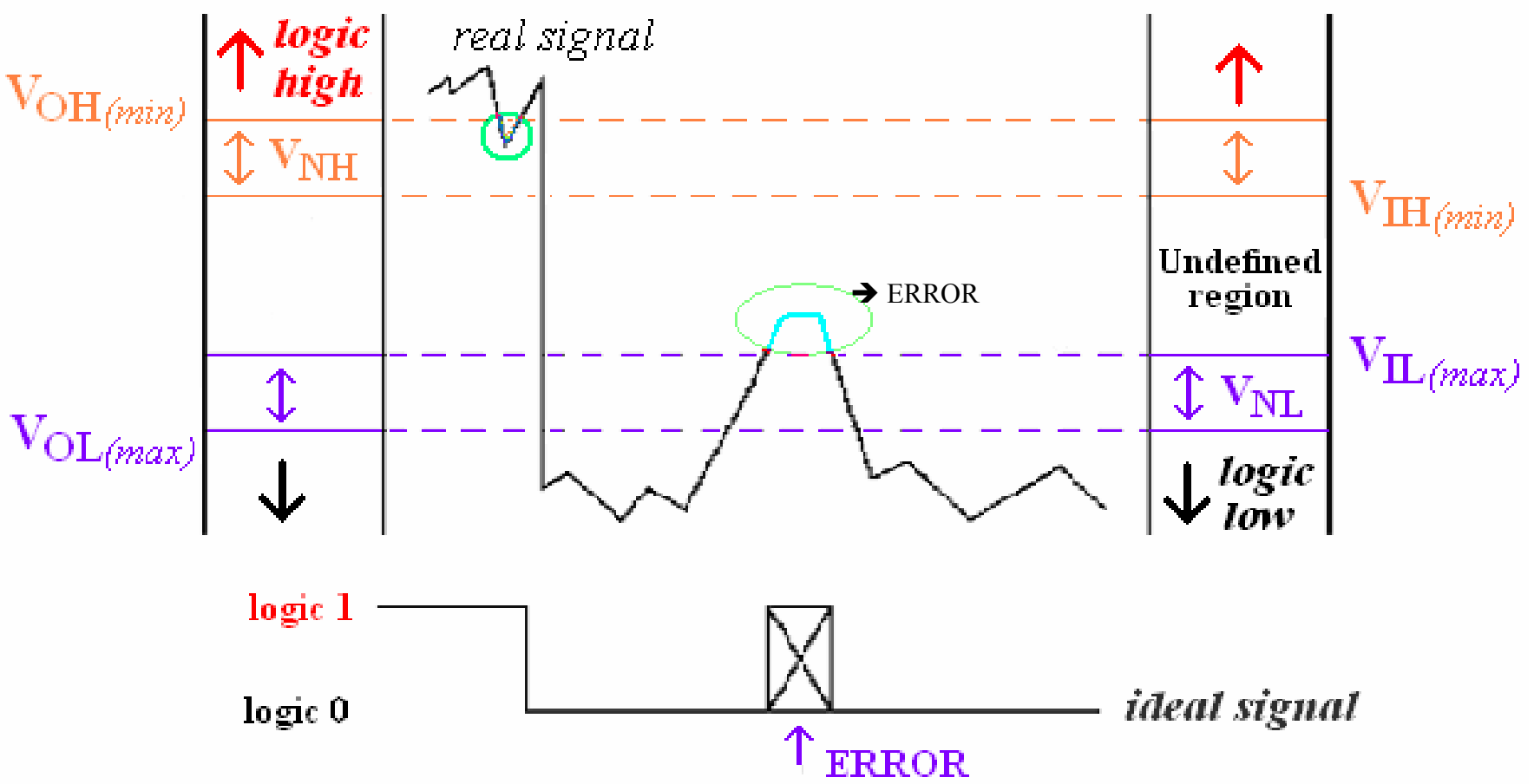
Characteristics that are essential to successfully design digital circuits are;

(a) **Allowable range** of input and output voltage/current at gates

- If '**H**' represents high or 'logic 1' state and '**L**' represents low or 'logic 0'
  - V_{IH} is the minimum voltage level at the input to be recognized as **H**.
  - V_{IL} is the maximum voltage level at the input to be recognized as **L**.
  - V_{OH} is the minimum voltage at the output when in state **H**.
  - V_{OL} is the maximum voltage at the output when in state **L**.
  - I_{IH} is the current flowing into input when a high voltage is applied.
  - I_{IL} is the current flowing into input when a low voltage is applied.
  - I_{OH} is the current flowing out of the output when in state **H** or high.
  - I_{OL} is the current flowing out of the output when in state **L** or low.
- Error free or unambiguous communication of logic level, from one gate to another, in a digital system require: $V_{OH} >= V_{IH}$ and $V_{OL} <= V_{IL}$

10.1: Characteristics of Digital Logic circuits: *Cont'd…*

(b) **Noise Margin** (≈ *expressed in volt*): Noise margin is a measure of the extent to which a logic circuit can tolerate noise or unwanted signals.



$$V_{NH} = V_{OH(min)} - V_{IH(min)} \quad \text{and} \quad V_{NL} = V_{IL(max)} - V_{OL(max)}$$

10.1: Characteristics of Digital Logic circuits: (*Loading rule*)

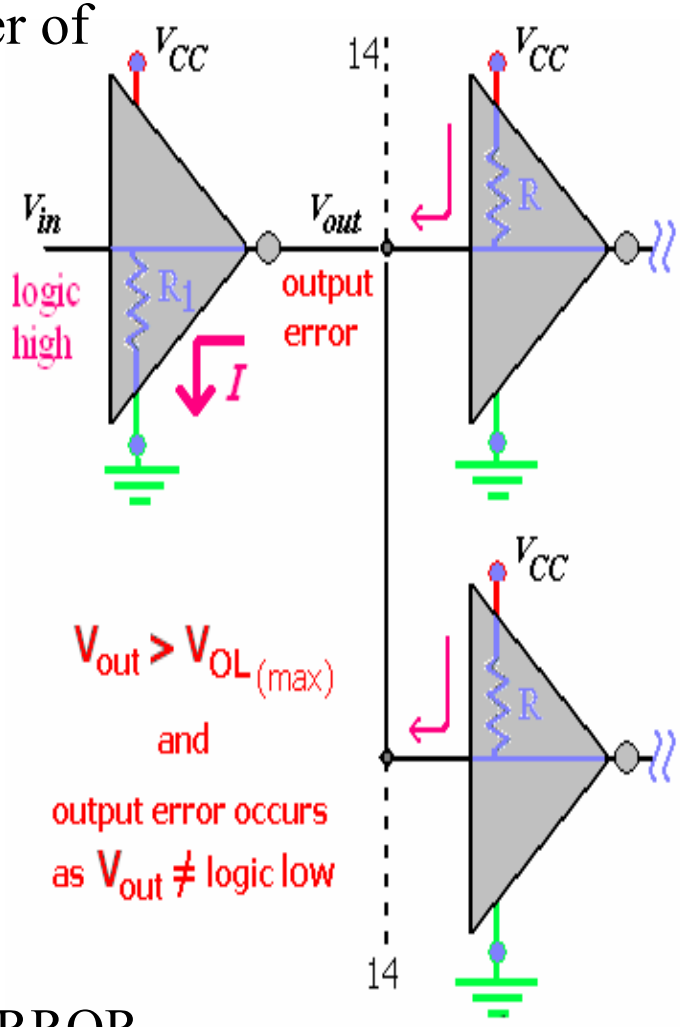
(c) - **Fan-in** of a logic gate is the number of its inputs driving the gate.

- **Fan-out**: The output of a logic gate often has to drive a number of other gate inputs. However, a gate can only supply a limited amount of current. Thus, ***fan-out*** of a gate is the maximum number of gates, allowed to be connected at the output of that gate, and are reliably driven by that gate.

- For logic high input, output of TTL inverter will be logic low. Thus, it will sink current from the load gates. Fan-out of this gate, specifies the max. no. of load gates that are successfully driven by the inverter output.

- If the inverter is sinking current from only one gate, the internal voltage drop in 'I_{R1}' is low and $v_{out}=V_{R1}=$ 'logic low' $< V_{OL(max)}$

- But if the given inverter is driving 30 gates, 'V_{R1}' is high and $v_{out} > V_{OL(max)}$ *or* $\neq$ 'logic 0' ➔ ERROR

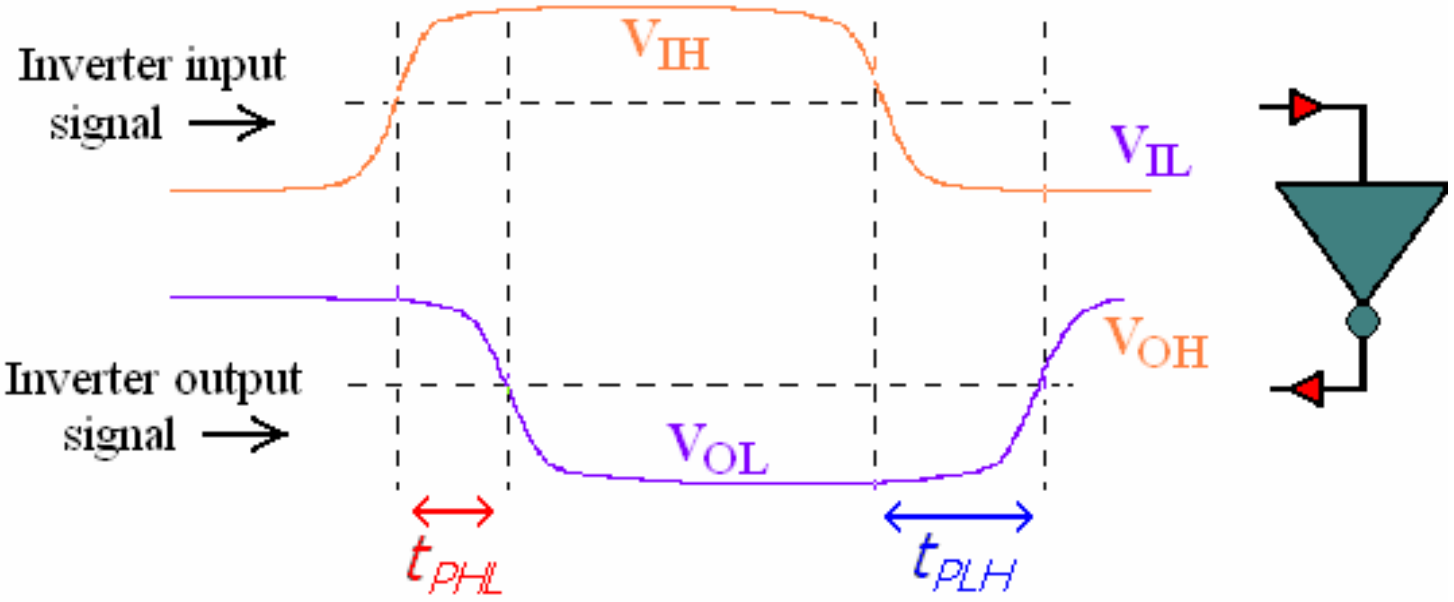


10.1: Characteristics of Digital Logic circuits: *Cont'd....*

(d) **Propagation delay** (≈ *expressed in nano-seconds*): t_P is a measure of time taken to change the output state after an input is applied. Thus,

t_{PHL} ➔ time taken to change from '1' to '0' & t_{PLH} ➔ time to change from '0' to '1'

Then, average propagation delay of a transistor inverter circuit, expressed in terms of t_{PHL} and t_{PLH} are given by;



Thus, switching speed of a logic circuit is limited by propagation delay.

10.1: Characteristics of Digital Logic circuits: *Cont'd....*

(e) **Power Dissipation** (≈*milliwatts*): is the supplied power required to operate the gate and is an important factor in designing portable digital products.

- When the output of a logic gate is in logic high state or 'logic 1', it draws a current of 'I_{CCH}'.
- But if the output is in logic low state, it draws a current of 'I_{CCL}'
- If gate is connected with a power supply of 'V_{CC}' volt, then the average current drawn by the gate is:

$$I_{CC(ave)} = \frac{I_{CCH} + I_{CCL}}{2}$$

and average ***power-dissipated*** in a gate is:

$$P_{D(ave)} = I_{CC(ave)} \times V_{CC}$$

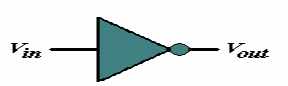
- Power dissipation also occurs in the gate during switching operation

(f) **Delay power product** (*should be as small as possible*): is a figure of merit that describe the gates power requirement and the related switching speed.

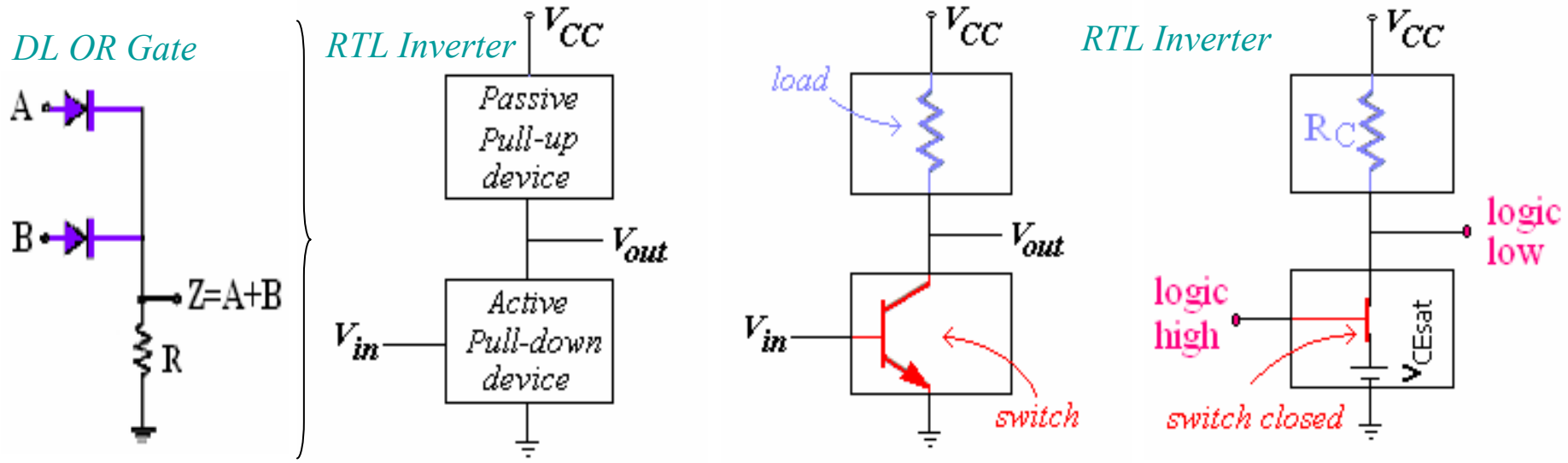
High speed switches often require more power.

Thus, ***delay-power-product*** is given by: $t_{p(ave)} \times P_{D(ave)}$

Evolution of Logic Gates → DL gate → RTL Inverters:



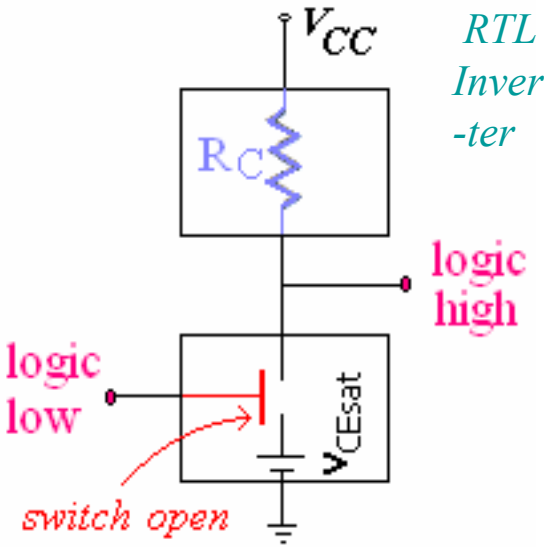
- Primary building block used in digital circuits are inverters
- Simplest of logic inverter uses a voltage-controlled switch (figure below)
- In early days, the switch was made using only transistors and resistors, constituents of the resistor transistor logic (RTL) family.



- If logic high input is applied to this transistor switch, the transistor becomes saturated and the switch will be on. Consequently, the circuit will sink current from any output device and the collector emitter saturation voltage (V_{CEsat}), will appear in the output => logic low state

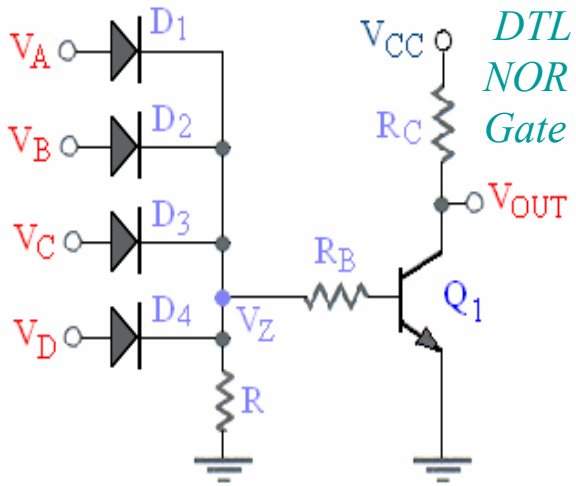
Improvement of Logic inverters; RTL → DTL → TTL .

- If logic low input is applied to this transistor, the transistor will cut off and the switch will be open. Consequently, the circuit will source current for any output device, and due to small voltage drop in the collector resistor, the output will be at logic high. If no load is connected with the output, as shown in the figure, V_{cc} will appear in the output port => logic high or '1'



RTL Inver -ter

- RTL switches were later improved by adding diodes in the input stage called diode transistor logic (DTL) circuits. Figure shows DTL NOR gate



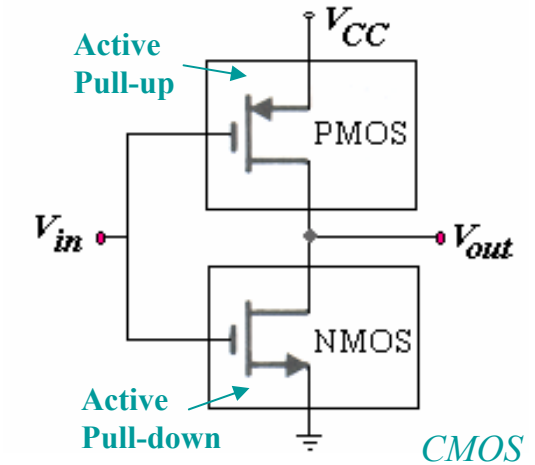
DTL NOR Gate

- Further improvement of the DTL gates were achieved by using multiple transistors, called transistor transistor logic (TTL) circuits,

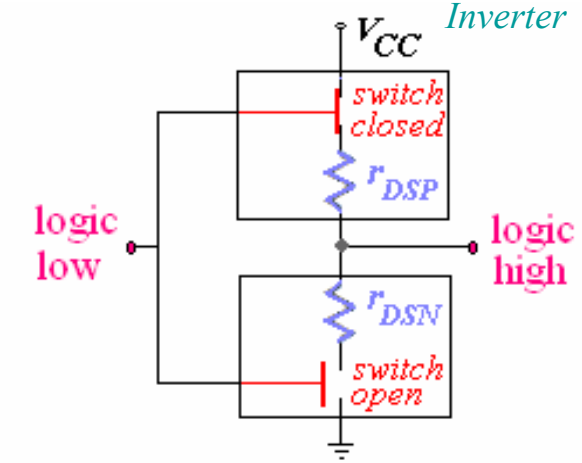
- The logic gates belonging to this family were very popular due to its microchip- area-efficient design and the use of multi-emitter transistor.

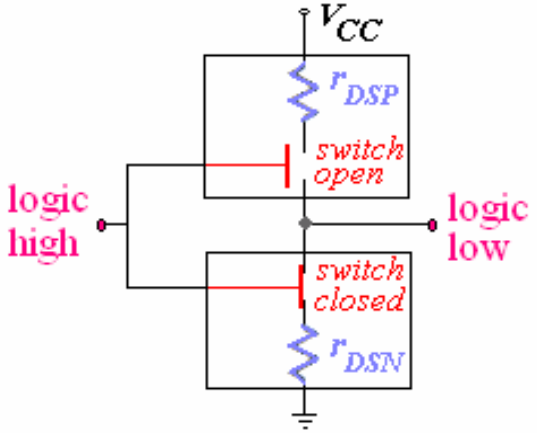
TTL ➔ CMOS Inverters ➔ BiCMOS :

- MOS is used to make voltage controlled switches, as it consumes low power and has very small size.
- In CMOS inverters, complementary switches made of NMOS and PMOS are used as a pull-down and pull-up networks, respectively.
- If V_{in} = logic low or '0', the PMOS will be ON, whereas the NMOS will remain OFF. Consequently, the circuit will source current to output device and V_{out} = logic high or '1'
- If V_{in} = logic high or '1', the PMOS will be OFF, whereas the NMOS will turn ON. Consequently, the circuit will sink current from any output device and circuit output, V_{out} = logic low or '0'
- BiCMOS combines advantages of TTL & CMOS



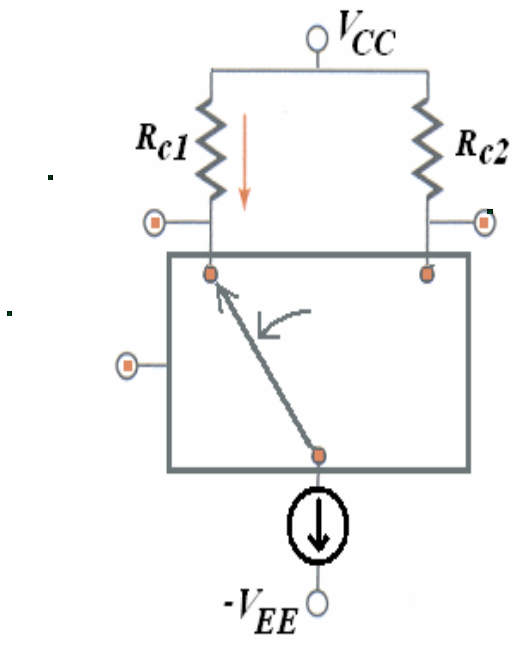
CMOS Inverter

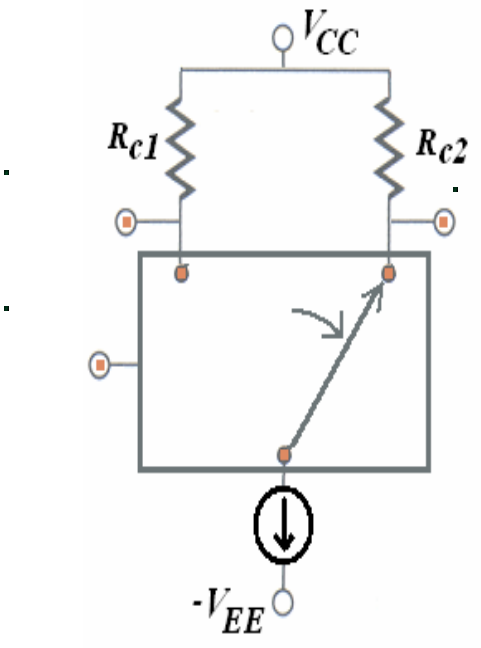


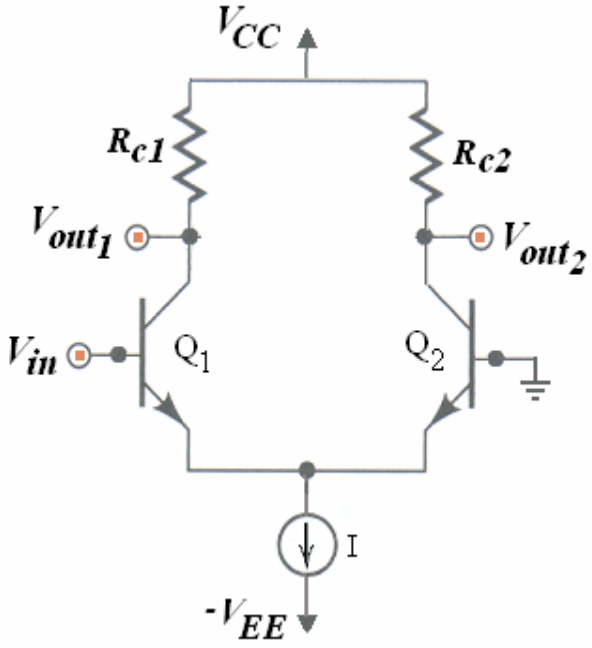


Another Type (ECL) of Logic Inverters :

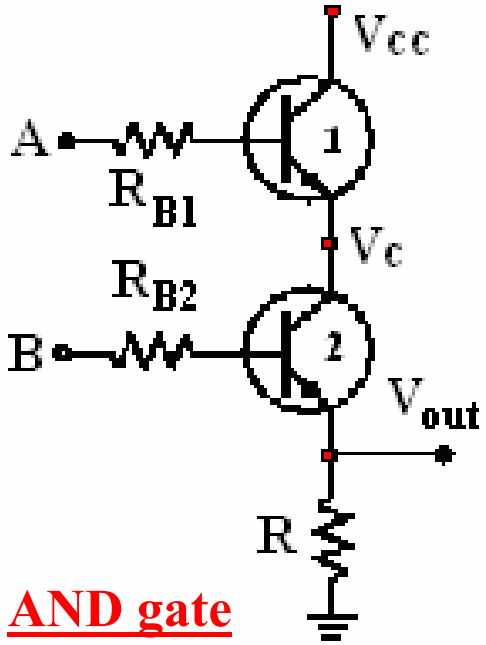
- Emitter coupled logic (ECL) gates uses double throw switches to realize logic inversion.
- This current steering logic arrangement is implemented using differential amplifiers, & yields the fastest available digital logic gates.
- This is because the ECL operates BJT's in active modes, and thus don't have storage time delay (from operating in Saturation and cutoff regions)



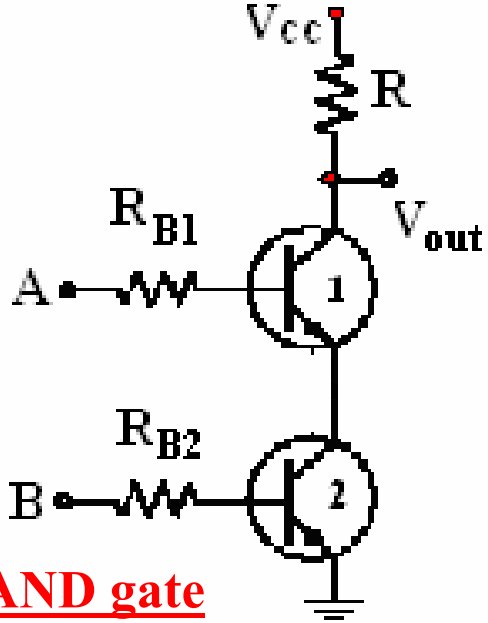




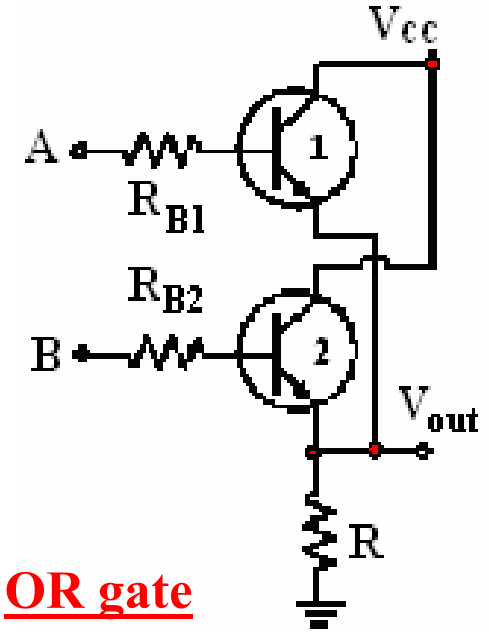
Resistor Transistor Logic (RTL) Gates: (For your information only)



AND gate



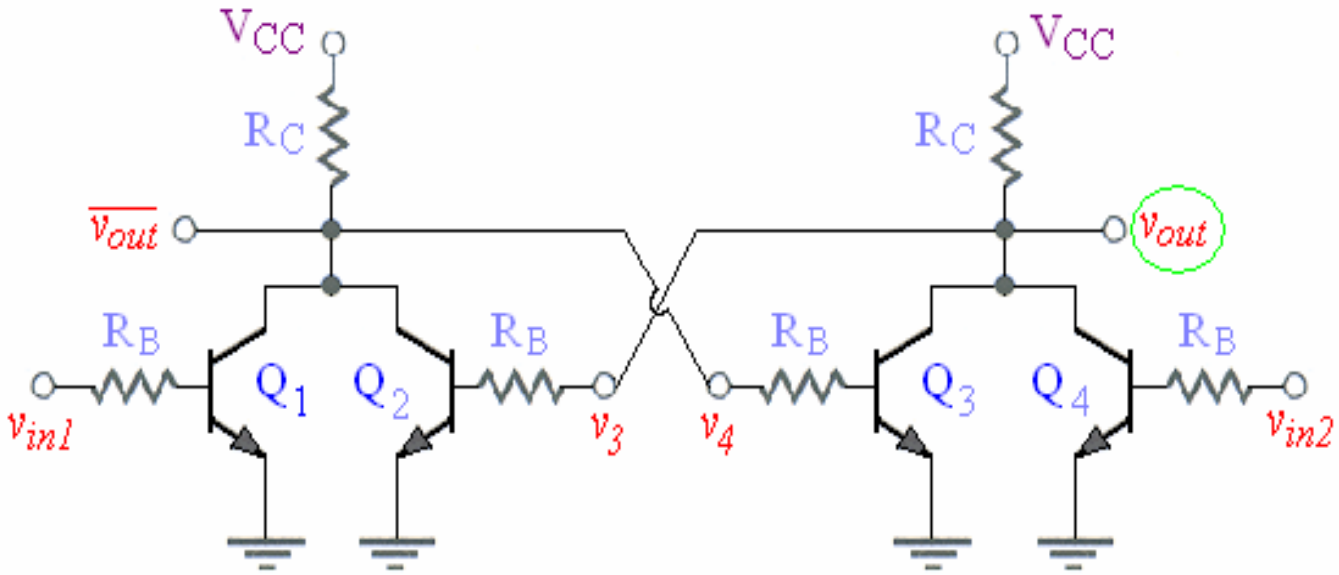
NAND gate



OR gate

Example: Find the logic function implemented by this RTL circuit.

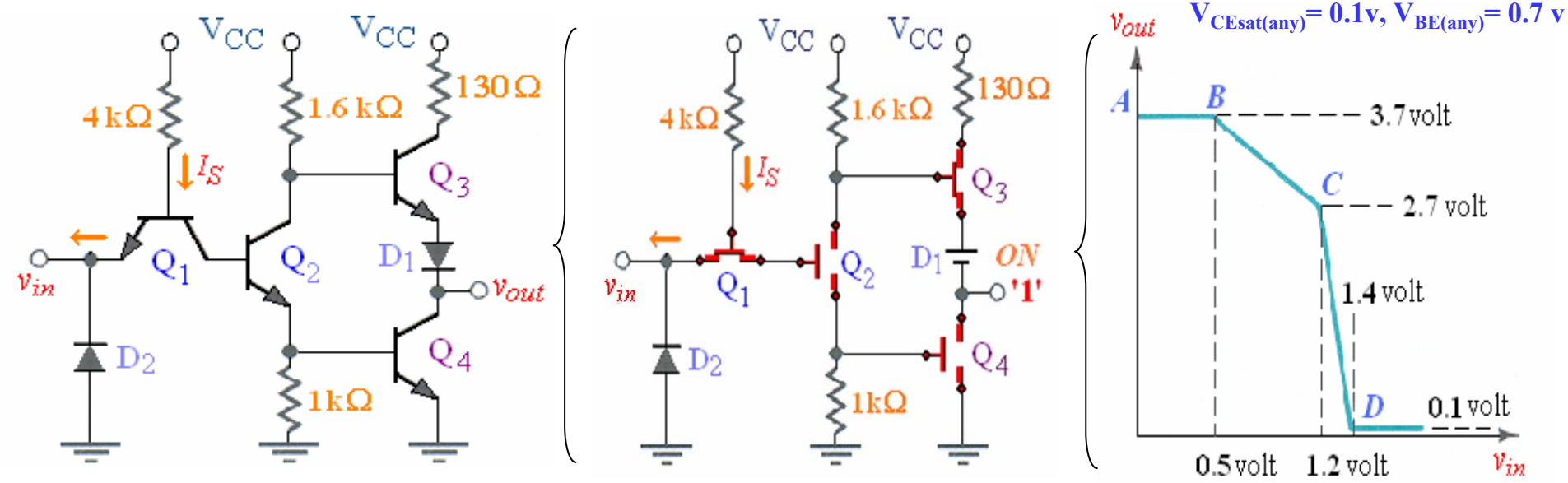
Solution: SR Flipflop (v_{in1}=S, v_{in2}=R v_{out}=Y)



Transistor-Transistor Logic (TTL) Inverter: (using BJT Switches)

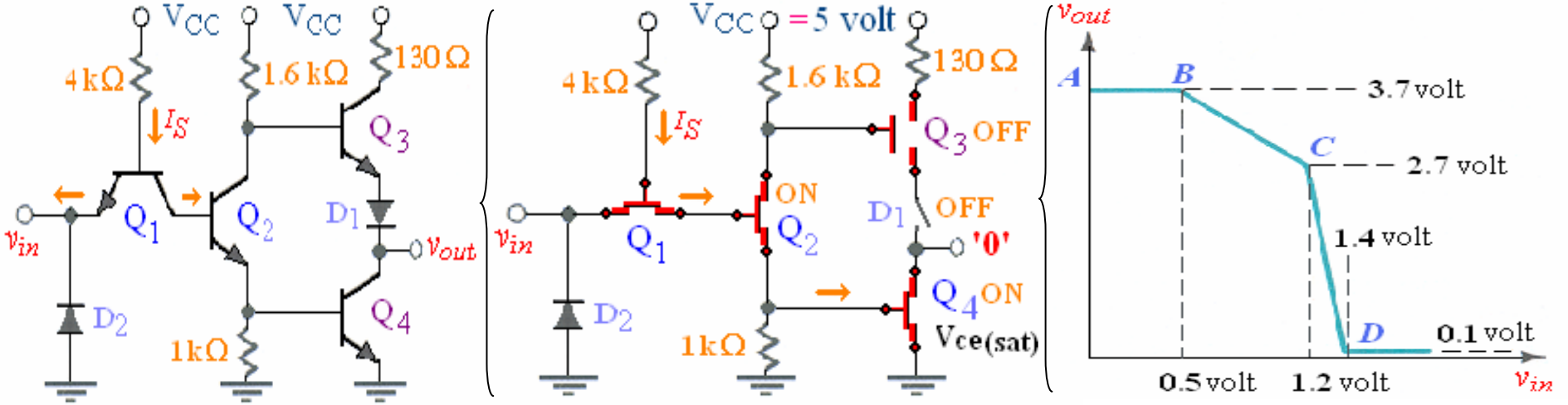
- Evolved from DTL circuits. Diodes are replaced with multi-emeter BJT's for more area-efficient IC desing. In TTL, BJT's operate in inverse active mode.
- TTL has Input stage, Driver stage and Output stage.

Say V_{CC}= 5 v , $V_{D\,(any)}$= 0.7 v, $V_{CEsat(any)}$= 0.1v, $V_{BE(any)}$= 0.7 v



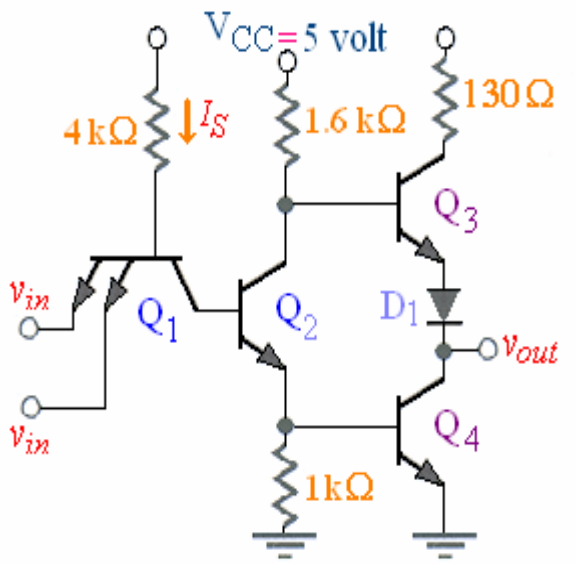
- For '$0<v_{in}<0.5$v' => Q_1 is ON (sat.) and V_{out} is given by section 'AB'.
- At 'A', Q_2=Q_4=off as V_{BQ2}=**0.1**, thus Q_3 & D_1 remain ON. V_{out}=logic 1
- At 'B', $(V_B)_{Q2}=V_{in}+(V_{CEsat})_{Q1}$=**0**.5+0.1=0.6v, thus Q_2 begins to turn ON
- For '$0.5<V_{in}<1.2$v' => Q_1 remains ON and V_{out} is represented by 'BC'
- If V_{in} increases from 0.5v , $(V_B)_{Q2}$ increases (V_B>0.6v) and Q_2 operates as an amplifier with more and more 'I_S' diverted to its base as $(I_B)_{Q2}$.
- Consequently, $(I_E)_{Q2}$ and $(V_B)_{Q4}$ increases but still remains insufficient (*as <0.6 volt*) to turn Q_4 ON. Thus, Q_3 and D_1 remains ON and V_{out}='1'

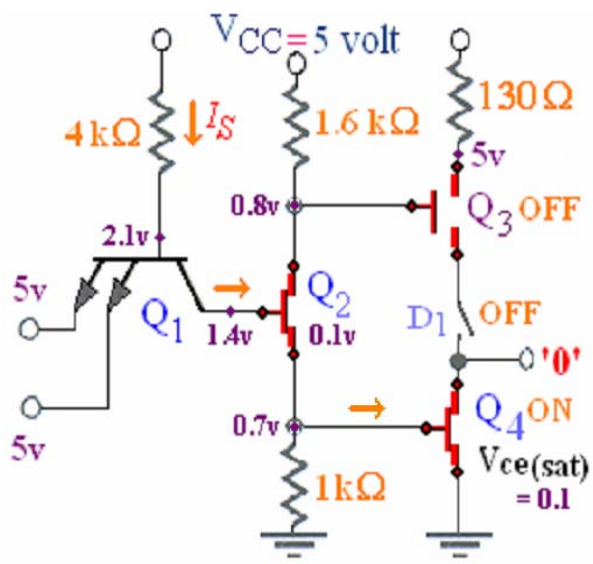
- 'BC' => Since Q_1 is sat. , an increase in input voltage will appear at base of Q_2, as $(V_C)_{Q1}=(V_B)_{Q2}$. Thus, Q_2 starts to turn on after point B
- Thus at point B, Q_2 is OFF => $(V_E)_{Q2}=0$; But at point C, Q_2 is in active region & Q_4 is close to turn-on as $(V_E)_{Q2}=<0.6v$; yields $0<(I_E)_{Q2}=<0.6mA$

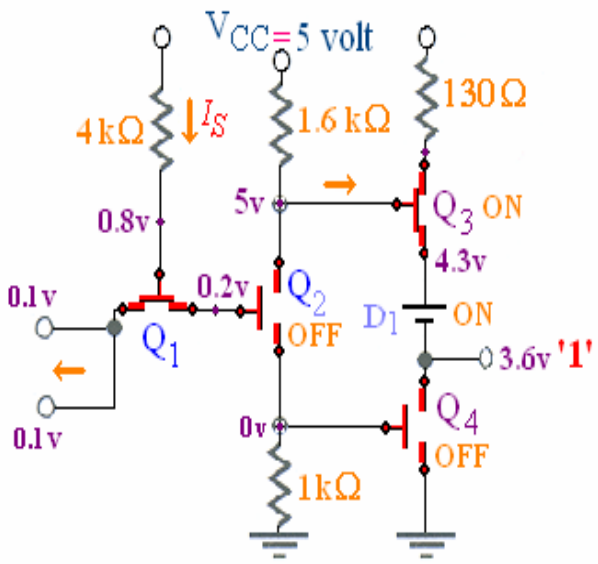


- For '$1.2<V_{in}<1.4v$' => Q_1 is ON and V_{out} is given by 'CD'. At 'C', Q_4 starts to conduct as $V_{in}=(V_{BE})_{Q4}+(V_{BE})_{Q2}-(V_{CEsat})_{Q1}=0.6+0.7-.1=1.2v$
- As $(V_E)_{Q2}=0.6$ v, $(I_E)_{Q2}=0.6$ mA and $(V_C)_{Q2}=5-(0.6 \times 1.6k)=4v$; Thus, Q_3 and D_1 remains ON and $V_{out}=(V_C)_{Q2}-(V_{BE})_{Q3}-V_{D1}=4-.65-.65=2.7v$
- As V_{in} increases ; $(I_B)_{Q2}\approx(I_E)_{Q2}$ increases ; $(V_B)_{Q4}$ increases but $(V_B)_{Q3}$ decreases until Q_4 is saturated and Q_3 and D_1 is cut-off at 'D'. V_{out}='0'
- For $V_{in}>1.4$ volt, the EBJ of Q_1 becomes RB as $(V_B)_{Q1}=2.1$ volt. But the CBJ still remains FB and Q1 starts operating in an inverse-active mode.
- Thus, $(I_B)_{Q1}$ flows into the base of Q_2 and saturates it. Also $(I_E)_{Q2}$ saturates Q_4 and output is pulled to 'logic 0' state. $V_{out}=(V_{CEsat})_{Q4}=0.1$ v
- As $(V_B)_{Q3}=(V_B)_{Q4}+(V_{CEsat})_{Q2}=0.7+0.1=0.8v$, Q_3 switches OFF as it needs atleast $V_{out}+V_D+(V_{BE})_{Q3}=1.5v$ to turn itself and the diode ON.

TTL NAND Gates: As per design, Q1 ➔inverse active (CBJ is FB & EBJ is RB)



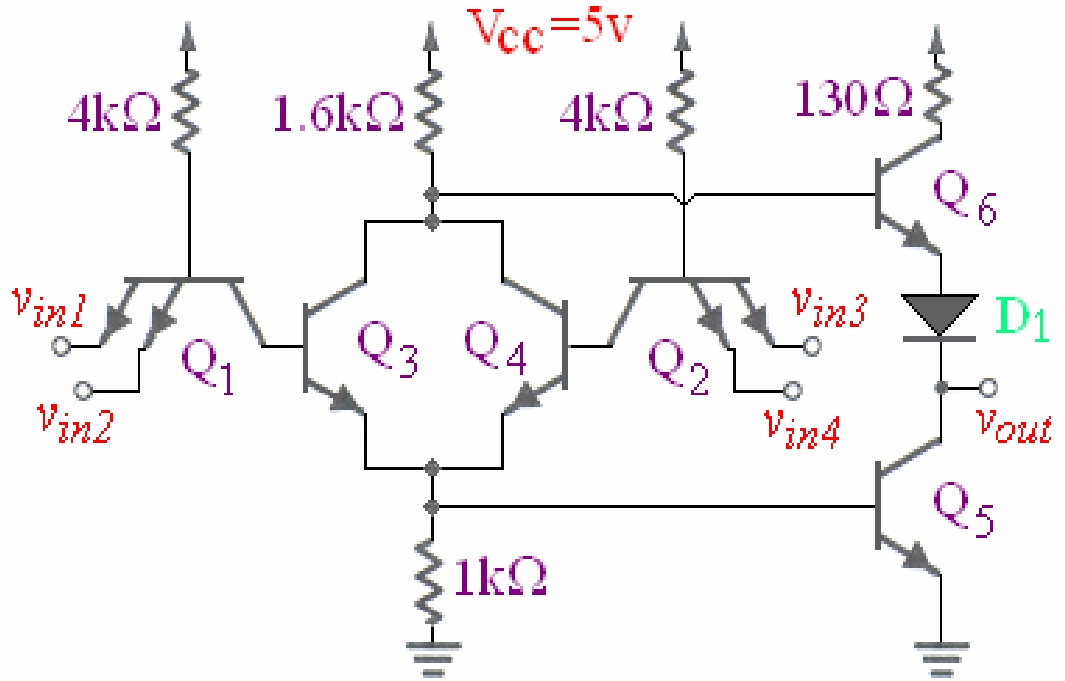




Characteristics of TTL gates	Propagation Delay (ns)	Power Dissipation (mW)	Speed-power product (pJ)
Standard TTL (*packaged in 54/74 IC series*)	10	10	100
Low-power TTL or 'LTTL'	33	1	33
High speed TTL or 'HTTL'	6	22	132
Schottky TTL or 'STTL' (*packaged in 74S IC series*)	3	19	57
Low-power Schottky TTL or 'LSTTL' (*in 74LS IC series*)	5	2	10
Advanced Schottky TTL or 'ASTTL' (*in 74AS IC series*)	0.075	20	1.5
Advance Low power Schottky or ALSTTL (*74ALS IC series*)	4	1	4

TTL Example Problem and solution:

Question: Analyze this TTL gate and find all the node currents and voltages for $V_{in1}=V_{in2}=V_{in3}=V_{in4}=$ '1' and $(V_{BE})_{D1}=(V_{BE})_{Q's}=0.7\text{v}$ and $(V_{CEsat})_{Q's}=0.2\text{v}$

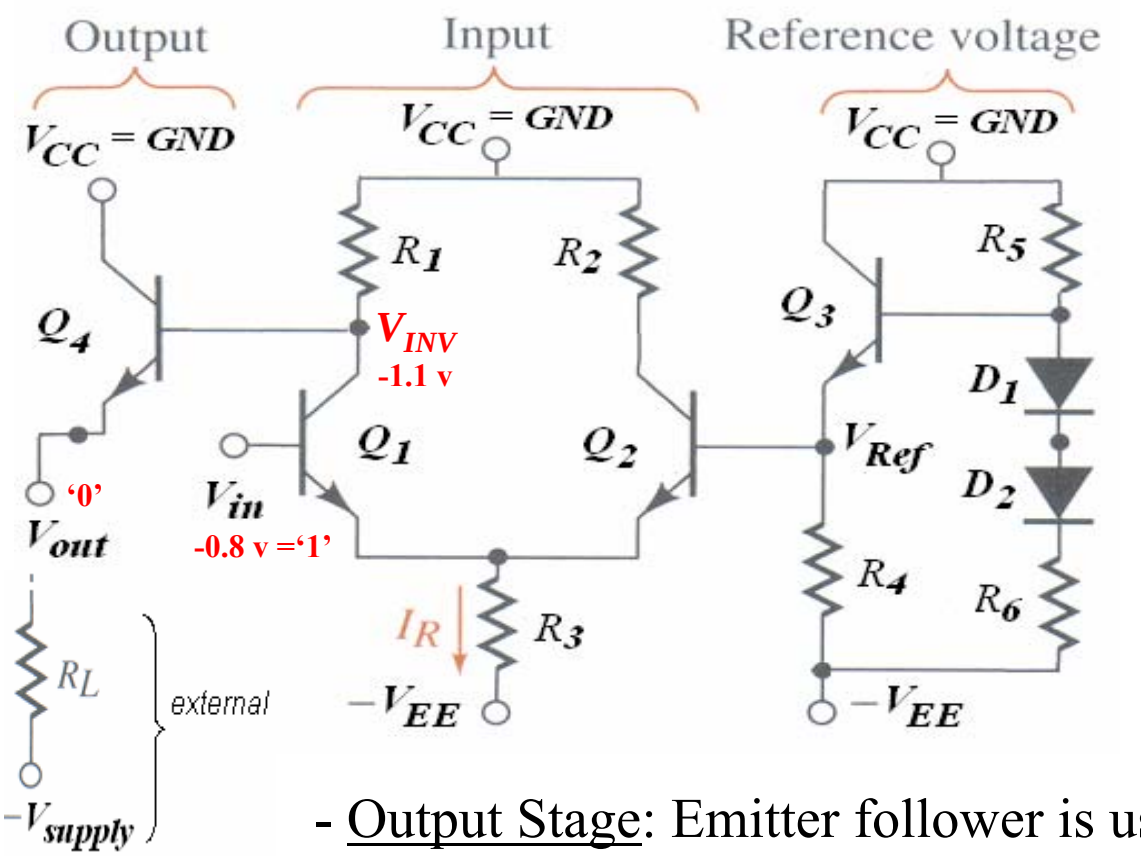


Solution: For all high inputs, Q_1 and Q_2 are in inverse active mode and resulting I_B's saturates Q_3, Q_4 and Q_5. Thus, $V_{B,Q1}=(V_{BE,Q5}+V_{BE,Q3}+V_{CB,Q1})=2.1\text{v} \Rightarrow V_{B,Q2}$. Thus $I_{B,Q1}=(5\text{-}2.1)/4k=.73\text{mA} \Rightarrow I_{C,Q1}$

Again, $V_{C,Q3,4}=V_{B,Q5}+V_{CEsat,Q3}=0.9\text{v}$, which is not enough to turn Q_6 & D_1 ON $\Rightarrow I_{B,Q6}=0$. So, $I_{1.6K\Omega}=(5\text{-}0.9)/1.6k=2.56\text{mA}$ & $I_{E,Q3,4}=I_{C,Q1}+I_{C,Q2}+I_{1.6K\Omega}=4\text{ mA}$ (as $I_{C,Q1}=I_{C,Q2}$) & $I_{1K\Omega}=.7/1k=.7\text{mA}$ & $I_{B,Q5}=4\text{-}.7=3.3\text{mA} \Rightarrow v_{out}=.2\text{v}$

Basic ECL (Emitter coupled logic) Inverters :

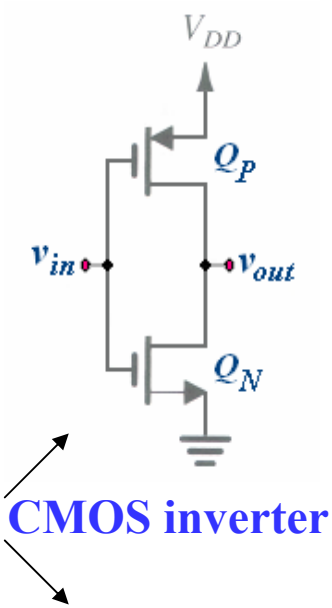
- ECL uses two voltage level about '-0.8 v' for logic-high and '-1.8 v' for logic-low



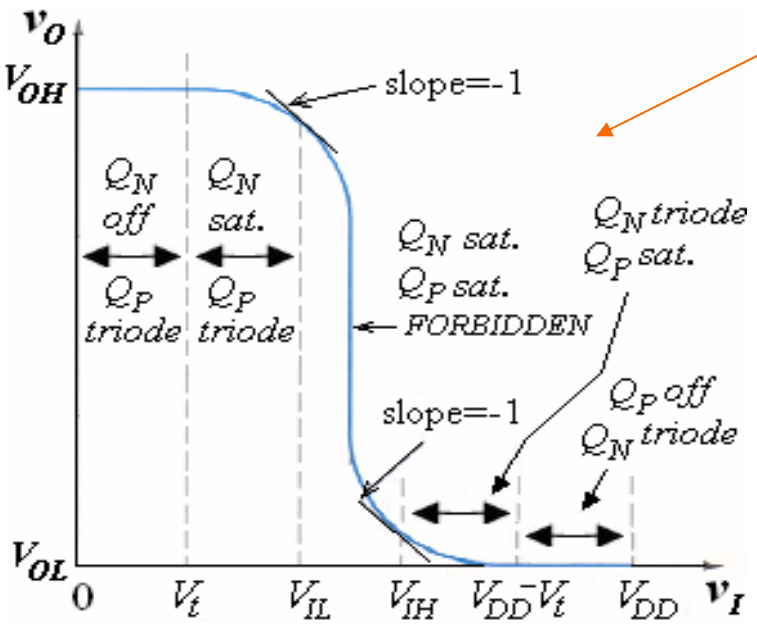
- In Reference Stage: Circuit components are selected to set the value of 'V_{Ref}=-1.3v', which is midpoint of signal logic swing from -.8 to -1.8v
- Input Stage: if V_{in} (-0.8 v) $>(V_{ref}+4V_T)$, Q_1 is ON and Q_2 is OFF. So current flows through Q_1. But, if $V_{in} < (V_{ref}+4V_T)$, Q1 is OFF and Q2 is ON. ***'I'*** flows via Q2

- Output Stage: Emitter follower is used to shift the output voltage logic level down by '$V_{BE(Q4)}$' (or 0.8 v) from that of 'V_{INV}'. This results (*shown later*) to an ECL output voltage logic swing of ; -0.8v to -1.8v. This stage also provides the gate with low output resistance and large output current to improve the gate FANOUT capability. The outputs are referenced to GND to improve the noise immunity of the gate.

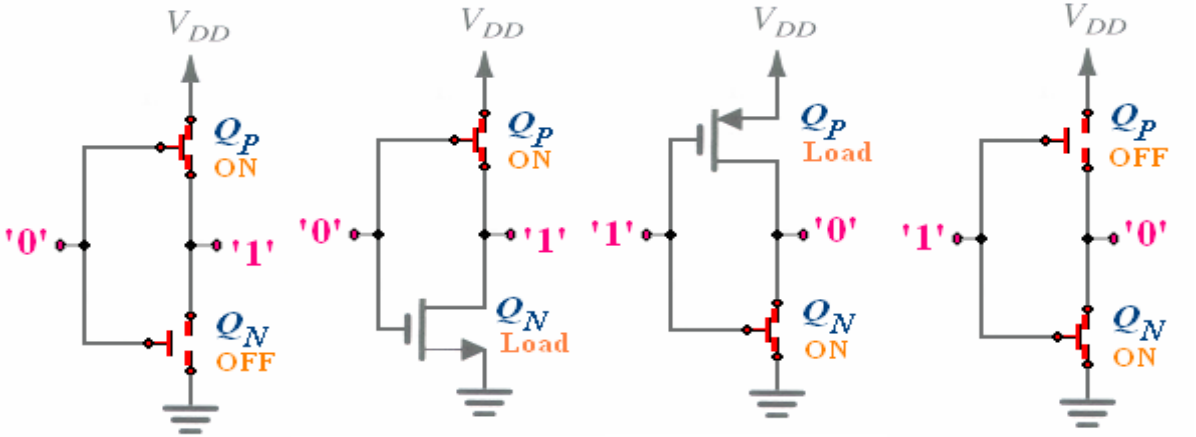
10.2: CMOS Inverter: - MOS logic circuits dissipates much less power. The high Z_{in} of MOS allows temporary charge storage, applied in memory circuits. MOS IC's has higher integration level due to optimized feature size and tight circuit packing.



CMOS inverter



See 10.2 (pg 957) for equations for Noise Margin, R_{DSn} , R_{DSp} , V_{th} ..



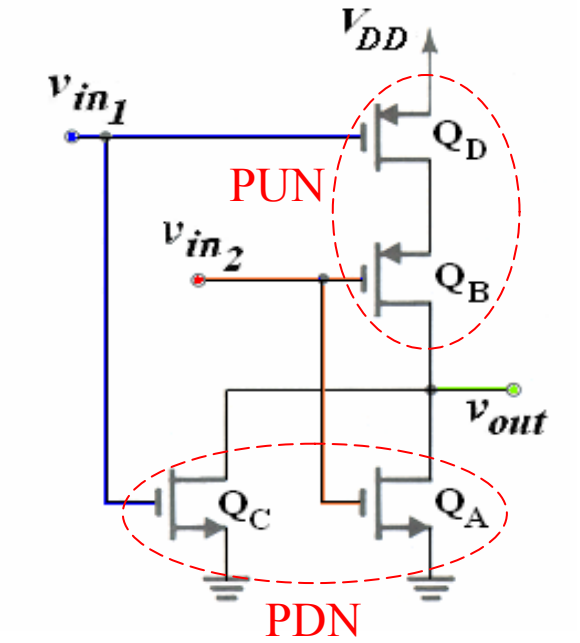
For '$0<v_i<V_t$'; since $v_{GSN}<V_t$ Q_N is OFF and since $v_{SGP}>V_t$ Q_P is ON. So Q_P pulls-up the output to logic-high level. Thus, $v_0 = V_{OH}$

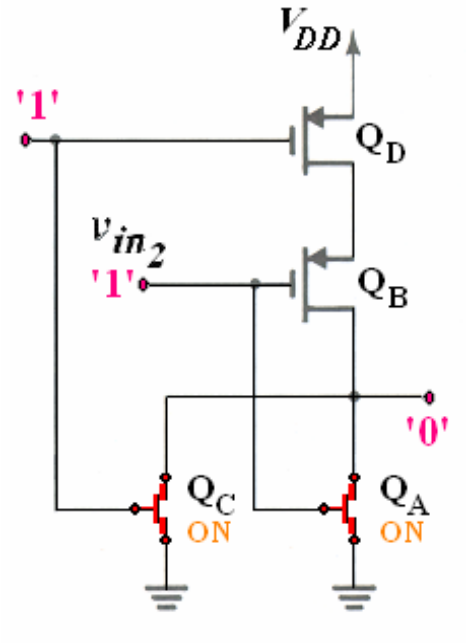
For '$V_t<v_i<V_{IL}$'; SAT Q_N acts as a load and Q_P remains ON. So Q_P pulls-up the output to logic-high level Thus, $v_0=V_{OH}$

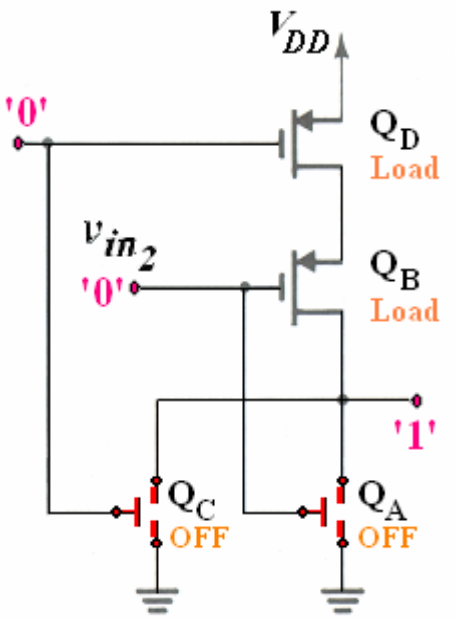
For '$V_{IL}<v_i<V_{IH}$'; Q_N and Q_P don't act as switch. So this is a forbidden region of operation

For '$V_{IH}<v_i<V_{DD}$'; Q_N is ON, Q_P acts as load or off. So the output is ➔ $v_0=V_{0L}$

10.3.2: CMOS NOR Gate: Note pull-up network (PUN), Pull-down network (PDN)



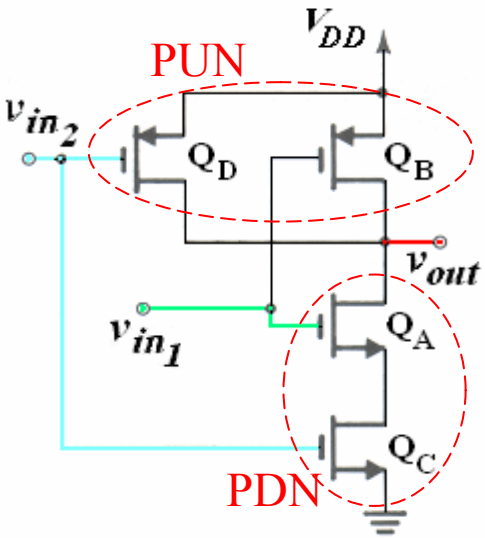


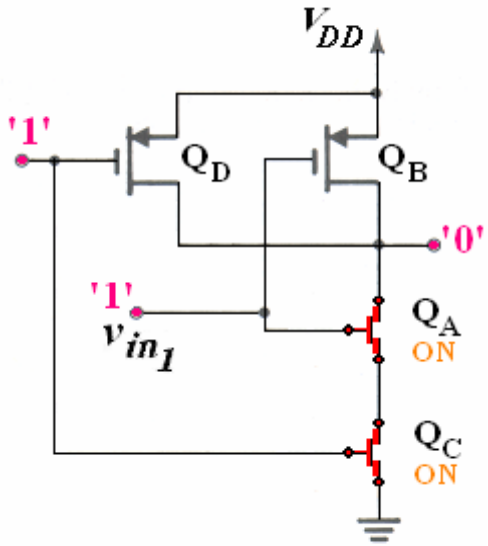


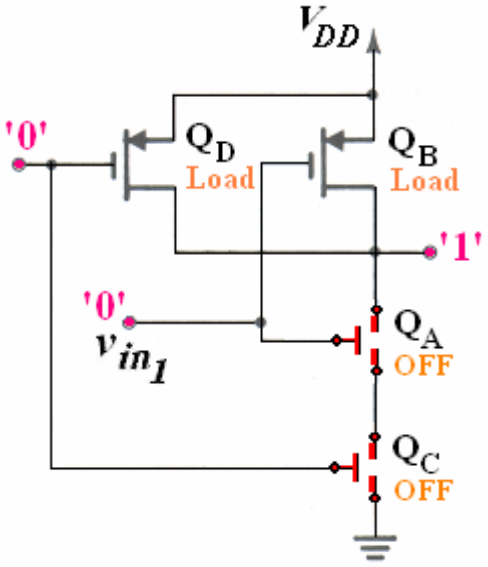
Q's are either Saturated or Cut-off or works as Active-load

PMOS ➔ PUN and NMOS ➔ PDN

10.3.3: CMOS NAND Gate:





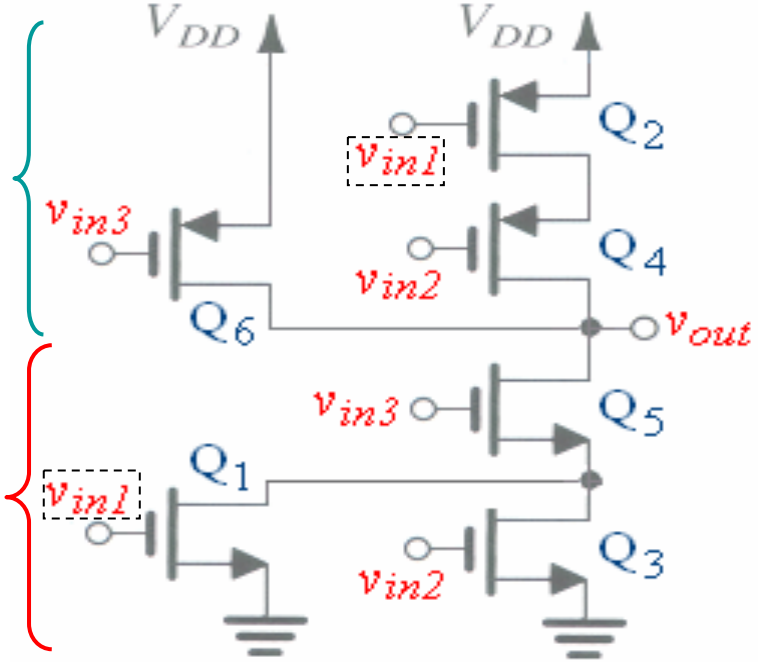


10.3.4/5: Use Demorgan's theorem (as in EE 200) to design the electronic circuit.

- Figure below: $v_{out} = \overline{v_{in3}} + \overline{v_{in1}}\,\overline{v_{in2}}$ ➔ PUN *and dual* $\overline{v_{out}} = v_{in3} \cdot (v_{in1} + v_{in2})$ ➔ PDN
- For a complex logic function: $Y = \overline{A(B+CD)}$ ➔ $\overline{A}+\overline{B}(\overline{C}+\overline{D})$. And the following CMOS circuit is shown in figure 10.14 of pg 968. Note the design of PUN & PDN's

Example on CMOS:

Question: Find the logic function performed by the following CMOS gate.



Solution: The gate consist of three CMOS, where Q_2, Q_4 and Q_6 (PMOS's) acts as PUN and Q_1, Q_3 and Q_5 (NMOS's) acting as PDN.

- if v_{in3} *or* (v_{in1} *and* v_{in2}) are at 'logic 0', switches Q_1, Q_3 and Q_5 remains OFF, but loads Q_6 *or* (Q_2 and Q_4) is ON $\Rightarrow v_{out} = '1'$

$$v_{out} = \overline{v_{in3}} + \left(\overline{v_{in1}} \cdot \overline{v_{in2}}\right) = \overline{v_{in3} \cdot (v_{in1} + v_{in2})}$$

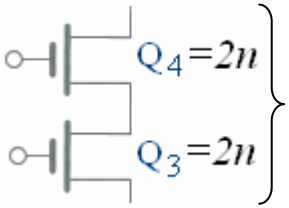
- if v_{in3} *and* (v_{in1} *or* v_{in2}) are at 'logic 1', loads Q_2, Q_4 and Q_6 remains OFF, but switches Q_5 *and* (Q_1 *or* Q_3) turns ON $\Rightarrow v_{out} = '1'$. So, LFP is, $\overline{v_{out}} = v_{in3} \cdot (v_{in1} + v_{in2})$; or, $v_{out} = \overline{v_{in3} \cdot (v_{in1} + v_{in2})}$

- Same results in both cases makes the gate consistance in terms of components

10.3.8: Transistor Sizing:

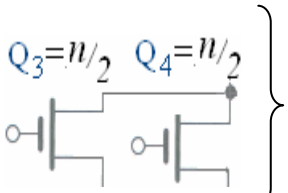
- **NMOS/PMOS, W/L selection is** to provide the gate with current-driving capability in both directions equal to that of a basic inverter.
- As an example of proper sizing, let us consider the previous two input CMOS NOR gate. For the pull-down network of this gate, the lowest current flow is obtained when only one of the NMOS switches are conducting. Thus, W/L ratio of each NMOS transistor can be equated to the W/L ratio of the NMOS switch of the basic inverter.
- But for the pull-up network, the worst case is obtained when all the inputs are at logic low and both series PMOS's are conducting. Since equivalent W/L ratio will be one-half of that of each PMOS transistor, the selected W/L ratio of each PMOS should be double compared to the W/L ratio of the PMOS transistor of a basic inverter.

For series connected MOSFET:



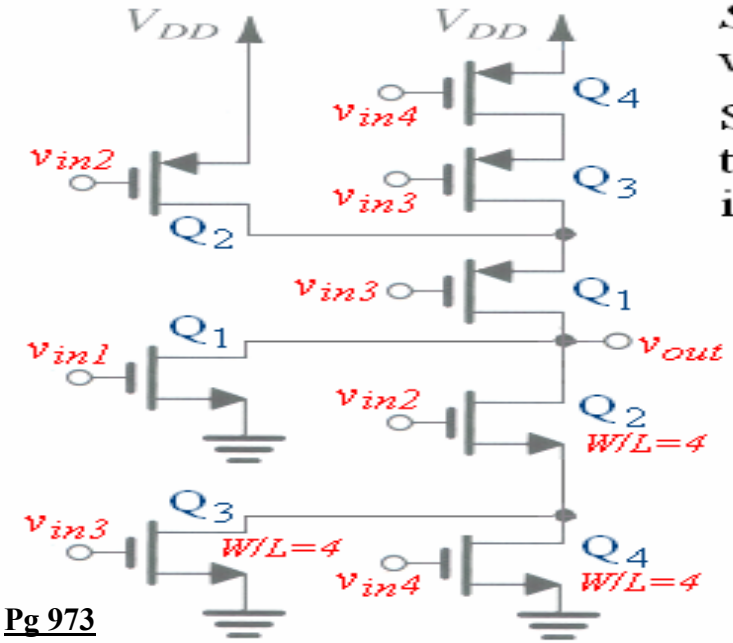
$(W/L)_{Q's}$= 2n;
½ * 2n = n,
or ≈ to that of a basic inverter

For parallel connected MOSFET



$(W/L)_{Q's}$= n/2
2*0.5n = n,
or ≈ to that of a basic inverter

Q: If the basic inverter has $n=2$, $p=5$, find the W/L ratios for all the MOS's.



Solution: For the PDN, the worst case occurs when NMOS's Q_2 and either Q_3 or Q_4 is ON.

Since, two transistors are in series, W/L of the transistors should be twice compared to basic inverter's Q_N. Thus, W/L *of* $Q_2=Q_3=Q_4=2n=4$

For the PUN, the worst case occurs when PMOS's Q_1, Q_3 and Q_4 are ON. Since, in this case, three transistors are in series, W/L of each of these transistors should be three times of that of Q_P in the basic inverter.

Thus, $(W/L)_{PMOS}$ *of* $Q_2= Q_3= Q_4= 3\,p=15$

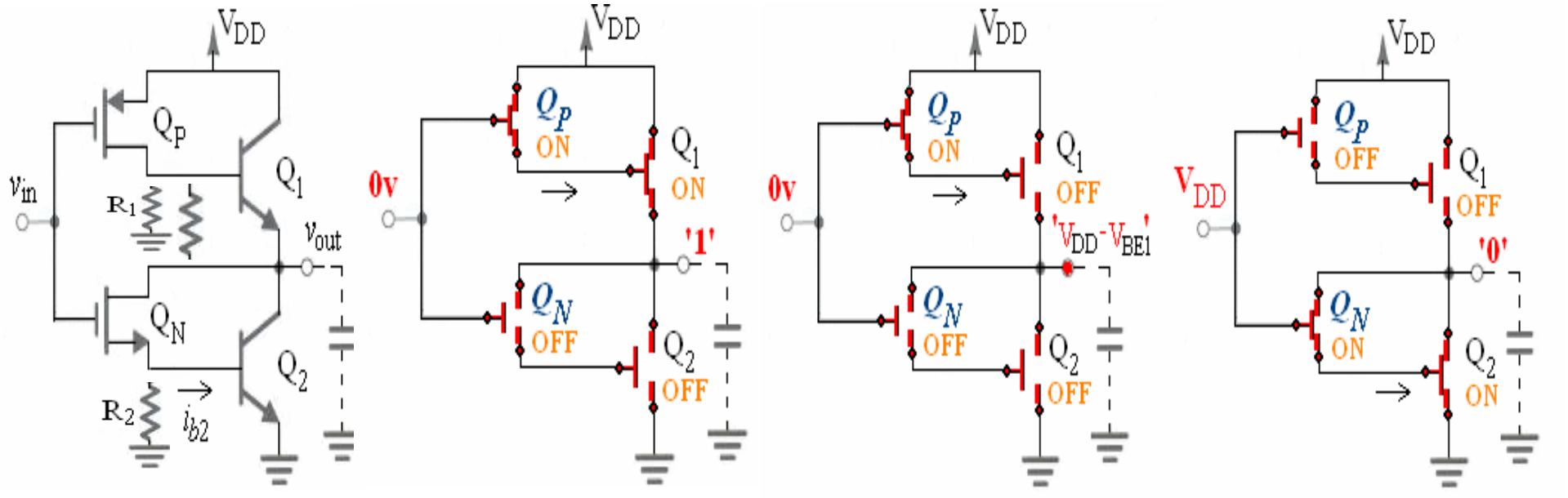
Similarly, it can be shown that for $(Q_1)_{NMOS}$, W/L $= n = 2$ and $(Q_2)_{PMOS}$, W/L $= 1.5p = 7.5$

Pg 973

BICOMOS logic gates:

- BiCMOS is a VLSI technology that unites Bipolar and CMOS circuits on the same chip to combine the advantages of both logic families. Consiquently, BiCMOS digital gates enjoys both, the low-power, high- input-impedance and wide-noise-margin of CMOS and the high current- driving-capability and high-speed-switching of BJT
- Furthermore, since BiCMOS technology is well suited for implementing high-performance analog circuits, realization of both analog and digital functions on the same IC chip or 'system on a chip' becomes attainable.
- BiCMOS Logic Gates are especially suitable for large capacitive loads (greater than 0.5 pF or so) or when the logic gate has to drive a number of other logic gates, requiring large amount of output current.
- Modern BiCMOS, invented by intel, was available in the market in 1992 and was eventually used to construct VLSI chips for personal computers.

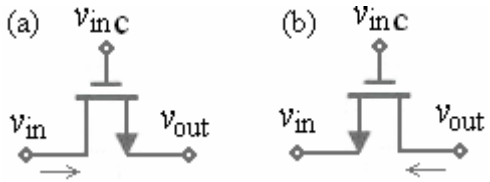
Basic BiCOMOS logic inverter:

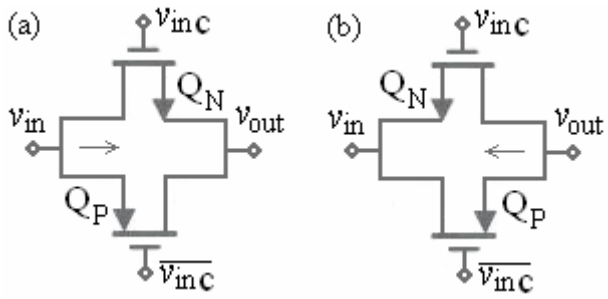


- BiCMOS inverter consist of a CMOS inverter (Q_P, Q_N) and a BJT output stage (Q_1, Q_2)
- For **logic low input** => Q_N turns OFF, leading Q_2 to remain OFF. But Q_P turns ON and supplies base current to Q_1. Consequently, Q_1 turns ON and supplies load current
- But, Q_1 turns off when $v_{out}=V_{DD}-V_{BE1}$ => Disadvantage: $V_{OH}<V_{DD}$ by V_{BE1}
- For **logic high input** => Q_P turns OFF resulting Q_1 to remain OFF. But Q_N turns ON, and the supplied base current turns Q_2 ON, which provides a large current path to quickly discharge capacitive load. Since, Q_2 turns off when $v_{out}=V_{BE2}$, & leads to a disadvantage of $V_{OL}= V_{BE2} \neq$ '0'. Improvement ➔ bleeder-resistors, R_1 & R_2 ➔ $R_{1,\text{ not GNDed}}$

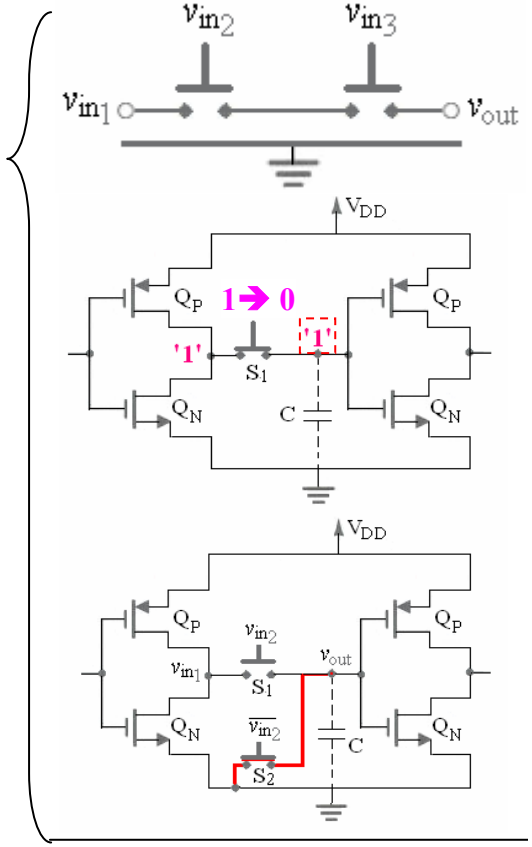
Pass Transistor Logic (PTL) Circuits: Also called 'transmission-gate logic'

- In PTL technology, logic circuits use series and/or parallel combination of NMOS or CMOS switches to provide low resistance paths to either V_{CC} or GND. A PTL 'AND gate' is shown in figure with logic function of; $v_{out} = v_{in1} \cdot v_{in2} \cdot v_{in3}$
- NMOS and CMOS switches for implementing PTL switches:





(a) operation during low-to-high transition of v_{in}
(b) operation during high-to-low transition of v_{in}



For CMOS switches, if *vout*= '0', *vinC= VDD* and *vin* changes state from low to high (*vin=> VDD*) => transistors *QN* and *QP* both conducts. Thus, *iout* is the sum of; *iDN= 0.5kn(VDD-Vtn-vo)2* and *iDP= 0.5kp(VDD-|Vtn|)2*. But as *vo=>VDD-Vtn*, *iDN=>0,* although *iDP* continues to charge *C* until *vo=VDD*. Thus, *tPHL* of CMOS is lower then NMOS due to extra initial current, *iDP*.

For CMOS switch in fig. b, when *vin=> 0*, *QN* and *QP* interchanges roles.