Handout 4

MOSFET

Sheikh Sharif Iqbal

(Ref: Text book and KFUPM Online course of EE-203)

(Remember to solve all the related examples, exercises problems as given in the Syllabus)
Chapter 4 – MOS Field-Effect Transistors (MOSFETs)

Text book: “Microelectronic Circuits by Sedra and Smith

- Metal-Oxide semiconductor Field-Effect Transistors (MOSFETs):

- MOSFET has been extremely popular since the late 1970s. Like transistors, the current flow between two terminals (Drain to source) in MOSFET are controlled by the third terminal (gate)

- Why MOS Transistors?
  • Takes smaller silicone area on the IC
  • Simple to manufacture
  • No need for biasing resistors.
  • Used in VLSI (very-large-scale integration)

- Comparison between MOSFET & BJT??
  • Can be made smaller /higher integration scale
  • Easier to fabricate /lower manufacturing cost
  • Simpler circuitry for digital logic and memory
  • Inferior analog circuit performance (lower gain)

- Most digital ICs use MOS technology.
- Also recently more and more analog circuits are implemented in MOS technology for lower cost integration with digital circuits in the same chip (IC)
4.1: Device Structure of MOSFET: The name of MOS is apparent from figures

- Four Terminals are Gate, Drain, Source & Body
- Unlike BJT, MOSFET is normally constructed as a symmetrical device (DS)
- Minimum achievable value of $L$ in a particular MOS technology is often referred as the feature size. Intel Pentium-4 uses 0.13 $\mu m$ technology.
- Lately poly-silicon with high conductivity is used instead of metal to form gates

\[
\begin{align*}
L &= 0.15 \text{ to } 10 \, \mu m, \\
W &= 0.3 \text{ to } 500 \, \mu m, \\
\text{MOS layer} &= 0.02 \text{ to } 0.1 \, \mu m.
\end{align*}
\]
BASIC OPERATIONAL THEORY OF NMOS: N-channel MOSFET considered

- The current controlled mechanism (for drain current) is based on electric field established by the voltage ‘$V_{\text{GS}}$’ applied to control terminal (gate).

- Current ($i_D$) is conducted by only one type of carrier “electrons (for NMOS or N-channel MOSFET) or holes (for PMOS)”. So FET is also called unipolar transistors.

Physical Operation with No $v_{\text{GS}}$: With no bias voltage is applied to gate, two back-to-back diodes between drain & source prevent the flow of $i_D$ as $v_{\text{DS}}$ is applied. ($R_{\text{DS}} \approx 10^{12} \, \Omega$)

Creating a Channel for $i_D$ flow: If ‘S’ & ‘D’ are GNDed and a ‘$+v_{\text{GS}}$’ is applied to ‘G’ holes are repelled from the channel region, leaving behind a carrier-depletion region.

Further increasing $V_{\text{GS}}$ attracts minority carrier (e⁻¹’s) from P-substrate into the channel region. When sufficient amount of e⁻¹’s accumulate near the surface of the substrate under the gate, an $N$ region (N-channel) is created-called as the inversion layer.
Applying a Small $v_{DS}$ or if $v_{DS} \approx (0.1$ or $0.2$ V) causes a current $i_D$ to flow through the induced $N$-channel from D to S. The magnitude of $i_D$ depends on the density of electrons in the channel, which in turn depends on $v_{GS}$. For $v_{GS} = V_t$ (threshold voltage), the channel is just induced and the conducted current is still negligibly small. As, $v_{GS} > V_t$, depth of the channel increases, $i_D$ will be proportional to $(v_{GS} - V_t)$, known as effective voltage. Increasing $v_{GS}$ above $V_t$ enhances the channel, hence it is called enhancement type MOSFET. Note that $i_G = 0$, due to M.O. layer.

Now since the $v_{DS}$ drops across the channel length, this voltages decreases from $v_{DS}$ to 0 volt, as we travel along the channel from drain to source. Thus the voltage between the gate and the points along the channel becomes: $v_{GS}$-0 at source end and $v_{GS}$-$v_{DS}$ at the drain end. This shows that the channel don't have even depth, as the depth depends on voltage. Now increasing $v_{DS}$ beyond $v_{GS}$ value causes channel to pinchoff.

- THUS, $(v_{GS} - v_{DS}) > V_t$, or $v_{DS} < (v_{GS} - V_t)$ or $v_{GD} > V_t$ produce continues channel depth at drain end and results the MOSFET to operate in Triode region. Otherwise the MOSFET operates in Saturation region with pincoff channel and $i_D \propto v_{DS}$.
**Channel length Modulation:** If $v_{DS}$ is further increased from pinched-off channel ($v_{DS_{sat}}$), the channel length is reduced (by moving from drain end). This phenomena is known as “channel length modulation” & its affect on $i_D$ is incorporated by “$\lambda$”  

Note: Most of the problems here will assume $\lambda=0$
Physical Operation of Enhancement NMOS: 

For increasing $v_{DS}$, $v_{DS}$ appears as a voltage drop across the channel. Voltage across the oxide decreases from $v_{GS}$ at ‘S’ to $(v_{GS} - V_t)$ at ‘D’. The channel depth will be tapered and become more tapered as $v_{DS}$ is further increased.

Eventually, when $(v_{GS} - v_{DS}) = V_t$, the channel will be pinched off (see figures 4.5 & 4.7).

Increasing $v_{DS}$ beyond this value has no effect as $i_D$ saturates. Thus, MOSFET is now operating in the saturation region. Thus, $v_{DSsat} = v_{GS} - V_t$

MOSFET transconductance $k'_n = \mu_n C_{ox}$ is constant depend on the fabrication process.

$\mu_n =$ channel $e^{-1}$ mobility

$C_{ox} =$ cap. of unit area of channel

---

$\begin{align*}
\text{Triode} & \quad v_{DS} < v_{GS} - V_t \\
\text{Saturation} & \quad v_{DS} \geq v_{GS} - V_t
\end{align*}$

$\begin{align*}
\text{Current saturates because the channel is pinched off at the drain end, and } v_{DS} \text{ no longer affects the channel.}
\end{align*}$

Book Figure 4.6
4.2: Circuit Symbol for Enhancement type

The arrowhead on the source terminal points in the normal direction of current flow. Therefore, it indicates three things: (1) distinguishing the source from the drain, (2) indicates the polarity of the device and (3) designating the terminals.

**Three Regions:**

- **Cutoff region**
  \[ V_{GS} < V_t \]

- **Triode region**
  \[
  V_{GS} > V_t, \text{ and } V_{GD} > V_t
  \]
  \[
  (V_{GD} = V_{GS} + V_{SD} = V_{GS} - V_{DS}) > V_t \Rightarrow V_{DS} < V_{GS} - V_t
  \]
  \[
  i_D = \frac{k'}{2} \frac{W}{L} \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} v_{DS}^2 \right]
  \]

- **Saturation region**
  \[
  V_{GS} > V_t, \text{ and } V_{GD} = V_{GS} + V_{SD} = V_{GS} - V_{DS} < V_t
  \]
  \[
  i_D = \frac{k'}{2} \frac{W}{L} (V_{GS} - V_t)^2
  \]

**Figures from textbook**
**Example:** Use triode expression of \( i_D \), given in eq 4.5(a), to calculate \( r_{DS} \)

For Triode Region

\[
i_D = k'_n \cdot \frac{W}{L} \left[ \left( V_{GS} - V_t \right) \cdot V_{DS} - \frac{1}{2} \cdot V_{DS}^2 \right]
\]

However, for small \( V_{DS} \), then \( \frac{1}{2} \cdot V_{DS}^2 \) approaches zero.

The resulting equation then is

\[
i_D = k'_n \cdot \frac{W}{L} \left[ \left( V_{GS} - V_t \right) \cdot V_{DS} \right]
\]

To find the drain-to-source resistance

\[
r_{DS} = \frac{V_{DS}}{i_D} \quad \text{if other parameter are given}
\]

We can solve this \( r_{DS} \)

**Exercise 1:** For Enhancement type NMOS with \( V_t = 1V \) and \( k'_n(W/L) = 0.5 \text{ mA/V}^2 \), find \( i_D \) and whether the circuit below is operating as a switch or an amplifier.

(a) if \( V_{GS} = 4v \) and \( V_{DS} = 2v \)

(b) if \( V_{GS} = 4v \) and \( V_{DS} = 6v \)

**CMOS:** Cross section of a complementary MOS integrated circuit. Note that the PMOS transistor is formed in a separate \( n \)-type region, known as an \( n \) well. Another arrangement is also possible in which an \( n \)-type body is used and the \( n \) device is formed in a \( p \) well.

*Figures from text book*
Physical Operation of Enhancement PMOS: P-channel MOSFET.

(a) Simplified PMOS circuit symbol with connected source & body. (b) PMOS circuit. Note that $v_{GS}$ and $v_{DS}$ are negative and $i_D$ flows out of drain.

Since in PMOS, $V_t$ is negative, So $v_{GS} \leq V_t$ is used to induce a channel. Thus, $v_{SG} \geq |V_t|$

To operate in **Triode region**:

$$v_{DS} \geq v_{GS} - V_t$$

(Continuous channel)

$$i_D = k'_p \frac{W}{L} \left[ \left( v_{GS} - V_t \right) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$$

where $v_{GS}$, $V_t$, and $v_{DS}$ are negative and $k'_p = \mu_p C_{ox}$

To operate in **Saturation region**:

$$v_{DS} \leq v_{GS} - V_t$$

(Pinned-off channel) or $v_{GD} > V_t$

$$i_D = \frac{1}{2} k'_p \frac{W}{L} \left( v_{GS} - V_t \right)^2 \left( 1 + \lambda v_{DS} \right)$$

Neglecting $\lambda$,

$$i_D = \frac{1}{2} k'_p \frac{W}{L} \left( v_{GS} - V_t \right)^2$$

Thus to recap PMOS operation, the gate voltage has to be made lower than that of the source by at least $|V_t|$. To operate in Triode region, the drain voltage has to exceed the gate voltage by at least $|V_t|$, otherwise the PMOS operates in Saturation region.

**Exa 4.6:** Design the circuit of Fig. 4.24 so that the transistor operates in saturation with $I_D = 0.5$ mA and $V_D = +3$ V. Let the enhancement-type PMOS transistor have $V_t = -1$ V and $k'_p (W/L) = 1$ mA/V$^2$. Assume $\lambda = 0$. What is the largest value that $R_D$ can have while maintaining saturation region operation?

*The figure is given in next page:*

**Sol:** $V_{GS} = -2$ V: $R_{G1} = 2$ M$\Omega$ and $R_{G2} = 3$ M$\Omega$. $R_D = 8$ k$\Omega$

See book pg 268 for solution
4.2.5 & 4.2.6: some Practical Considerations of Enhancement MOS

■ The Body Effect

In ICs, the substrates of all NMOS are usually common and connected to the most negative power supply. If a source is not at this voltage level, the reverse-bias voltage $V_{SB}$ between S and B will widen the depletion region and in turn reduces the channel depth. The result is an increase of $V_t$:

$$V_t = V_{t0} + \gamma \left( \sqrt{2\phi_f} + V_{SB} - \sqrt{2\phi_f} \right)$$

where $V_t = V_{t0}$ with $V_{SB} = 0$.

$\phi_f$ is a physical parameter with $2\phi_f$ typically 0.6V, and $\gamma$ is a fabrication - process parameter.

It follows that the body voltage controls $i_D$; This is an undesired phenomenon know as the body effect.

Same situation exists in PMOS.

Body effect can cause considerable degradation in circuit performance (as shown in chapter 6 of book)

■ Temperature Effects

Both $V_t$ and $k'$ are temperature sensitive. The magnitude of $V_t$ decrease by about 2mV for every 1°C rise in temperature. This decrease in $|V_t|$ gives rise to a corresponding increase in drain current as temperature is increase. However, because $k'$ decreases with temperature and its effect is a dominant one, the overall observed effect of a temperature increase is a decrease in drain current.

PMOS circuit in previous Exercise 4.6

\[ V_{DD} = +5\, \text{V} \]
\[ V_D = +3\, \text{V} \]
\[ R_G1 \]
\[ R_G2 \]
\[ R_D \]
\[ I_D = 0.5\, \text{mA} \]
4.11: Depletion Type NMOS or n-channel MOSFET’s:
The depletion type MOSFET has similar structure to that of enhancement type but with a **physically implanted** channel (**instead of an induced channel**). Thus an n-channel depletion-type MOSFET always has an n-type silicone region connecting the source and drain (both +n) at the top of the type substrate. Thus, for any \(v_{DS}\) applied between the drain and source, \(i_D\) flows even if \(v_{GS} = 0\). Thus, the channel depth and hence its conductivity is controlled by \(v_{GS}\). Applying a ‘+ \(v_{GS}\)’ enhances the channel by attracting more e\(^{-}\)’s. Applying ‘– \(v_{GS}\)’ is said to deplete/reduce the channel.

![Figures from text book](image-url)
4.3: MOSFET circuits at DC:

**EXAMPLE** Design the circuit of Fig. 4.20, so that the transistor operates at $I_D = 0.4$ mA $V_D = 1$ V. The NMOS transistor has $V_t = 2$ V, $\mu_n C_{ox} = 20 \mu$A/V$^2$, $L = 10 \mu$m, and $W = 400 \mu$m. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

Since $V_D = 1$ V means operation in the saturation region, we use the saturation-region expression of $i_D$ to determine the required value of $u_{GS}$.

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_d)^2 \quad \Rightarrow \quad 0.4 = \frac{1}{2} \times 20 \times 10^{-3} \times \frac{400}{10} (V_{GS} - 2)^2$$

This equation yields two values for $V_{GS}$, 1 V and 3 V. The first value does not make physical sense since it is lower than $V_t$. Thus $V_{GS} = 3$ V. Referring to Fig. 4.20, we note that the gate is at ground potential; thus the source must be at $-3$ V, and the required value of $R_S$ can be determined from

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-3 - (-5)}{0.4} \quad \left\{ \begin{array}{l} \text{To establish a dc voltage of} +1 \text{ V at the drain, we must select} \quad R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5 - 1}{0.4} = 10 \text{ k}\Omega \end{array} \right.$$

**EXAMPLE** Design the circuit to obtain a current $I_D$ of 0.4 mA. Find the value required for $R$ and find the dc voltage $V_D$. Let the NMOS transistor have $V_t = 2$ V, $\mu_n C_{ox} = 20 \mu$A/V$^2$, $L = 10 \mu$m, and $W = 100 \mu$m. Neglect the channel-length modulation effect (that is, assume $\lambda = 0$).

**SOLUTION** Because $V_{DG} = 0$, the FET is operating in the saturation region. Thus

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_d)^2$$

$$0.4 = \frac{1}{2} (20)(10^{-3})(100/10)(V_{GS} - 2)^2$$

which yields two values for $V_{GS}$, namely 4 and 0. The second value obviously does not make physical sense since it is lower than $V_t$. Thus $V_{GS} = 4$ V, and the drain voltage will be $V_D = +4$ V.

The required value for $R$ can be found as follows: $R = \frac{V_{DD} - V_D}{I_D} = \frac{10 - 4}{0.4} = 15 \text{ k}\Omega$.
### 4.3: MOSFET circuits at DC:

**EXAMPLE** Analyze the circuit shown to determine the voltages at all nodes and the currents through all branches. Let $V_\text{f} = 1 \text{ V}$ and $k'_n(W/L) = 1 \text{ mA/V}^2$. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

**SOLUTION** Since the gate current is zero, the voltage at the gate is simply determined by the voltage divider formed by the two $10-\text{M}\Omega$ resistors,

$$V_G = 10 \times \frac{10}{10 + 10} = +5 \text{ V} \quad \Rightarrow \quad V_{GS} = 5 - 6I_D \quad \Rightarrow \text{ Assume Saturated}$$

Thus

$$I_D = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_t)^2 = \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2$$

which results in the quadratic equation: $18I_D^2 - 25I_D + 8 = 0$

This equation yields two values for $I_D$: 0.89 mA and 0.5 mA. The first value results in a source voltage of $6 \times 0.89 = 5.34$, which is greater than the gate voltage and does not make physical sense. Thus

$$\{v_{GS} = (v_G - v_S)\} > V_t$$

$$I_D = 0.5 \text{ mA}$$

$$V_S = 0.5 \times 6 = +3 \text{ V}$$

$$V_{GS} = 5 - 3 = 2 \text{ V}$$

$$V_D = 10 - 6 \times 0.5 = +7 \text{ V}$$

Since $V_D > V_G - V_t$, the transistor is operating in saturation, as initially assumed.

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**Exercise-2**: Solve the above problem in Fig.1, after replacing NMOS with PMOS ($P$-channel MOSFET) with $V_{t(\text{PMOS})} = -1 \text{ V}$. **Hint**: see example 4.5 (NMOS) & 4.6 (PMOS) solutions
CMOS DC circuits

Assuming $k'_n(W_n/L_n) = k'_p(W_p/L_p) = 1 \text{ mA/V}^2$, $V_{in} = -V_{tp} = 1 \text{ V}$ and $\lambda = 0$

$Q_P$ = cut off, as $V_{GS}$ of zero

$Q_P$ = OFF

$Q_N$ = triode region

$v_o$ will be negative, $v_{GD} > V_t$, or $V_{DS} < (v_{GS} - V_t)$

Biasing Using Constant Current source

Find $V_{OV}$, $V_{GS}$, $V_{G}$, $V_{S}$, $V_{D}$.

$V_t = 1.5 \text{ V}$, and

$k'_n(W/L) = 1 \text{ mA/V}^2$

$V_{DD} = 10 \text{ V}$

$R_D = 1.5 \text{ k} \Omega$

$I_D = 0.5 \text{ mA}$

$V_D = V_{DD} - R_D I_D$

$V_{OV} = V_{GS} - V_t$

$R_G = 4.7 \text{ M} \Omega$

$V_{SS} = -10 \text{ V}$

Figures from text book

assume small $v_{DS}$:

$I_{DN} = k'_n(W_n/L_n)(V_{GS} - V_t)V_{DS}$

$= 1[2.5 - (-2.5) - 1][v_O - (-2.5)]$

also From the circuit diagram:

$I_{DN} (\text{mA}) = \frac{0 - v_O}{10 (\text{k} \Omega)}$

These two equations yield:

$I_{DN} = 0.244 \text{ mA} : v_O = -2.44 \text{ V}$
Summary of DC biasing a MOS amplifier in discrete circuits:

- Single power supplier
- Since $I_G=0$, $R_{G_1}$ and $R_{G_2}$ can be very large, allowing large $R_{in}$
- $R_S$ provides negative feedback
- $R_D$ should be large for high gain and should be small for large signal swing.

- Two power suppliers
- Simpler bias arrangement.
- $R_G$ establishes a dc ground and presents a high input resistance to a signal that may be capacitively coupled to the gate.

- Even simpler and more direct bias.
- A constant-current source $I$ feeds the source terminal.

- Large resistor $R_G$ forces the $V_G$ to be equal to $V_D$.
- The output signal swing should be limited in the negative direction to $|V_i|$.

See text book
4.6: Small signal models for MOSFET amplifier:

(a) neglecting the dependence of $i_D$ on $v_{DS}$ in saturation region of operation (channel-length modulation effect);

(b) including the effect of channel-length modulation modeled by output resistor ($r_o$)

(c) T-model with output resistance,  $r_o = |V_A|/I_D = 1/(\lambda I_D)$

Remember that for PMOS: $V_t = -$ and
Calculating small signal parameter for MOSFET Amplifier:

**MOSFET transconductance**

Formula 1: \[ g_m = k'_n \frac{W}{L} (V_{GS} - V_t) \]

It indicates that \( g_m \) is proportional to the \( k' \), W/L ratio and \( (V_{GS} - V_t) \). However, a large \( V_{GS} \) reduces the allowable signal swing at the drain.

Formula 2: \[ g_m = \sqrt{2} k'_n \left( \sqrt{\frac{W}{L}} \right) \sqrt{I_D} \]

It shows:

1. for a given MOSFET, \( g_m \propto \) the square root of the dc bias current.
2. At a given bias current, \( g_m \propto \sqrt{W/L} \)

In contrast, the \( g_m \) of BJT \( \propto \) the biasing current \( I_C \) and is independent of the geometry.

Remember for PMOS, the calculation of \( g_m \), \( r_o \) and \( K'_n \) is calculated using \( |(V_{gs} - V_t)| \), \( |V_A| \) or \( |\lambda| \) and replacing \( \mu_n \) with \( \mu_p \), respectively. See book page 297

*Here for NMOS* \( K'_n = \mu_n C_{ox} \)

**Formula 3:** \[ g_m = \frac{I_D}{(V_{GS} - V_t)/2} \]

As compared with that of BJT, for which \( g_m = \frac{I_C}{V_T} \)

The transconductance value for MOSFET is much smaller than that of BJT in light of the fact that the values of \( (V_{GS} - V_t)/2 \) are at least 0.1 V or so.

In spite of their low \( g_m \), MOSFETs have many other advantages, such as high \( R_{in} \), small size, low power dissipation and ease of fabrication.
MOSFET As An Amplifier – Small-Signal Analysis:

**Example 4.10** Figure 4.38 (a) shows a discrete enhancement MOSFET amplifier in which the input signal $v_i$ is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance $R_L$ via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain and its input resistance. The transistor has $V_t = 1.5$ V, $k'_n(W/L) = 0.25$ mA/V$^2$, and $V_A = 50$ V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.

**Solution**

We first evaluate the dc operating point as follows.

As $I_G=0$, $V_{RG}=V_{10M}=0$, Thus $V_G=V_D$. Since $V_S=0$, $V_{GS}=V_{DS}$ transistor must operate in saturation region as $V_{DS}>(V_{GS}-V_t)$

$$I_D = \frac{1}{2} \times 0.25(V_{GS} - 1.5)^2$$
$$I_D = \frac{1}{2} \times 0.25(V_D - 1.5)^2$$

$$V_D = 15 - R_D I_D = 15 - 10 I_D$$

Two solutions: $I_{D1} = 1.0589$ mA and $V_D = 4.4$ V
$I_{D2} = 1.721$ mA and $V_D < 0$
which is not physically meaningful

So, $V_D = (15 - i_D \times 10K) = 4.4$ V $\Rightarrow V_{DS} \Rightarrow V_{GS}$
The value of $g_m$ is given by
\[
g_m = k' \frac{W}{L} (V_{GS} - V_t)
\]
\[
= 0.25(4.4 - 1.5) = 0.725 \text{ mA/V}
\]

The output resistance
\[
r_o = \frac{V_A}{I_D} = \frac{50}{1.06} = 47 \text{ k}\Omega
\]

Since $R_G$ is very large ($10\text{M}\Omega$), the current through it can be neglected.

\[
v_o \approx -g_m v_{gs} (R_D // R_L // r_o)
\]

Since $v_{gs} = V_i$, the voltage gain is
\[
\frac{v_o}{V_i} = -g_m (R_D // R_L // r_o)
\]
\[
= -0.725(10//10//47) = -3.3 \text{ V/V}
\]

To evaluate the input resistance $R_{in}$, we note that the input current $i_i$
\[
i_i = \frac{(V_i - V_o)}{R_G}
\]
\[
= \frac{V_i}{R_G} \left(1 - \frac{V_o}{V_i}\right)
\]
\[
= \frac{V_i}{R_G} [1 - (-3.3)] = 4.3 \frac{V_i}{R_G}
\]

Thus,
\[
R_{in} = \frac{V_i}{i_i} = \frac{R_G}{4.3} = \frac{10}{4.3} = 2.33 \text{ M}\Omega
\]

- Remember channel length modulation is neglected in this solution.
- Solve exercise 4.24, 4.28 and hand-in next class.
4.7: **Common Source (CS) Amplifier**: Single stage MOS Analysis

\[ G_v = \frac{R_{in}}{R_{in} + R_{sig}} \]

\[ A_v = -\frac{R_G}{R_G + R_{sig}} g_m (r_o \parallel R_D \parallel R_L) \]

\[ R_{out} = r_o \parallel R_D \]

\[ \begin{align*}
  i_g &= 0 \\
  R_{in} &= R_G \\
  v_i &= v_{sig} \frac{R_{in}}{R_{in} + R_{sig}} = v_{sig} \frac{R_G}{R_G + R_{sig}} \\
  v_i &\approx v_{sig} \quad v_{gs} = v_i \\
  v_o &= -g_m v_{gs} (r_o \parallel R_D \parallel R_L) \\
  A_v &= -g_m (r_o \parallel R_D \parallel R_L) 
\end{align*} \]
4.7.4: **Common Source (CS) Amplifier with source resistance (Rs):**

\[
R_{in} = R_i = R_G \quad \text{and} \quad R_{out} = R_D
\]

As \( i_g = 0 \),

\[
v_i = \frac{R_G}{R_G + R_{sig}} v_{gs}
\]

here \( v_{gs} \) is only a fraction of \( v_i \).

\[
v_{gs} = v_i \frac{g_m}{g_m + R_s} = \frac{v_i}{1 + g_m R_s}
\]

\( v_{gs} \propto 1/R_s \)

Rs introduce ‘-’ feedback, that \( \uparrow \) the BW but \( \downarrow \) the gain by \((1 + g_m R_s)\) w.r.t CS

\[
i_d = i = \frac{v_i}{1 + R_s} = \frac{g_m v_i}{1 + g_m R_s}
\]

\( R_s \) reduces \( i_d \) by the factor \((1 + g_m R_s)\).

\[
v_o = -i_d (R_D \parallel R_L)
\]

\[
= -\frac{g_m (R_D \parallel R_L)}{1 + g_m R_s} v_i
\]

\[
A_v = -\frac{g_m (R_D \parallel R_L)}{1 + g_m R_s} v_i
\]

\( r_0 \) is neglected

**Figures from text book**
4.7: **Common Gate (CG) Amplifier**: acts as Unity gain current amplifier

\[ R_{\text{in}} = \frac{1}{g_m} \; ; \; \quad R_{\text{out}} = R_o = R_D \; ; \quad v_i = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} v_{\text{sig}} = \frac{1}{g_m} \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} v_{\text{sig}} \frac{1}{1 + g_m R_{\text{sig}}} = v_{\text{sig}} \frac{1}{1 + g_m R_{\text{sig}}}
\]

\[ i_i = \frac{v_i}{R_{\text{in}}} = \frac{v_i}{1/g_m} = g_m v_i \; ; \; \quad i_d = i = -i_i = -g_m v_i
\]

\[ v_o = v_d = -i_d (R_D \parallel R_L) = g_m (R_D \parallel R_L) v_i
\]

\[ A_v = g_m (R_D \parallel R_L)
\]

\[ G_v = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} A_v = \frac{1}{g_m} \frac{1}{R_{\text{in}} + R_{\text{sig}}} A_v = \frac{A_v}{1 + g_m R_{\text{sig}}}
\]
4.7: **Common Drain (CD) Amplifier**: acts as voltage amplifier

\[ R_{\text{in}} = R_G \quad ; \quad R_{\text{out}} = \frac{1}{g_m} \parallel r_o \]

\[ v_i = v_{\text{sig}} \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} = v_{\text{sig}} \frac{R_G}{R_G + R_{\text{sig}}} \quad ; \quad R_G \text{ is much larger than } R_{\text{sig}} \quad ; \quad v_i \cong v_{\text{sig}} \]

\[ v_o = v_i \frac{R_L \parallel r_o}{(R_L \parallel r_o) + \frac{1}{g_m}} \]

\[ A_v = \frac{R_L \parallel r_o}{(R_L \parallel r_o) + \frac{1}{g_m}} \]

\[ G_v = \frac{R_G}{R_G + R_{\text{sig}}} \left( \frac{R_L \parallel r_o}{(R_L \parallel r_o) + \frac{1}{g_m}} \right) \]

which approaches unity for \( R_G \gg R_{\text{sig}}, r_o \gg 1/g_m \), and \( r_o \gg R_L \).
4.4.4: **Operation as a linear Amplifier:** see page 279 of book for more explanation

Load line is drawn between the two extreme biasing points; (1) when \( i_D = 0 \), \( v_o = V_{DD} \); (2) since slope = \( 1/R_D \), \( i_D = V_{DD}/R_D \) (when max \( i_D \) is flows)

As \( v_i \) varies, \( v_{GS} \) also varies and the Q-point moves along the load line. Thus, wrong Q-point will cause distortion in \( i_d \)

Triangular \( v_i \) is superimposed on a DC bias voltage

**FIG**

**Figures from text book**