



RECONFIGURABLE MULTIMEDIA DATAPATH FOR LOW COST MEDIA PROCESSORS

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ABSTRACT

Media processing involves complex signal processing algorithms that require high-speed integer and floating-point operations. Moreover, media signal processing with the wider and varying word lengths require reconfigurable architectures, which can be reconfigured for a variety of data formats, algorithms, and applications. This paper presents a new reconfigurable datapath organization for media signal processing supporting MPEG-1, MPEG-2, and MPEG-4 standards. A single datapath has been utilized for integer as well as floating-point operations, suitable for low cost consumer electronics media processors. The proposed datapath can support a maximum of 16 parallel single instruction multiple data (SIMD) integer operations and 2 parallel SIMD floating-point operations. New instructions have been developed to speed up the execution of Matrix Multiplication, Discrete Cosine Transform (DCT), Inverse Discrete Cosine Transform (IDCT), Fast Fourier Transform, 3D-Graphics and Synthetic & Natural Hybrid Video Coding (SNHC). These operations are implemented by re-using the hardware without significant increase in area and delay. The datapath has been modeled in Verilog using 0.25u CMOS library and synthesized using Synopsys. All operations are single-cycle running at 200 MHz.

Keywords: MPEG, VLSI, Computer Arithmetic, Multiplication, IDCT, Datapath.

المخلص

.MPEG-4 MPEG-2 MPEG-1

(SIMD)

Synopsis

CMOS

Verilog

.MHZ

1. INTRODUCTION

Low cost, low power, consumer electronics embedded media processors need a simple, and area efficient data path that can support MPEG standards and Synthetic & Natural Hybrid video Coding (SNHC, or 3D graphics support) [Nadehara, and Daito and Nakayama,1995], [Makino and Suzuki and Morinaka and Nakase and Mashiko, ,1995], [Suzuki, K.; et.al, 1999], [Mohri, A.; et. al, 1999] and [Fujishima, H.; Takemoto, Y.; Onoye, T.; Shirakawa, I, 1999]. The goal of this research is to develop a reconfigurable data path that can support integer as well as floating-point (FP) operations for low cost consumer low media processors

This paper presents the design of a data path organization and special SIMD instructions to support MPEG-1, 2, 4, SNHC and 3D graphics. The data path is reconfigurable, scalable, area efficient, and offers programmability for interactive use. The reconfigurability and area reduction is achieved by the efficient re-use of same hardware instead of using redundant hardware as done in [Schmookler, M.S., et. Al,1999] and [Suzuki, K.; et. Al.,1999]. The data path can assist in the efficient and flexible coding and representation of both natural (pixel-based) as well as synthetic (computer generated) data (SNHC) by integrating FP operation support with integer operations. In order to support multiple data types with variable word lengths and formats, special techniques are developed to reconfigure the multipliers, adders, and to perform condition resolution.

The remainder of the paper is organized as follows. In Section 2 the overview of the proposed data path is presented. In Section 3 integer instruction execution is described. Finally, results and comparisons are presented in Section 4.

2. OVERVIEW OF THE DATAPATH

In this Section, we present the data path organization. The data path supports operations on 128- and 64-bit signed unsigned integers and single precision floating-point numbers. Figure 1 shows the block diagram of the data path. This is a two-stage, pipelined data path. The first pipeline stage contains four 16x32 partitioned multipliers (blocks 1, 2, 3, and 4), two 64-bit partitioned comparators, and three 12-bit adders for FP exponent calculation and 4x4 Sum of Absolute difference (SAD) instruction. The second pipeline stage contains two 64-bit partitioned shifters, adders, and circuitry for normalization and rounding.

The data path instructions are divided into the following groups: 1) Add/Sub, Average, Shift, Logic and Permute 2) Multiply, Sum, Sum of Absolute difference, Pack and UNPACK, 3) Compare, Min, Max, Absolute value, and Absolute difference. All the instructions are SIMD type. All instructions have a latency and throughput of single cycle, except "Multiply, FP Multiply, FP Add, and SAD" that has a latency of two cycles and single cycle throughput. Following, we explain the implementation of some of these instructions using the proposed data path.

3. INSTRUCTION EXECUTION

In this section we present the instruction execution on the proposed data path Fig 2 shows the macro-level implementation of the two-cycle data path, containing four 16x32 multipliers, 3x2 compressors, and two 64-bit adder-sub tractors.

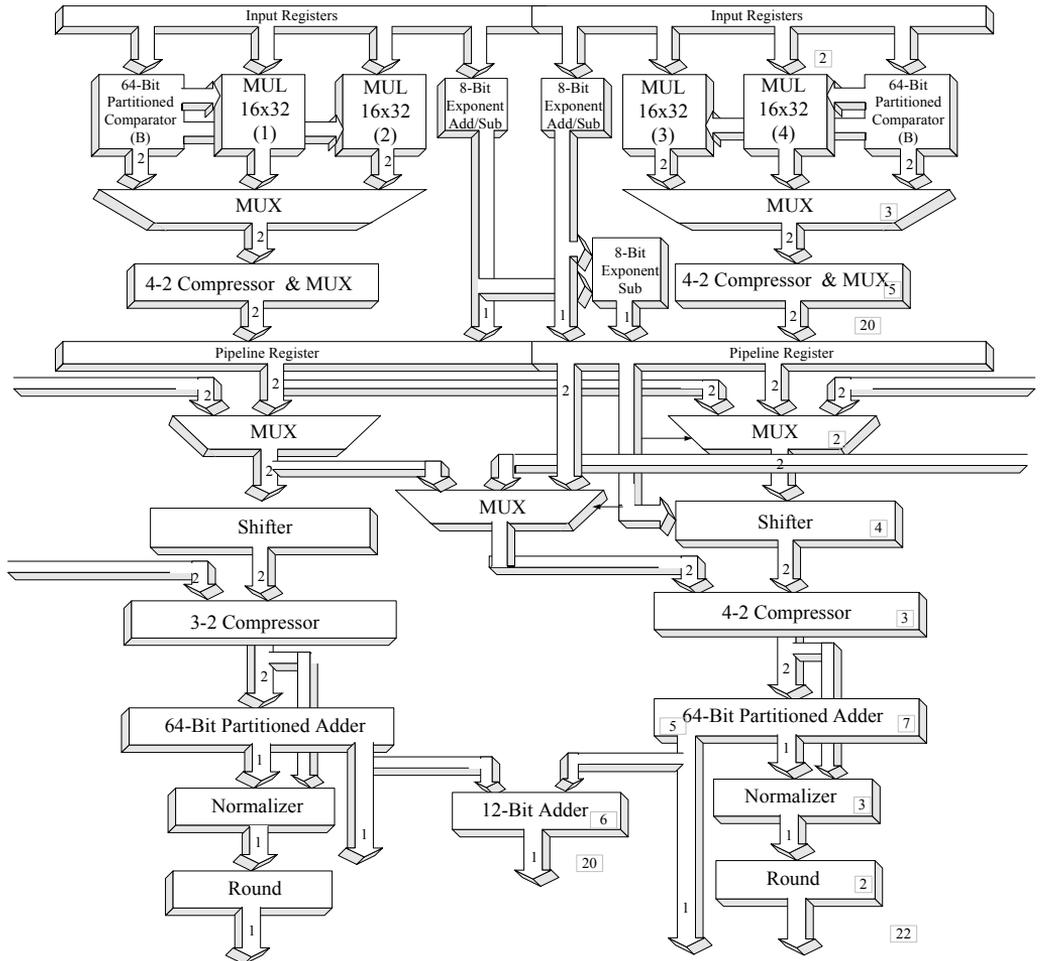


Figure 1: Block diagram of the proposed Data path

3.1. Add/Sub Instructions

The Add/Sub instructions are executed in the second pipeline stage of the data path using the 64 bit-partitioned adders. The partition of the 64-bit adders is performed according to the partition control signals as shown in Table 2. Since we require two 64-bit adders for the multipliers, therefore by re-using these adders we can support two 64-bit operations in parallel.

Table 3 shows the operation of these instructions on input operands A and B, the result is produced in C and D. The A, B, C, and D can be a byte, half-word, word, or double word packed as 8-bytes, 4-half-words, 2-words, and a double-word respectively; in a 64-bit register Rx, where x = 0...n.

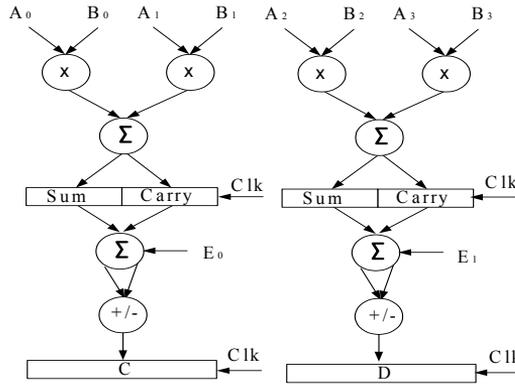


Figure 2: Macro-level implementation of the data path

The ADD and SUB operations are performed as normal Addition and Subtraction (with and without saturation). The parallel average of two numbers is a very common and useful function in image and video processing, (see Figure 3-a). Only few high performance ISAs [Oberman, et. Al,1999] support this operation. This combined operation involves an addition and a right shift of one bit (divide by two). In the proposed data path, AVG2 operation is implemented using the 64-bit partitioned adder; performing normal addition and finally shifting the result one bit right. The data path shifts in the carry out bit as the most significant bit of the result, so it has the added advantage that no overflow can occur.

Table 1
Instructions supported by the ALU (A, B, are the inputs, and C, D are the outputs)

Instruction	Operation	Result
ADD	A + B	C
ADS(U)	A + B	C or SAT(max)
ADS(S)	A + B	C or SAT(min) or SAT(max)
SUB	A-B	C
SUBS(U)	A-B	C
SUBS(S)	A-B	C or SAT(min) or SAT(max)
AVG2(U)	(A+B)/2	C
AVG2(S)	(A+B)/2	C

Table 2
Partition of the ALU, using Partition control signals.

Part1Part0	ALU partition
00	Byte
01	Half word
10	Word
11	Double word

3.2. MULTIPLY INSTRUCTIONS

The multiply instructions and their macro operations are shown in. These instructions are executed using 32x16 multiplier blocks of the data path. The partition of the multipliers is performed according to the partition control signals as shown in Table 1, (11 is used for 24-bit operation). The multiplier hardware is configured for signed and unsigned operation using the sign control bit. When 'Sign' bit is '1' signed multiplication is performed and when it is '0' unsigned multiplication is performed. This group of instructions requires two-cycle latency with a single-cycle throughput. Following we explain the execution of multiply and sum of products instructions.

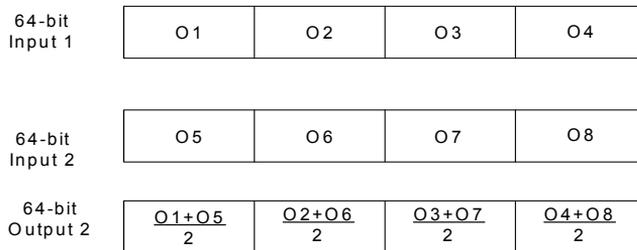


Figure 3: Parallel averaging operation.

3.3. Multiply

In multiply operation, the two input operands are multiplied in the first cycle producing Sum and carry vectors, and in the second cycle Sum and carry vectors are finally added using the 64-bit partitioned adder to produce the final result as shown in Figure 4. Since the result of multiplication is twice the width of the input operands, the result of simple multiplication is produced in C and D (C contains the lower half of the result and D contains the upper half of the multiplication). The only difference in MUL (U) and MUL(S), is that MUL(U) is the unsigned multiplication, while MUL(S) is the signed multiplication.

Table 3: Multiply operations supported by the proposed data path.

Description	Inst.	Operation
Mult. with full resol. (S/U)	MUL	$C = A * B$
Mult. with accumulate (S/U)	MULA	$C = A * B + C'$
Mult. with deduct (S/U)	MULD	$C = A * B - C'$
Multiply upper half result with round. (S/U)	MULH	$C = A_n * B_n$
Floating point Multiply	FP MUL	$(M_0 \times M_1, E_0 + E_1)$
3D-Floating point sum of two products	3D-FSMUL	$(M_3 \times M_2, E_3 + E_2) + (M_0 \times M_1, E_0 + E_1)$
Sum of 2 Integer prod. (S/U)	SUMP	$A_1 * B_1 + A_0 * B_0$
Sum of 2 products with accumulate (S/U)	SUMPA	$A_1 * B_1 + A_0 * B_0 + C'$
Sum of 2 products with deduct (S/U)	SUMPD	$A_1 * B_1 + A_0 * B_0 - C'$
Sum of 4 Integer prod. (S/U)	SUM4P	$A_3 * B_3 + A_2 * B_2 + A_1 * B_1 + A_0 * B_0$
Sum of Absolute difference	SAD	$\Sigma A - B $
Sum of eight operands	SUM8	ΣA
Pack (S/U) numbers	PK	
Unpack (S/U) numbers	UPK	

3.4. Sum4p

Sum of two products is supported by most of the high performance media processors, but at present no processor exists that supports Sum of Four products. This operation performs the addition of four products and it is equivalent to four multiply and three additions as shown below:

$$C = A_0 \times B_0 + A_1 \times B_1 + A_2 \times B_2 + A_3 \times B_3$$

Matrix multiplication is heavily used in IDCT, FFT, and other media signal processing algorithms. We have found that this operation (SUM4P) dramatically increases (2 to 1) the execution of matrix multiplication by performing seven operations in a single cycle. Moreover, by using this operation, high precision processing is done because the rounding error is reduced as compared to two sum of products operation, in which two rounded results are added to get the addition of four products. While in this case full precision addition of the four products is performed and then rounding is performed.

The proposed data path performs the addition of four products (SUM4P instruction) in two cycles with single cycle throughput. This operation is supported only for half-word operands. The instruction execution at macro level is shown in

Fig (5). This instruction requires four multiplications $A_3 \times B_3$, $A_2 \times B_2$, $A_1 \times B_1$, and $A_0 \times B_0$ these multiplications are performed in the first cycle using the MUL 32x16 blocks. The summation of two products ($A_3 \times B_3 + A_2 \times B_2$, and $A_1 \times B_1 + A_0 \times B_0$) is performed in the first cycle Fig (5) using the 4x2 compressor after the multipliers. Then, the summation of four 16x16 products is performed in the second cycle using the second 4x2 compressor. The sum and carry vectors produced by the summations are finally added using the 64-bit partitioned adder to produce the addition ($A_0 \times B_0 + A_1 \times B_1 + A_2 \times B_2 + A_3 \times B_3$) as shown in Fig(5).

In order to produce the result of the same bit width as the input the result of the addition is rounded and only the upper half of the result is stored in the output. As one can see from Fig(5), Sum of four products operation requires the same data path and components as required in Sum of two products for word operands, hence this instruction is implemented without any extra hardware cost and delay.

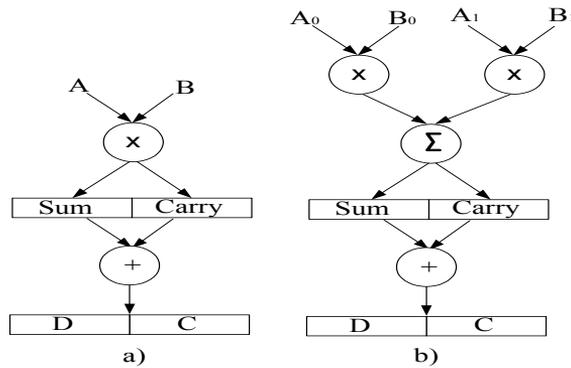


Figure 4: Two cycle multiply operation a) 8x8 or 16x16, and b) 24x24 or 32x32.

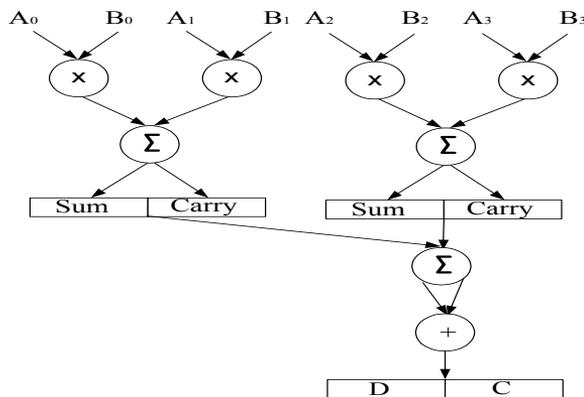


Figure 5: Sum of four products.

4. PERFORMANCE ESTIMATION

The data path performance is estimated for IDCT, Image reconstruction, and 3D Geometric Transformations using hand written assembly code. In this performance analysis it is assumed that the data is already available in the registers (loaded by the main processor or load store unit). Cache hit rate is assumed to be 100%, and instruction issue rate is one instruction/cycle. Add (ADD), Subtract (SUB), Average (AVG), Average of four operands (AVG4) and Permute (PERM) instructions operate on 128-bit data, while multiply related instructions operate on 64-bit data, Butterfly instruction perform two operations on two 64-bit operands and produce two 64-bit results.

The data path requires, a total of 192 cycles to perform an 8x8 (2D) IDCT matrix-vector implementation of IDCT, while [Fujishima, H.; Takemoto, Y.; Onoye, T.; Shirakawa, I,1999], [Bum and Yun and Lee,1997], [Yoshida and Ohtomo and. Kuroda,1993], and [Mohri, A.; et. Al,1999] requires 512, 448, 560, 500 respectively. This gives a performance gain of 2.33 over the current existing architectures. The main contribution to this performance gain is the new Sum of Four Products (SUM4P) instruction. Similarly, a total of $(92 + 16 =) 108$ cycles are required to perform 8x8 IDCT using Lee's Algorithm [i] for fast 2D IDCT. While [Kuroda,1995] [Kuroda,1995 (optimized)], [Holmann and Yamada and Yoshida and Uramoto, 1996], and [Peleg and Weiser,1996] require 704, 504, 450, and 520 instructions respectively, giving it a performance gain of more than four times over existing architectures. The main contributions to this performance gain are the Butterfly, and 128-bit Add-Sub instructions, which constitute nearly 40% of Fast IDCT computation.

The data path requires only 9 instructions/cycles to implement 3-D geometric transformation, while [Fujishima, H.; Takemoto, Y.; Onoye, T.; Shirakawa, I, 1999], [Mohri, A.; et. al,1999], and [Oberman, et. Al,1999] require 16, 16, and 13 instructions respectively. This is more than a 1.4 times increase in performance. This gain is due to the new FP Sum of Products (3D-FSMPY) instruction, which can perform two FP multiplications in parallel, thereby giving a performance gain of nearly 1.44 over the current existing architectures.

5. CONCLUSIONS

This paper presents an overview of a programmable data path to support MPEG-1, MPEG-2, and MPEG-4 standard Synthetic & Natural Hybrid video Coding (SNHC). The data path can support a maximum of 16 parallel SIMD integer operations and 2 parallel SIMD floating-point operations. The data path is reconfigurable, scalable, and area efficient and offers programmability for interactive use. In this data path, the reconfigurability is achieved by the efficient re-use of same hardware. The data path can assist in the efficient and flexible coding and representation of both natural (pixel-based) as well as synthetic (computer generated) data (SNHC) by integrating floating-point operation support with integer operations. New instructions have been developed to speed up the execution of Matrix Multiplication, Discrete

Cosine Transform (DCT), Inverse Discrete Cosine Transform (IDCT), Fast Fourier Transform, 3D-Graphics and Synthetic & Natural Hybrid Video Coding (SNHC). The data path organization and development of algorithms, combined with circuit techniques yield performance improvement in media signal processing.

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