Modeling of Time Delay in VHDL-based Design of a Multiplier

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Abstract

Top-Down design of large digital system has many advantages over the conventional bottom up approach. However, some important information about the components of the digital system at the bottom level is critical to satisfy design and timing constraints. This is especially true when physical layout procedure and post-layout simulation tools are not available. The layout of the pre-designed components, an inverter and a full-bit adder, based on the 0.5µm CMOS technology, were completed. The extraction of their capacitance parasitic and propagation delay was also done. The extracted time delay will be used in the VHDL description program of a multiplier. This approach is beneficial in the case of the absence of a technology file linked to the available design tools. Therefore, the time delay and parasitic parameters can only be estimated and not extracted from the post-layout simulation. The results of the extraction and modeling of the time delay, along with the VHDL description of the multiplier and its testing will be presented.

I. Introduction :

Time to market, rapid technology advancement, increase in chip size, and complexity of digital systems are some of the factors that led to the development of hardware description languages, (VHDL and Verilog) along with the automated logic synthesis tools. This is a departure from the conventional bottom-up design approach, stressing more the system functions without wasting time and effort on the basic components. The VHDL program describing the digital system is technology independent, but the synthesis tool that generates the circuit requires a technology file attached to it. The absence of such file causes the problem of non-possibility of time delay extraction. In this work, one of the suggested solutions, based on modeling of the time delay in the VHDL description of a multiplier circuit structure, will be presented. This requires choosing specific (CMOS) technology.

CMOS Integrated Circuits are ideally designed for high speed, low power, and minimum area. Such requirements are conflicting and the design can be optimized for only some of the above conditions. The time delay due to metal interconnects of CMOS technology is increasing as the device dimension is shrinking [1]. The inter-metal dielectric constant is being lowered to reduce the capacitance parasitic by choosing the proper material. Conventional approach, the bottom-up design starting from the transistor and the logic gate, is being replaced by the top down design as we are advancing to very large digital circuits and system-on-chip technology. VHDL is a powerful hardware description language used in the top-down design and description of the digital system under design. The time delay and the parasitic capacitance and resistance are usually extracted at later stage of the design, at the post-layout simulation. However, it is beneficial to introduce such extraction or estimation at earlier stage to reduce the number of iterations to reach the optimum solution. It is also necessary to find an alternative approach in case of the design tools don't have a technology file on which it is based the post-layout simulation extraction.

This project investigates top-down design of a multiplier. VHDL program will be used for the description and testing of the circuit. However, some of the characteristics of the components are needed in the top-down partition of those circuits. Such parameters include the gate time delay which depends on parasitic capacitances. The 0.5µm CMOS technology was chosen for the bottom up design of the multiplier components, an Adder and an And gates.

II. Modeling of time delay :

Time delay (t_d) of a digital circuit depends mainly on the load capacitance (C_L) and the driving current. C_L consists of the output capacitance of the driving gate, the input capacitance of the driven gates, and of the interconnect capacitance [2]. The driving current can be controlled by choosing the width of the P- or N-MOS transistors depending on the design constraints (area, speed, power dissipation). In this work, t_d will be extracted from layout of the gate using Cadence tool and HSpice simulation. The 0.5µm CMOS technology was attached to the Cadence tool for layout and parasitic extraction necessary for t_d calculation. Estimation of t_d of the basic components of the digital system (4x4 multiplier) can be achieved in various ways, some of which are :

* Bottom-up approach using Cadence tool for the layout, parasitic extraction, then HSpice simulation to compute t_d (this work).
* MOSFET model using HSpice circuit simulator. Such models are either available in the simulator or can be locally developed. However the interconnect capacitance [3] is often neglected resulting in an underestimation of the total load capacitance and consequently the delay time.
* Published data on some of the needed technology parameters such that the gate length, electron and hole mobility, oxide and inter-metal dielectric thickness.

* Analytical time delay models [2]

Three components (gates) with their extracted t_d will be used in the bottom up design (using Cadence) and top down design (using VHDL) of a 4x4 multiplier.

III. The CMOS inverter time delay:

The design of the CMOS inverter is mainly choosing the widths of the PMOS and the NMOS gates to reflect the different hole and electron mobility. This is to get the same electric current driving capabilities of the two transistors (PMOS and NMOS) resulting in equal turn-on and turn-off time of the inverter. W_n and W_p were chose to be 2.6µm and 6.8µm respectively, the target design constraint was minimum area. Table 1 shows the propagation time delay (t_d) of the CMOS inverter, calculated from the layout-extracted-parameters. The inverter was assumed driving a similar inverter to obtain the above time delays results. The equivalent output capacitance, driven by the inverter, and giving the same above results was found to be 50pF using HSPICE simulation.

In	Out	t_d
1	0	0.173
0	1	0.2 2

Table 1: time delay t_d, in nS, of CMOS inverter

IV. The Full-bit Ripple Carry Adder time delays :

The layout of the Ripple adder circuit [2], as shown in figure 1, was accomplished, based on the 0.5µm CMOS technology. Only metal one and two were used, metal three may be used for the optimization of the design in terms of minimum area and parasitics (by shortening the metal interconnects). Table 2 gives the propagation time delays t_d of the ripple carry adder. The input signals are (A, B, C_i), the output signals are (S, C_{out}). A load of 50pF capacitance is connected to each output. .

Table 2 : t_d, in nS, of the 1bit full adder

A	B	C_{in}	S	t_d	C_{out}	t_d
0	0	0	0	----	0	----
1	1	1	1	0.54	1	0.34
0	1	1	0	0.56	1	----
0	0	1	1	0.82	0	0.55
1	0	1	0	0.83	1	0.53
0	1	0	1	0.81	0	0.51
0	1	1	0	0.80	1	0.49

The numbers in the table represents the bits '0' and '1' except for the time delay t_d is in units of nS.

The widths of various gates were not optimized for the adder performance by increasing the gate-width where time delay is the biggest resulting in a small increase in the area. In this work, all PMOS transistors width are 6.8µm, and NMOS transistors width are 2.6 µm. However larger widths can be used, while conserving the W_p/W_n ratio, resulting in higher current and consequently shorter time delays but higher power consumption

V. The AND gate time delay :

The AND gate layout was carried using Cadence tool. The gate time delay (t_d) in units on nS, computed from Hspice simulation using the extracted parasitics from the gate layout, are given in the table 3 below. X_i and Y_i are the 1bit input signals, X_iY_i is the 1bit output with t_d is the time delay of the And gate.

Table 3 : t_d (10^{-9} S) of AND gate

X_i	Y_i	$X_i Y_i$	t_d (nS)
0	0	0	----
1	1	1	0.39
0	1	0	0.32

VI. The combined (Adder – AND) gate time delay :

The above two design, the 1-bit full adder and the AND gate were merged in one layout (needed in the design of the 4x4 multiplier). Such gate had a time delay (t_d) of the sum (S) and the carry-out (Co) bits, as shown in table 4 below. (X_i and Y_i are inputs to the AND gate. X_iY_i, S_i, and C_i are inputs to the adder, S_o and C_o are the output sum and carry-out).

Table 4 : t_d (10^{-9} S) of Adder-And gate

X_iY_i	S_i	C_i	S_o	t_d	C_o	t_d
0	0	0	0	----	0	----
1	1	1	1	0.72	1	0.53
0	1	1	0	0.92	1	----
0	0	1	1	0.85	0	0.56
1	0	1	0	1.23	1	0.91
0	1	0	1	1.13	0	0.86

VII. Bottom-up design of the multiplier:

A 4x4 Braun multiplier were designed using the bottom-up approach by butting the previously designed component [2], as shown in figure 2. Time delay (t_d in ns) of the three components were extracted from layout. The time delay is summarized in table 5. The parasitic parameters, giving rise to t_d, will be very close to those of its component if we neglect the metal interconnect between its parts. This multiplier has two 4-bits input signals (X and Y), and an 8-bits output signal ($P= XY=P_7P_6P_5P_4P_3P_2P_1P_0$)

Table 5 : Columns 3:10 are t_d (nS) of output bit P_i

X	Y	P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7
0000	0000	----	----	----	----	----	----	----	----
1111	1111	0.40	----	----	----	----	2.10	3.35	1.85
1110	1111	0.47	1.46	----	----	2.10	2.33	----	----
1100	1111	----	1.24	2.10	----	----	2.66	2.85	----
1000	1111	----	----	2.04	2.75	----	----	3.25	2.88
0000	1111	----	----	----	2.83	2.82	2.00	1.20	----
0001	1110	----	0.60	0.60	0.60	----	----	----	----
0001	1100	----	1.15	----	----	----	----	----	----
0001	1000	----	----	0.95	----	----	----	----	----

(—) means that the bit didn't change and conserved its previous value (bit 0 or bit 1).

The testing was not exhaustive and large glitches of the output signal of this 4x4 multiplier were observed.

VIII. VHDL-based design of the multiplier

A VHDL program describing the structure of the 4x4 Braun multiplier (fig. 2) was written based on three components : An (And) gate with table 2 giving its corresponding time delay, an (Adder) gate with its t_d in table 3, and a combined (Adder + And) gate with its t_d in table 4. These three componenets were also described with a VHDL program using behavior architecture. The time delay of each gate was modeled by delaying the output signal assignment by t_d depending on the current and previous values of the input signals and possibly the previous values of the output signal (carry-out signal of the adder). Such values of t_d, given in tables 2, 3, and 4 were calculated from HSpice simulations using models based on the parameters extraction from the corresponding layout of each gate (using 0.5µm CMOS technology attached to the Cadence design tool).

VHDL-based testing of the functionality and time delay of the multiplier was carried-out, table 6 gives t_d for each output bit (P_i with i=0 to 7)

Table 6 : Columns 3 to 10 are t_d (nS) of output bit P_i

X	Y	P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7
0000	0000	----	----	----	----	----	----	----	----
1111	1111	0.39	----	----	----	----	2.55	2.89	1.48
1110	1111	0.32	1.13	----	----	1.68	1.97	----	----
1100	1111	----	0.86	1.69	----	----	2.24	2.53	----
1000	1111	----	----	1.40	2.25	----	----	2.80	2.53
0000	1111	----	----	----	1.94	1.94	1.40	0.86	----
0001	1110	----	0.92	0.92	0.92	----	----	----	----
0001	1100	----	0.72	----	----	----	----	----	----
0001	1000	----	----	0.72	----	----	----	----	----

(---) means that the bit didn't change and conserved its previous value (bit '0' or bit '1').

Comparison of table 6 (VHDL-based) and table 5 (Cadence-layout-based) shows that the difference between the maximum time delay of the two approaches (2.89 ns and 3.35 ns respectively) is about 15%. This can be partly explained by the interconnect parasitic capacitance neglected in the VHDL structure description of the multiplier.

The behavioral description of the multiplier may be done to describe the multiplier entity speed performance after the modeling of the time delay using the structural description. Such unit may be stored in a library for further use in other larger digital systems.

VI. Implementation of the designed multiplier on FPGA:

The top-down design of a 4x4 Braun multiplier using VHDL structure description was implemented on Xilinx XS40-Field Programmable Gate Array (FPGA). The time delay model was not included in the component behavioral description since there is a technology file in the form of the XS4010 FPGA family attached to the Xilinx VHDL synthesis. A 4x4 Brute Force multiplier [5] was also designed for the purpose of comparison. Table 7 gives the simulation results in the form of maximum time delay (t_d) and the number of CLB used in the gate array (as a way to monitor the area) of the Braun (I) and Brute-Force (II) multipliers.

Table 7: FPGA implementation of the multiplier

	Multiplier I	Multiplier II
Number of CLBs	14 (3%)	22 (5%)
Maximum t_d	25.164 ns	28.61 ns

X. Conclusion :

It is possible to check both the functionality and time delay of VHDL-based design of a digital system even in the absence of a technology file attached to the synthesis tool. One needs only to find the time delay t_d of the basic components either analytically or by extraction from layout. HSpice models, corresponding to a specific CMOS technology, of the used transistors can also be used to estimate t_d. Interconnects between the components is usually small but can also be calculated and included in the time delay modeling.

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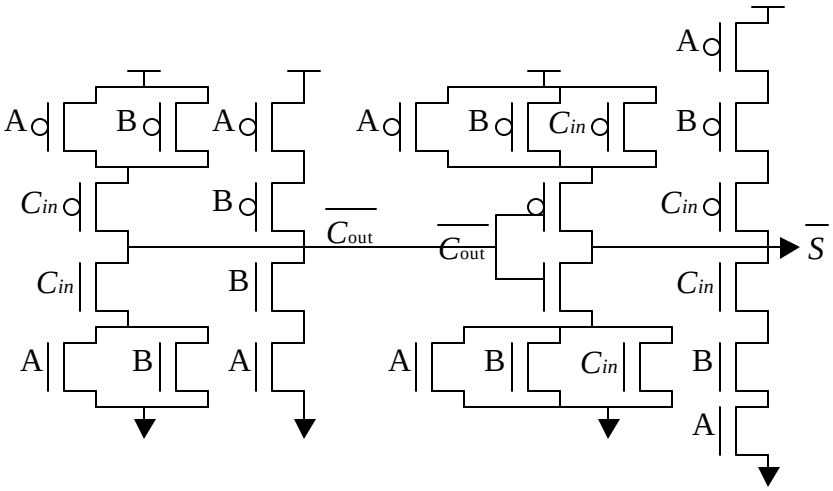

Figure 1 : 1-bit RCA Adder

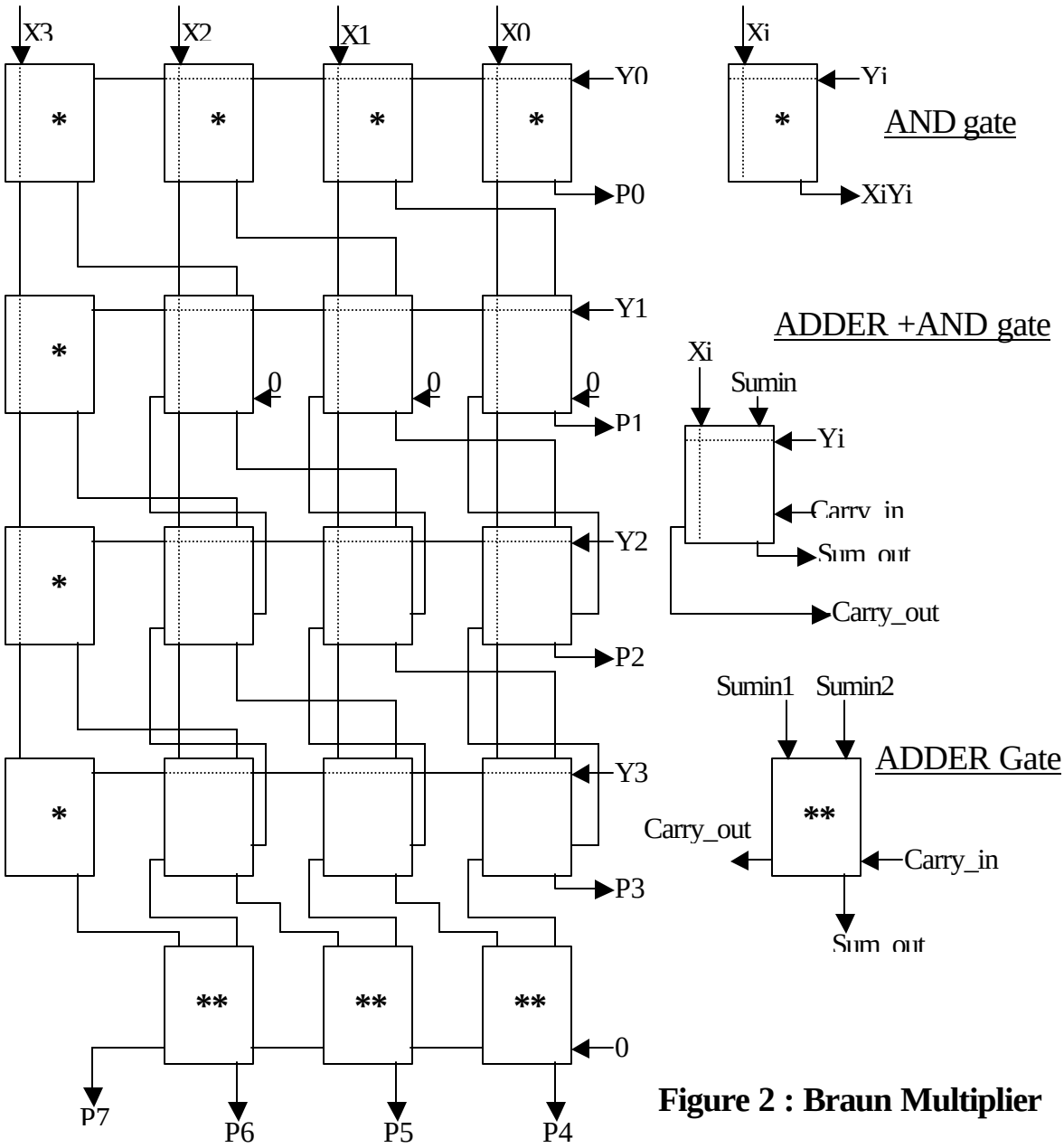

Figure 2 : Braun Multiplier