Introducing Undergraduate Students to Simulation of Semiconductor Doping Techniques.

M. Narayanan and H. Al-Nashash

Department of Electrical Engineering, American University of Sharjah, P.O.Box 26666, UAE

Abstract **__ This paper presents some of the techniques used to introduce simulation of semiconductor fabrication processes to undergraduate electrical engineering students at the American University of Sharjah. Students use Silvaco Athena process simulator and Atlas device simulator to perform experiments on semiconductor fabrication processes. Simulation results are compared with the theoretically expected results. As semiconductor process simulation tools respond to user initiated actions in real time, breaking the process at any point of time permits the visual inspection of the intermediate and final results. Therefore these tools are found to be effective in the learning process. A survey is conducted at the end of each semester to asses the ability of the students to perform semiconductor process simulation. Experience indicates that there is considerable increase in the confidence level of the students in terms of their understanding of semiconductor processes and devices.**

Index Terms **__ Semiconductor Fabrication, Education, Laboratory Experiments, Diffusion, Ion implantation**.

I. INTRODUCTION

Advances in the field of semiconductor manufacturing techniques have fueled an explosive growth in the number of microelectronics based systems developed during the past few years. The semiconductor fabrication process involves numerous elementary steps leading to the development of integrated circuits. The advances in the in the field of semiconductor fabrication techniques and shortage of skilled work force in the microelectronic industries have necessitated the need for learning microelectronics at the undergraduate level. Hence semiconductor fabrication process is an important part of the microelectronic courses of electrical engineering curriculum.

The quality of engineering courses comes from a proper combination of theoretical and practical components of the subject. The hands-on experience gained through laboratory work would equip the young graduates with the necessary skills to work in the manufacturing industries. Several universities in U.S. and other advanced countries have facilities for the fabrication of semiconductor devices. But the microfabrication process involves hundreds of steps that take weeks or months to complete which makes the learning cycle too long [1]. This is in addition to the exorbitant investment necessary to set up and maintain the state-of-the art machines and facilities required for the integrated circuit fabrication. An alternate approach which reduces the learning time and associated cost factor is the use of TCAD software which models and simulates semiconductor fabrication process.

Process simulation, device simulation and circuit simulation together are termed as TCAD or Technology Computer Aided Design [1]. Process simulation deals with structures such as atoms and their distribution, device simulation deals with currents and potentials in the devices and circuit simulation is used to study larger circuit blocks [1]. Circuit simulation is the most advanced and process simulation is the least developed of the three kinds of simulation. These simulators realistically reflect the time-dependant behavior of the processes and devices.

Electrical engineering students at the American University of Sharjah learn about semiconductor devices, fabrication techniques and device characteristics at the sophomore and junior year levels. Students conduct experiments on semiconductor fabrication processes and devices with simulation tools. Process steps like oxidation, diffusion and ion-implantation are simulated along with testing the electrical characteristics of the simulated devices. At AUS Silvaco tools are used for process and device simulation. Athena provides an easy to use platform to simulate fabrication processes while Atlas is used to simulate the electrical behavior of the semiconductor device under study. The software can respond to user initiated actions in real time, break the program (Process) at any point of time and visually inspect the intermediate results.

Students perform simulation experiments on oxidation, diffusion and ion-implantation and verify the results under different processing conditions. The results are then compared with the expected values. Students also fabricate a semiconductor pn junction and simulate the forward and reverse characteristics of the fabricated device. In this paper we will discuss the doping techniques used for semiconductor manufacturing process namely diffusion and ion implantation process.

II. DIFFUSION TECHNIQUES FOR SEMICONDUCTOR DOPING.

II.A THEORY.

Diffusion is the physical phenomenon where materials move from high concentration regions to low concentration regions driven by thermal motion of the

molecules. During this process particles confined to the same volume tend to spread out and redistribute themselves evenly throughout the confining volume. It occurs at all temperatures, but the diffusivity has an exponential dependence on temperature. Diffusion can be used for doping semiconductors. When high concentration of dopant is introduced on the surface of the silicon at high temperature, dopant diffuses in to the silicon substrate.

During diffusion process particles tend to diffuse from a region of high concentration to lower concentration at a rate proportional to concentration gradient between the two regions [2].

$$F_{diff} = -D\frac{dN}{dx} m^{-2}s^{-1} \qquad (1)$$

F_{diff} is the net particle flex density.
N is the number of particles per unit volume and
x is the distance measured parallel to the direction of flow.
D is the diffusion coefficient and has units of (Length)^2 / Time. Negative sign indicates that the flow is from high concentration region to low concentration region. Fig. 1 below shows the diffusion coefficients of various dopants in silicon as a function of temperature.

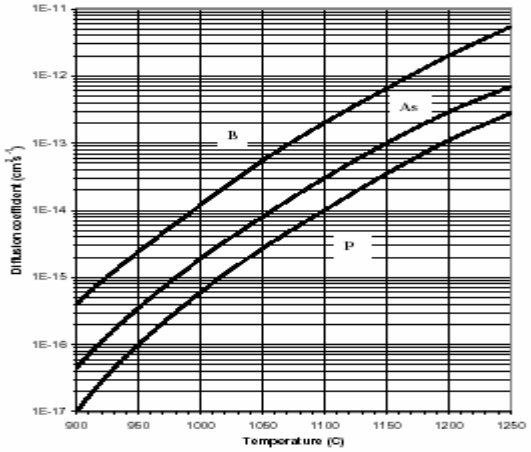

Fig.1. Diffusion coefficients of commonly used dopants.

The maximum concentration of dopant that can be dissolved in silicon under equilibrium condition without forming a separate phase is termed as solid solubility [4]. This is indicated in Fig. 2. Above solid solubility a separate phase forms.

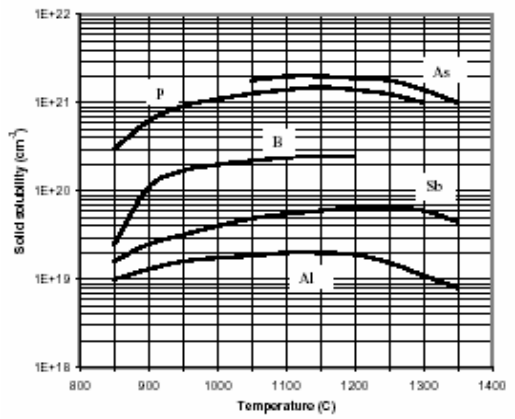

Fig.2. The solid solubility and impurity–concentration limits in silicon.

Diffusion is carried out in two phases. Step 1 is called Predeposition and step 2 is called Drive-in diffusion. Doping often proceeds by an initial pre-deposition step to introduce the required dose of dopant into the substrate. A subsequent drive-in diffusion redistributes the dopant giving the required junction depth and surface concentration. Fig.3 indicates the diffusion steps and progress during the diffusion process.

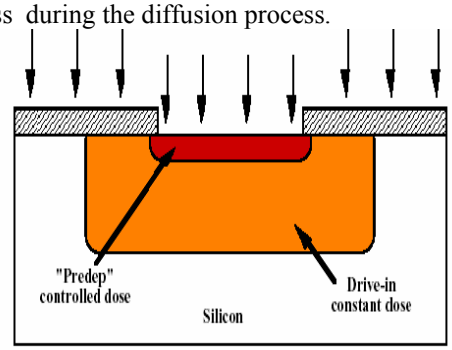

Fig.3. Illustration of pre-deposition and drive-in diffusion steps.

During predeposition the wafer is exposed to the impurity source during the entire duration of the diffusion [3]. There is an undiminished supply of impurities at the wafer surface. The impurity concentration at the wafer surface is kept constant as set by the solid solubility of the particular dopant in silicon. Predeposition is controlled by several factors. One is the diffusivity of the particular dopant. Another factor is the maximum solid solubility limit of the dopant in the wafer material. During diffusion, the density of impurity atoms (Atoms/ cm^3) at a distance "x" from the diffusion

surface at a time "t" after the start of diffusion is given[5] by

$$N(x,t) = N_0 Erfc(\frac{x}{2\sqrt{Dt}}) \qquad (2)$$

N_0 is the surface concentration in atoms/cm^3,
t is the diffusion time for pre-deposition.
x is the diffusion depth in to the substrate (cm.)
D is the diffusion coefficient (cm^2/s), given by the relationship

$$D = D_0 e^{\left(\frac{-E_D}{kT}\right)} \qquad (3)$$

D_0 is a temperature independent term that depends on the vibrational frequency and geometry of the lattice.

E_D is the activation energy,
k is Bolzmann's constant, and
T is the temperature in Kelvin.

The dose of pre-deposition diffusion varies with the time of diffusion. The dose [2] is obtained as

$$Q = \int_0^\infty N(x,t)dx = 2N_0\sqrt{Dt/\pi} \qquad (4)$$

Dose specifies the total number of dopant atoms per unit area of the semiconductor.
N_0 is the surface concentration in atoms/cm^3,
D is the diffusion coefficient and
t is the diffusion time.

The depth of the predeposition profile is usually less than 1 µm. So a dose of 10^{15} cm^{-2} will produce a large volume concentration (> 10^{19} cm^{-3}).

After the pre-deposition stage, the wafer is subjected to drive-in diffusion. After pre-deposition the impurity source is turned off. The mathematical expression for the concentration of dopant atoms during drive-in diffusion is given as

$$C(x,t) = \frac{Q}{\sqrt{\pi Dt}} \exp\left(-\frac{x^2}{4Dt}\right) \qquad (5)$$

Where Q (atoms/ cm^2) is the initial concentration of impurity atoms deposited on the surface during the pre-deposition step.

II.B SIMULATION.

Using Athena program students initialize a silicon wafer of the size 2 µm. X 5 µm. Following the common practice followed in the semiconductor process labs time and temperature variables are selected. Predeposition diffusion is carried out at 900^{0}C for 15 minutes using boron as dopant and drive-in diffusion is carried out for 5 hours at 1100^{0}C. The results of the simulation for predeposition is given in Fig. 4 as concentration of boron atoms/cm^3 Vs the distance from the surface. The simulation results for drive-in diffusion is given in Fig.5.

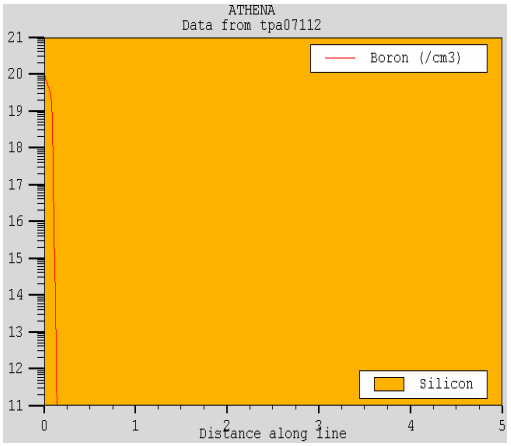

Fig.4. Results of Athena simulation of Predeposition diffusion at 900^{0}C for 15 minutes.

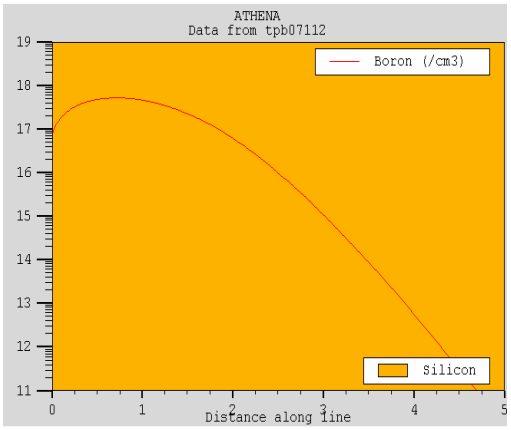

Fig.5. Results of Athena simulation of Drive-in diffusion at 1100^{0}C for 5 hours.

The concentration of born from simulation result at a depth of 1 µm. is 5.1*10^{17} boron atoms/ cm^3. Expected concentration of boron atoms as calculated with equations (4) and (5) is 5.7*10^{17} boron atoms/ cm^3.

III. ION IMPLANTATION FOR SEMICONDUCTOR DOPING.

III.A THEORY.

Ion implantation is the method of choice in state of the art semiconductor manufacturing to bring the dopants into the substrate material, mainly due to its ability to accurately control the number of implanted dopants. During the ion implantation process ionized atoms are accelerated in an electric field and the beam is directed towards the substrate material. When entering the substrate material the energy of the dopant atoms decrease while they interact with the target material. After some time the atoms come rest at some depth depending on their initial energy. Dopant concentration at a desired depth can be controlled by the combination of ion beam current and implantation time and the junction depth can be controlled by the ion energy.

The impurity profile resulting from ion implantation has a Gaussian distribution with the peak of the distribution appearing below the surface of the silicon wafer. The peak of the distribution increases with increasing mass and energy of the incident ions. The total distance that an ion travels before coming to rest is called it's range. The projection of this distance along the axis of incidence is called the Projection Range Rp.

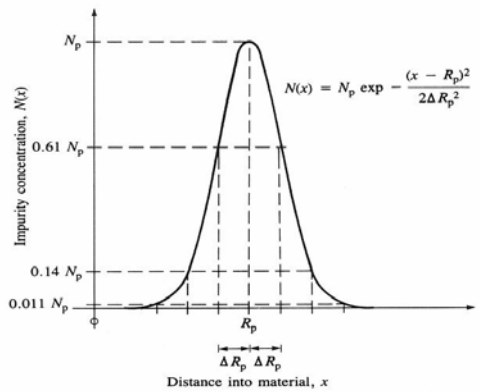

Fig.6. Gaussian distribution resulting from ion implantation.

$$N(x) = \frac{Q_{dose}}{(2\pi)^{0.5}\Delta R_p}\exp[-\frac{(x-R_p)^2}{2\Delta R_p^{\ 2}}] \qquad (6)$$

The impurity concentration as a function of depth x in a solid [2] is given by equation 6.

Rp is the projected range

ΔRp is the standard deviation of the projected range.

Q_{dose} is the dose per unit area.

The above expression gives the concentration of the ions at a distance *x* from the surface of the specimen. Typical ion energies used in ion implantation processes is in the range of 10 keV to 500 keV and ion dose is in the range of $1*10^{10}$ atoms/ cm^2 to $1*10^{18}$ atoms/ cm^2.

III.B SIMULATION.

Using Athena program students initialize a silicon wafer of the size 2 µm. X 2 µm. Ion implantation is carried out with a dose of $1*10^{13}$ phosphorus atoms per cm^2. After setting the ion beam energy to 200 keV, ion implantation is carried out. The results of simulation is indicated below.

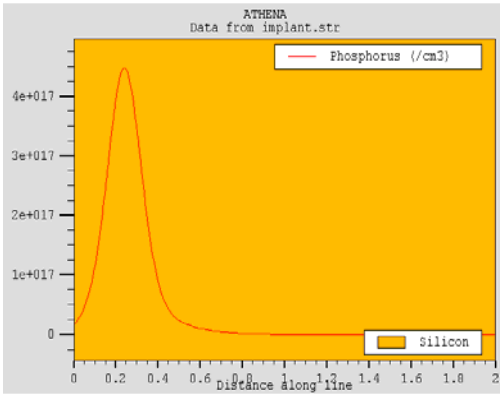

Fig.7. Results of Athena simulation of ion implantation

The simulation results of the ion implantation as concentration of phosphorus atoms/cm^3 Vs the distance from the surface is indicated in Fig. 7. The concentration of phosphorus atoms from simulation results at a depth of 0.3 µm is found to be $3.4*10^{17}$ boron atoms/ cm^3. The expected concentration of phosphorus atoms as calculated with equation (6) is $3.53*10^{17}$ phosphorus atoms/ cm^3.

IV. ASSESSMENT RESULTS

A survey was conducted among the students to identify the learning outcome on the semiconductor fabrication processes. One of the questions in the questionnaire is to indicate whether the student can simulate semiconductor device fabrication processes. Students give their response by choosing numbers. In TABLE 1 number 1 represents agreement, 3 represents disagreement and 2 indicates neutral. Feedback collected over the last four semesters is indicated in Table 1.

TABLE 1
Students feedback on learning outcomes.

1. Agree. 2. Neither agree nor disagree. 3. Disagree				
Semester	Number of students	1	2	3
Spring 2005-1	15	6	6	3
Spring 2005-2	15	9	2	4
Fall 2005 -1	18	13	4	1
Fall 2005 -2	15	8	3	4
Spring 2006-1	19	10	5	4
Spring 2006-2	17	10	3	4
Fall 2006 -1	19	7	6	6
Fall 2006 -2	19	6	8	5
Total	137	69	37	31
		50%	27%	23%

Survey average results shown in Fig.8 indicates that 50% of the surveyed students agreed that they can simulate semiconductor device fabrication processes, 27% were neutral and 23% disagreed on whether they can simulate semiconductor device fabrication processes.

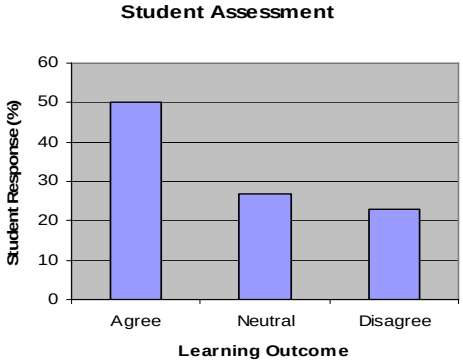

Fig.8. Learning outcome chart

V. CONCLUSION

Semiconductor device processing involves several complex stages. In order to understand the concepts well, one should be able to verify the results obtained during individual steps. A large number of university students are deprived off the opportunity to get a feel of the semiconductor fabrication processes because of the practical difficulties associated with the setting up of fab labs. Teaching semiconductor processes and devices with simulation tools is an effective and cost effective method. With simulation tools, students take a more active role in learning complex fabrication processes and therefore understand the techniques in depth. Our experience with TCAD tools proved that it is a powerful tool for understanding semiconductor fabrication processes and also for learning and training purposes. Dynamic semiconductor process simulators are therefore strongly recommended for electrical engineering students in order to complement their basic understanding on semiconductor processes.

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