FAST DIRECT DIGITAL SYNTHESIZER

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***Abstract* — The frequency synthesizer is the heart of any frequency hopping system. Recently, the direct digital synthesizer is considered as one of the most important type due to the high resolution capability. The switching time of the conventional direct digital is mainly depending on the number of bits of the accumulator and the main clock of the reference frequency. In this paper, a proposed direct digital synthesizer is designed to reduce the time needed to change the required frequency. Computer simulation tests are used to examine the proposed system. The results of these tests show that the switching time is equal to the time interval of the main clock frequency.**

***Index Terms* — Industrial electronics, Modulation, Mobile communication, Power amplifier, Spread spectrum systems.**

I. INTRODUCTION

The frequency hopping system is one of the spread spectrum techniques, where the carrier frequency is rapidly changed (or hopped) to a new frequency. The goal of this technique is to reduce the ability of locking onto the communication link. Therefore, it is important to introduce a significant design issue-building hardware that can generate a fast hopped carrier signal. Historically, this can be accomplished by reducing the switching time of the main part of the frequency hopping system, which is called frequency synthesizer. The frequency synthesizer is defined as a system that generates one or more frequencies derived from a single reference oscillator [1]. The direct digital synthesizer is a type of frequency synthesizers, which can be practically described as a means of generating highly accurate and harmonically pure digital representation of signals. The simplified form of the conventional direct digital synthesizer is shown in Fig.1.

The first component of the direct digital synthesizer is the phase accumulator. The phase accumulator consists of frequency register, full adder and a phase register. To make the output of the accumulator useful, it must be converted from phase information into a sinusoidal value (amplitude information) using a look-up table (LUT). The digital signal is then reconstructed with high speed digital to analog converter (DAC) to provide an analog output signal. Finally, the low pass filter is used to remove the unwanted parts of the required signal [2, 3]. At each clock, the digital input phase increment word (Δp) is added to the data previously held in the phase accumulator to produce a linearly increasing digital value. The phase increment word represents a phase angle step, which rotates through a fixed angle for each unit of time (Δt) [4].

$$\Delta p = \omega \Delta t \tag{1}$$

where Δt is the time interval of one cycle of the clock frequency (f_{clock}). Then solving (1) for ω;

$$\omega = \Delta p . f_{clock} \tag{2}$$

The synthesizer output frequency may be represented by;

$$f_{out} = \frac{\Delta p . f_{clock}}{2\pi} \tag{3}$$

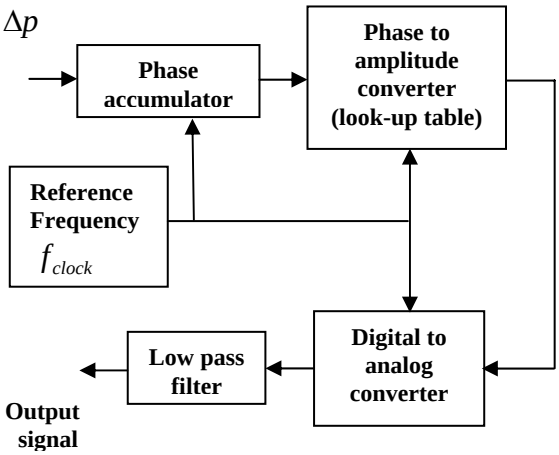

Fig.1 Conventional direct digital synthesizer.

Continuous time functions have phase range of 0 to 2π. Outside this range of numbers, the functions repeat themselves in a periodic manner. The accumulator of the direct digital synthesizer is implemented with n bits. Therefore, 2π is equivalent to the number of 2^n. Then [5, 6];

$$f_{out} = \frac{\Delta p . f_{clock}}{2^n} \tag{4}$$

As clearly appears in (4), the maximum generated frequency of the direct digital synthesizer is one half of the reference frequency.

II. PROPOSED SYSTEM

The switching time (T_{sw}) of the conventional direct digital synthesizer may be represented by [7, 8];

$$T_{sw} = (n-1)T_{CLOCK} \qquad (5)$$

where T_{clock} the duration of the clock frequency and n is the number of bits of the synthesizer. From the above equation, it is clear that the time required to switch the output frequency from one value to another is mainly depend on the number of bits of the accumulator. The idea behind the suggestion of the proposed system is to replace the phase accumulator by so called the direct phase generator (Fig.2).

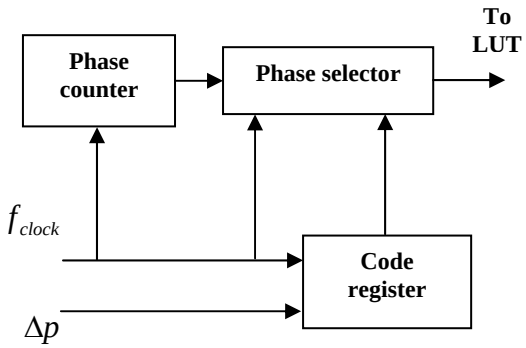

Fig.2. Direct phase generator.

As shown in Fig.2, the direct phase generator consists of phase counter, phase selector and code register. The number of bits of the phase counter determines the number of the resulted signal frequencies. Since the phase counter cannot complete the bits propagation in a short single clock, a pipelined circuit is used. This circuit is located behind the phase counter and it consists of five arms, each one is delayed with clock period as compared with the next one. As a result, the total number of delay elements for such synthesizer is equal to ten elements [8]. The phase selector is a digital control circuit, which selects the sequence coming from the phase counter to produce a signal with the required frequency. During the period of transmission, the phase increment word is saved using the code register, which is a parallel in parallel out shift register.

In the proposed system and for a certain value of phase increment word, there is a corresponding connection of the phase selector. To generate the first frequency for example, (Δp=1), the output bits of the phase counter are directly connected to the input bits of the look-up table. The second frequency (Δp=2) is generated by connecting the first bit of the phase counter to the second input bit of the look-up table and the second bit of the phase counter to the third bit of the look-up table and so on. The first input bit to the look-up table is set to logic "1". The generation of the third frequency (Δp=4) is summarized by connecting the first bit of the phase counter to the third input bit of the look-up table and the second bit of the phase counter to the fourth bit entered to the look-up table and so on, while the first two bits of the look-up table are forced to have the value of logic "1". The operation of the phase selector may be more explained using the following two cases:-

A. First Case

For a phase increment word of one ($\Delta p = 1$), the contents of the code register is (10000)and the phase counter output bits a, b, c, d and e will transferred directly to the output of the phase selector bits 1, 2, 3, 4 and 5 respectively as shown in Fig.3. Therefore, at each clock, the phase selector transfers all the outputs of the counter to the look-up. The duration of the resulted signal is equal to 2^m. The parameter m represents the number of bits of the phase counter. Therefore, the time of the resulted signal is 32 times the main clock interval.

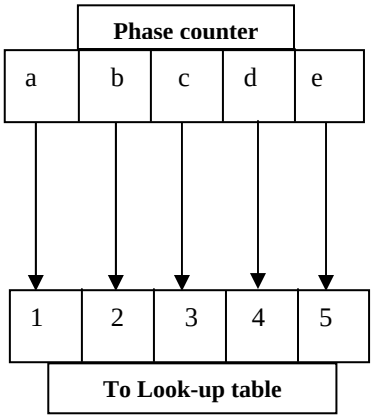

Fig.3. Operation of the phase selector with Δp=1.

B. Second Case

For Δp=2 (01000), the operation of the direct phase generator is summarized by taking bit number 1 to have logic "1" and the data of phase counter bits a, b, c and d are transferred to look-up table input bits 2, 3, 4 and 5 respectively as shown in Fig.4. So the time of the resulted signal is 16 times of the clock time as a result of using four bits of the phase counter. For other values of phase increment word, the operation of the phase selector is changed simultaneously, and according to that, the synthesizer produces the required signal with a time interval proportional to the value saved in the code register.

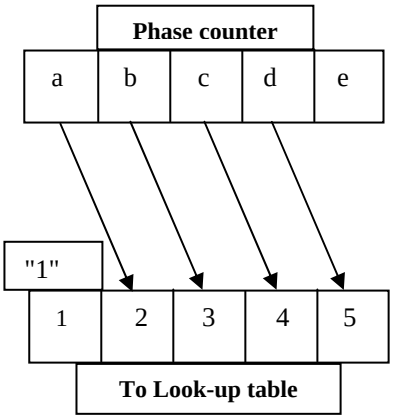

Fig.4 Operation of the phase selector with Δp =2.

III. Computer Simulation Tests

Computer simulation tests have been carried out to show the performance of the proposed system as compared with the conventional direct digital synthesizers. In these tests, the clock frequency is assumed to be equal to 250 MHz, the number of bits is five and so the possible output frequencies related to the phase increment word Δp are as shown in table 1.

TABLE 1
POSSIBLE OUTPUT FREQUENCIES

Phase increment word Δp	Output frequency (MHz)
1	7.8125
2	15.625
4	31.25
8	62.5
16	125

The time waveforms of the conventional and the proposed direct digital synthesizers are shown in Fig.5 and Fig.6 respectively. In each of these two figures, there are three time waveforms. The upper waveform represents the signal at the output of the look-up table, the second waveform represents the signal before the low pass filter and the lower waveform represents the required output signal. It is assumed that the frequency of the output signals is 7.8125 MHz during the time t_1, 15.625MHz during t_2 and 31.25 MHz during t_3. As clearly appears in Fig.5 (upper waveform), the time needed to change the frequency from the first value to the second is started at the white line and it needs four clock durations (16 nsec).

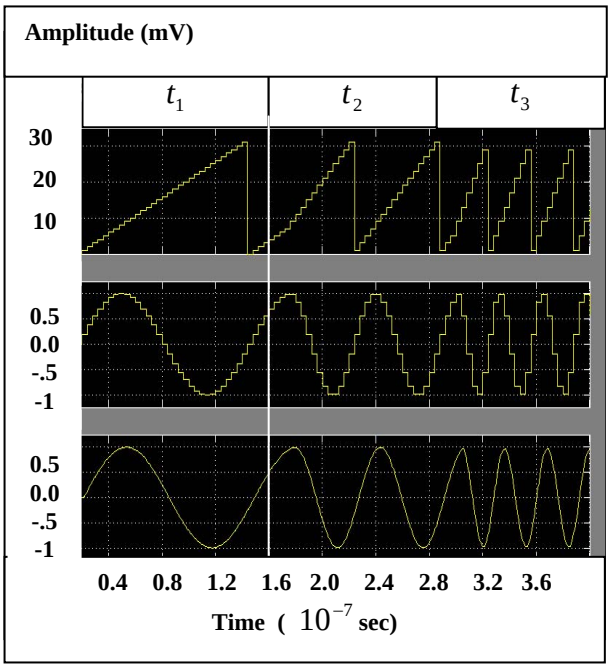

Fig.5 Time waveforms of the conventional DDS.

The simulated switching time is identical to that may be obtained using (5) by taking n=5 and T_{clock} = 4 nsec (clock frequency equals to 250 MHz), so the switching time is 16 nsec.

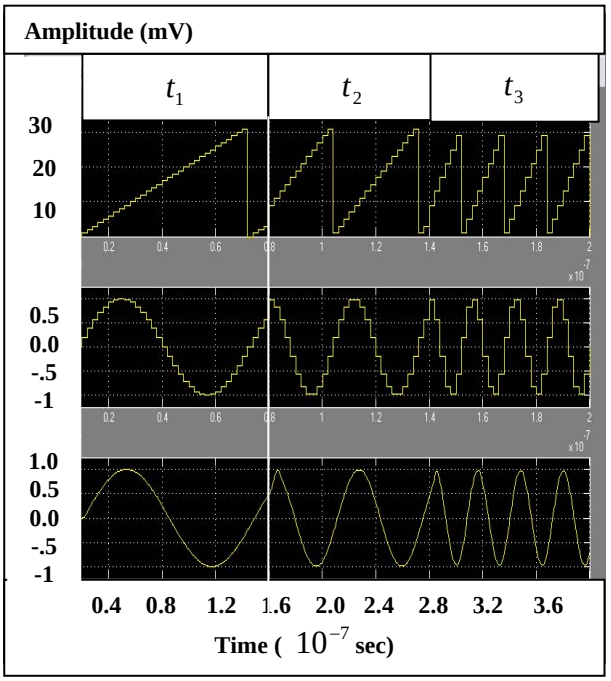

Fig.6 Time waveforms of the proposed DDS.

Fig.6 shows that the switching time for the proposed direct digital synthesizer is reduced to one clock duration. As a result, this time is equal to 4 nsec (for 250 MHz reference frequency).

IV. Conclusion

It is important to reduce the time required to change the frequency of the synthesizer output signal which improve, for example, the hop rate of the frequency hopping systems. However, the resolution of the conventional DDS is directly proportional to the number of bits of the synthesizer, but this leads to increase the synthesizer switching time. The tests used to examine the system suggested in this paper show that the switching time is independent on the number of the bits of the synthesizer. Therefore, the resolution improvement of the proposed system has no effect on the time required to change the synthesizer frequency. To reduce the expected complexity of the proposed direct digital synthesizer, the system may be implemented using Field Programmable Gate Array technology due to the ability for such technology to operate as a single chip and the fact that can be tailored to meet the requirement of a specific operation.

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