MicroPhotonic Components for Optical Packet-Switched Networks

Muhsen Aljada[1], ChungKiak Poh[1], Kamal Alameh[1], and Khalid Al-Begain[2]

[1]Electron Science Research Institute, Edith Cowan University, Australia.

[2]Communications and Networking Research Group, University of Glamorgan, UK.

***ABSTRACT* — The implementation of packet switched optical network architectures bring forth a set of new challenges in network node design. This paper discusses and demonstrates promising MicroPhotonic architectures that perform optical header recognition and reconfigurable add/drop multiplexing for future optical networks.**

***Index Terms*—Wavelength Division Multiplexing, Optical Header Recognition, Add-Drop Multiplexing, Optical Networks**.

I. INTRODUCTION

Telecommunication traffic is expected to grow dramatically in the next years, as a consequence of the offer of new diffusive and interactive services [1]. Fiber-optic technology is promising technology for its potentially limitless capabilities [2], huge bandwidth [nearly 50 terabits per second (Tb/s)], low signal attenuation (as low as 0.2 dB/km), low power requirement, small volume, and low cost [3] [4]. To handle the exponential growth of Internet traffic, future all-optical networks need to provide packet routing at terabits rates. Packet switched optical networks, in particular, have attractive features that allow routing and data switching without necessitating the interpretation or regression of signals within the network [5]. However, several challenges are still restricting packet switched optical networks from fully utilizing the available advantages in the photonic technology, namely:

- A practical optical packet switch should route packets from the switch input to the output using simple routing procedures. Currently optical data packets are converted from the optical domain to the electrical domain to process their headers and make routing decisions which is consider the bottleneck for future high-speed optical network [6]. Therefore, interference-free, fast, all-optical header recognition is still needed.
- The foreseeable transport capacity will require sufficient technique capable of supporting high bit rates. Combining wavelength division multiplexing (WDM) transmission [7] together with fast photonic switching [8-10] leads to high throughputs and more flexibility, allowing dynamic bandwidth sharing between different users through the use of reconfigurable optical add/drop multiplexers (ROADM's), which allow the WDM channels to be added, dropped, or bypassed without the need for optical-electrical-optical conversion. Therefore, ROADMs are needed to build an agile optical network.

In this paper, we present two promising Microphotonic architectures for optical header recognition and reconfigurable optical add drop multiplexing. In Section II, we demonstrate a MicroPhotonic structure for optical packet header recognition based on the integration of an optical cavity, optical components and a photoreceiver array. The structure is inherently immune to optical interference thereby routing an optical header within optical cavities to different photo receiver elements to generate the autocorrelation function, and hence the recognition, of the header using simple microelectronic circuits. In Section III, we present and experimentally demonstrate a MicroPhotonic architecture based on a reflective, free-space Opto-VLSI processor which generates reconfigurable holographic diffraction gratings to steer optical beams incident onto its surface, thus performing Reconfigurable Optical Add/Drop Multiplexing (ROADM). Experimental results are also presented, which demonstrate a 5-channel ROADM.

II. ALL-OPTICAL HEADER RECOGNITION

A conceptual diagram of optical header recognition is illustrated in Fig. 1. The stream of information from source to destination usually consists of small packets. The packet is comprised of the header (which has all routing information processed only by the switch) and the payload (the body of the packet/information processed only by the source and destination). The header and the payload can be transmitted within the same packet or parallel on separate channels within the same fiber. An optical tap is used to by-pass a small power of the optical packets. This small power is then split into M outputs using the 1xM optical splitter. At the output ports of the optical splitter, an array of optical correlators is used. Through correlation, an

incoming header pattern can be recognized by matching it with predetermined pattern. If both patterns are similar, the correlation function a symmetrical waveform that exhibits very-high amplitude at its axis of symmetry. Using the comparators, the electrical signals at the output ports of the M optical correlators are converted into control signals fed into the control ports of the N-port optical switch that routes the packet to its next hop.

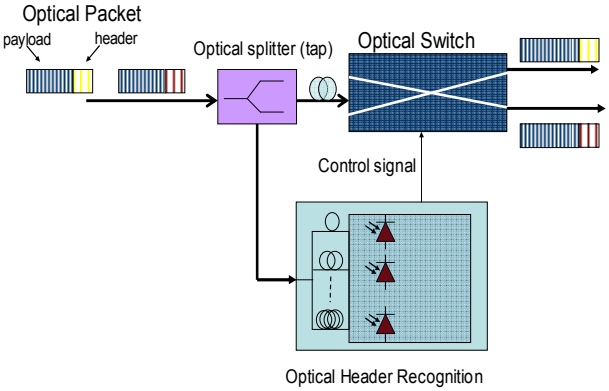

Fig.1. Conceptual of optical header recognition

Fig.2 schematically illustrates the MicroPhotonic correlator for optical header recognition [11] [12]. The small power of the optical packet, which consists of the optical payload and the optical header, is by-passed from the optical fiber using the optical tap (about 10% is tapped). The 1×N optical splitter equally splits the tapped optical packet into N packets. The microlenses are appropriately etched into the optical substrate in order to convert the in-fiber optical packets into collimated optical beams. Each collimated optical beam propagates within the optical substrate and undergoes several reflections in a cavity whose width defined by the mirror and the diffractive optical element (DOE). Every time a beam hits the DOE, a small fraction of the power of that beam is transmitted through the DOE for detection and amplification by an element of the wideband photoreceiver array that is integrated on the surface of the optical substrate, while the remaining large fraction is reflected and routed to for subsequent delayed photodetection. The gain of a photoreceiver can be set to a low value (0) or a high value (1). The gains of each row of photoreceivers are set to recognize a specific header pattern and the gain configuration of the entire rows will act like the look-up table. Each element of the combiner/comparator array adds the amplified photocurrents of a photoreceiver row, generates an output signal depends on the photoreceiver gain configuration, and then sent to a threshold detector. The output control signals are fed into the control ports of the N-port optical switch (not shown in Fig.2) that routes the packet to its next hop.

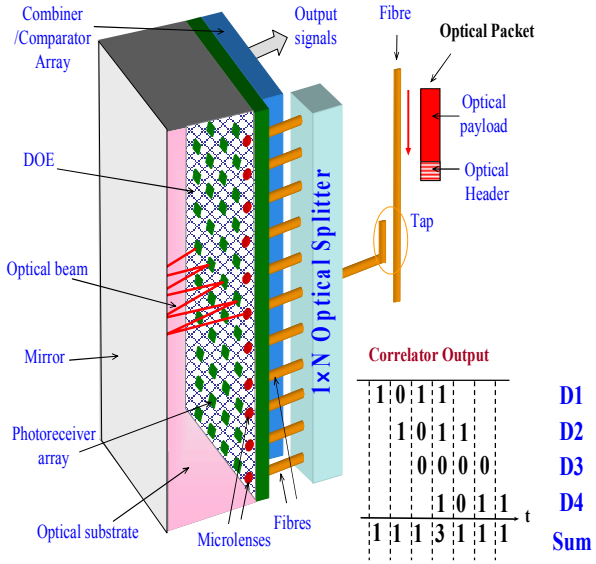

Fig. 2. MicroPhotonic correlator architecture.

III. RECONFIGURABLE OPTICAL ADD-DROP MULTIPLEXING

WDM technology is being deployed by several telecommunication companies for point-to-point communications. This deployment is being driven by the increasing demands on communication bandwidth. When the demand exceeds the capacity in existing fibers, WDM is turning out to be a more cost-effective alternative compared to laying more fibers [4]. OADM (optical add/drop multiplex) nodes are key elements of such systems, assuring network survivability by fast reconfiguration and enabling add/drop of WDM channels. Optical add-drop multiplexers (OADM) are fundamental devices for the operation of multi-node optical WDM networks. It selectively removes (drops) a wavelength from a multiplicity of wavelengths in a fiber, and thus from traffic on the particular channel. It then adds in the same direction of data flow of the same wavelength, but with different data content as shown in Fig.3.

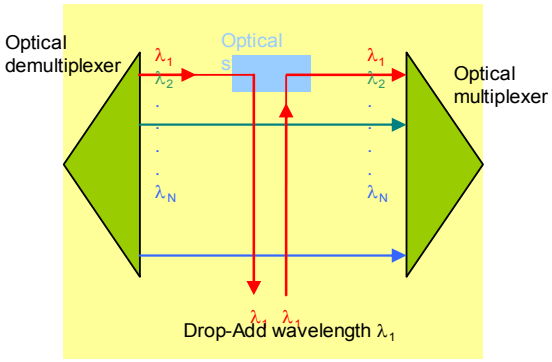

Fig. 3. Generic optical add-drop multiplexer.

IV.OPTO-VLSI PROCESSING

A reconfigurable Opto-VLSI processor comprises an array of liquid crystal (LC) cells driven by a Very-Large-Scale-Integrated (VLSI) circuit that generates digital holographic diffraction gratings to steer and/or shape optical beams [13], as illustrated in Fig. 4.

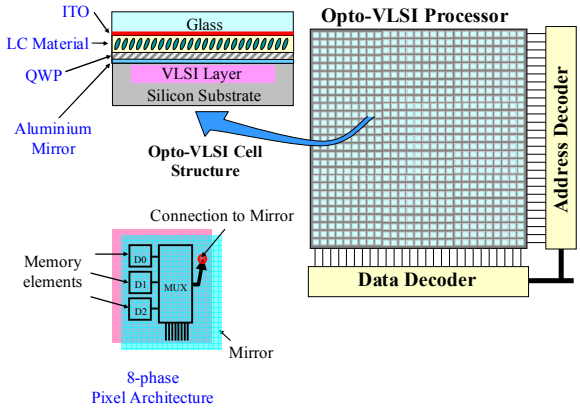

Fig. 4. Typical 8-phase Opto-VLSI processor and LC cell structure design.

Each pixel is assigned a few memory elements that store a digital value, and a multiplexer that selects one of the input voltages and applies it to the aluminum mirror plate. Opto-VLSI processors are electronically controlled, software-configured, polarization independent, cost effective because of the high-volume manufacturing capability of VLSI chips as well as the capability of controlling multiple fiber ports in one compact Opto-VLSI module, and very reliable since beam steering is achieved with no mechanically moving parts. Fig. 4 also shows a typical layout and a cell design of an 8-phase Opto-VLSI processor. Indium-Tin Oxide (ITO) is used as the transparent electrode, and evaporated aluminium is used as the reflective electrode. The ITO layer is generally grounded and a voltage is applied at the reflective electrode by the VLSI circuit below the LC layer. Fig. 5 illustrates the steering capability of Opto-VLSI processors.

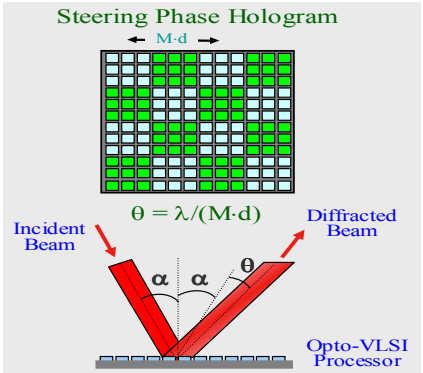

Fig. 5. Steering capability of an Opto-VLSI processor.

For a small incidence angle, the maximum steering angle of the Opto-VLSI processor is given by

$$\theta_{\max} = \frac{\lambda}{M \cdot d} \qquad (1)$$

where M is the number of phase levels, d is the pixel size, and λ is the wavelength. For example, a 4-phase Opto-VLSI processor having a pixel size of 5 microns can steer a 1550 nm laser beam by a maximum angle of around ±4°. The maximum diffraction efficiency of an Opto-VLSI processor depends on the number of discrete phase levels that the VLSI can accommodate. The theoretical maximum diffraction efficiency is given by [14]

$$\eta = \mathrm{sinc}^2\left(\frac{\pi n}{M}\right) \qquad (2)$$

where $n = gM + 1$ is the diffraction order ($n = 1$ is the desired order), and g is an integer. Thus an Opto-VLSI processor with binary phase levels can have a maximum diffraction efficiency of 40.5%, while a four phase levels allow for efficiency up to 81%. The higher diffraction orders (which correspond to the cases g ≠ 0) are usually unwanted crosstalk, which must be attenuated or properly routed outside the output ports to maintain a high signal-to-crosstalk performance.

Adaptive optical beam steering can be achieved by reconfiguring the phase hologram uploaded onto the Opto-VLSI processor. Recent advances in low-switching-voltage nematic LC materials and Layer thickness control have allowed the incorporation of a thin quarter-wave-plate (QWP) layer between the LC and the aluminum mirror to accomplish polarization-insensitive multi-phase-level Opto-VLSI processors [15], as shown in Fig. 5. In addition, with current 130nm VLSI fabrication processes, VLSI chips featuring 24mm×24mm active area, maximum switching voltage of 3.0 volts, and pixel size of 5 microns, can be realised. Depositing low-switching-voltage electro-optic materials and QWP over such VLSI chips, can realize a polarization-insensitive Opto-VLSI processor that has a diffraction efficiency of 87% (0.6 dB loss) and a maximum steering angle of more than ±4.0° [15].

There are several algorithms for the optimization of Opto-VLSI holograms to achieve effective beam steering, including simulated annealing and projection methods. In our study, a modified simulated annealing method that can achieve accurate beam steering with low crosstalk is adopted [16].

V. OPTO-VLSI BASED ROADM

Reconfigurability is a desirable attribute in an OADM. It refers to the ability to select the desired wavelengths

to be dropped or added as wishes, as opposed to having to plan ahead and deploy appropriate equipment. This allows carriers to be flexible when planning their network and allows light paths to be set up or taken down dynamically as needed in the network. A promising candidate that can potentially realize ROADM is Opto-VLSI processor. A schematic setup to realize ROADM using Opto-VLSI processor is as shown in Fig. 6. The multiplexed wavelengths enter the ROADM system via the 'input' of the THRU-port. In this case, the multiplexed wavelengths consist of λ_1, λ_2, and λ_3. The multiplexed wavelengths are directed at a dispersive grating after passing through circulator-1, C1. This causes different wavelengths to incident on different region on the Opto-VLSI active window. Depending on the hologram loaded into the Opto-VLSI processor, each wavelength can either be steered back to the THRU-port, or directed to the DROP-port for Drop-operation. As an illustrative example here, λ_1 is steered to the DROP-port. Alternatively, a same wavelength but carrying different data content λ_1' can be added to the original multiplexed signal.

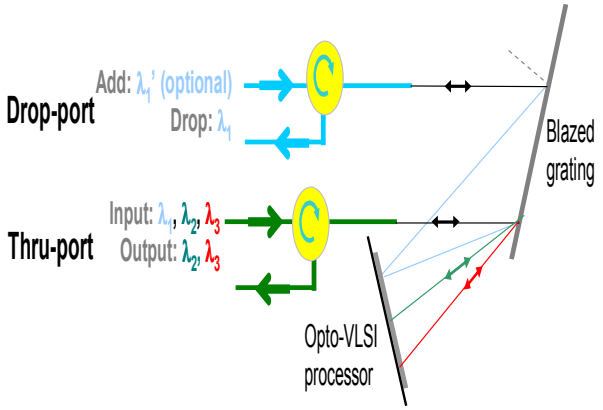

Fig. 6. Experimental setup for the Reconfigurable OADM.

VI. EXPERIMENTAL RESULTS

In this Section, we demonstrate a 5-channel ROADM by showing the measured output spectra at the THRU and DROP ports for different add/drop scenarios. Fig. 7(a) shows the phase hologram that couples all the WDM channels into the THRU port (no dropped channels). Figs. 7(b) and (c) shows the measured output optical spectra at the THRU and DROP ports of the 5-channel ROADM. WDM channels at 1545nm, 1550nm, 1555nm, 1560nm and 1565nm were used. The input signal power per channel was +4dBm and the loss of the grating plate was 2dB at 1550nm. The Opto-VLSI processor used in the experiments had low reflectivity and low fill factor resulting in a measured loss of around 6dB. The measured two-way fiber coupling losses were around 2dB.

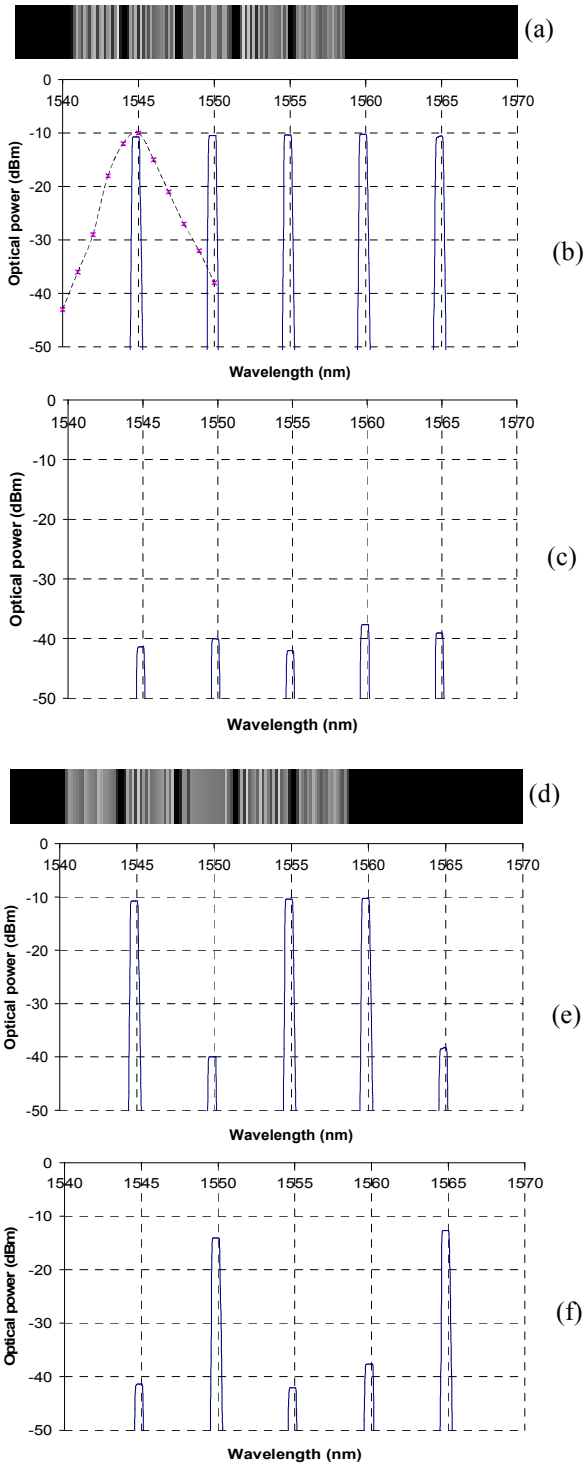

Fig.7. Phase hologram and corresponding output power spectra at the THRU and DROP ports of the ROADM.

(a) No-drop phase hologram,
(b) Output spectrum at THRU-port.
(c) Output spectrum at DROP-port.
(d) Drop phase hologram.
(e) Output spectrum at THRU-port when channels at 1550 nm and 1565 nm are dropped.
(f) Output spectrum at DROP-port when channels at 1550 nm and 1565 nm are dropped.

Note that acceptable crosstalk levels of less than -25 dB at the THRU and DROP ports are displayed. The crosstalk is due to high-order diffraction which can be improved by increasing the fill factor of the Opto-VLSI processor and enhancing the linearity of the electro-optic material used. Fig. 7(d) shows the hologram that drops the 1550nm and 1565nm wavelengths from the THRU port to the DROP port as shown in Figs. 7(e) and (f). For a VLSI chip fabricated using 130nm process, a 5-micron pixel size and an LC area of 20×20 mm^2 is practical. Theoretically, an Opto-VLSI processor having 48×48-pixel block size and 16-pixel dead spacing between adjacent blocks could dynamically add/drop more than 60 WDM channels. This demonstrates the potential of Opto-VLSI technology to offer reconfigurable MicroPhotonic components for future all- optical networks.

IV.CONCLUSION

In this paper, we have discussed promising MicroPhotonic architectures that perform optical header recognition and reconfigurable add/drop multiplexing for future optical networks. Experimental results have been shown, which demonstrate the principles of the optical header recognition and reconfigurable add/drop multiplexing structures.

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