Increasing the Efficiency of Interconnects Using A Compensating Circuit

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Abstract — **It is shown that the efficiency of an arbitrary previously designed interconnect can be increased using a suitable compensating circuit at its far end. A lossless lowpass circuit is considered for this purpose and its element values can be obtained by an optimization method. The proposed idea is evaluated using an example.**

Index Terms — **Interconnects, Compensating Circuit**

I. Introduction

An interconnect structure is a multi-conductor coupled transmission line designed to transfer several signals from the main die to the users. The far-end crosstalk and mismatching are two important phenomenas that degrade the performances of interconnects. The far-end crosstalk in interconnects result in the distortion of analog and digital signals and this difficulty increases as the frequency increases or the transverse dimensions decrease. Many efforts have been made to design of efficient interconnects, which have a low far-end crosstalk and a high matching in a wide frequency band [1-8]. Some of the ideas used in these efforts are as placing additional grounded or opened lines between signal traces [1-3], using multi-layer substrates [4-5], using additional discrete capacitances [6], using a gap in the ground plane [7] and using a homogeneous media [8]. However, in this paper a new idea is proposed to increase the efficiency of arbitrary interconnects. The basis of this idea is using a suitable circuit, called compensating circuit, between the user end of interconnects and their loads. In fact, an optimum compensating circuit is designed to increase the efficiency of a previously designed interconnect.

II. Analysis of Compensated Interconnects

Fig. 1 shows a general compensated interconnect, which consists of N coupled lines with length of d and a compensating circuit. It is assumed that all source and load impedances are the resistors R_S and R_L, respectively. The load voltage vector, $\mathbf{V}_L$, of the compensated interconnect can be written as follows

$$\mathbf{V}_L = \mathbf{H}_C \mathbf{F} \mathbf{V}_S = \mathbf{F}_C \mathbf{V}_S \tag{1}$$

in which $\mathbf{V}_S$ is the source voltage vector and $\mathbf{H}_C$ is an N by N matrix corresponding to the compensating circuit and relates the load voltages to the voltages of the far end of the interconnect. Also, $\mathbf{F}$ is an N by N matrix which relates voltages of the far end of the interconnect to the source voltages and can be written as follows [8]

$$\mathbf{F} = \mathbf{Z}_L \boldsymbol{\varphi}_{21} - \mathbf{Z}_L(\boldsymbol{\varphi}_{22} - \boldsymbol{\varphi}_{21}\mathbf{Z}_S) \times (\boldsymbol{\varphi}_{12} - \boldsymbol{\varphi}_{11}\mathbf{Z}_S - \mathbf{Z}_L\boldsymbol{\varphi}_{22} + \mathbf{Z}_L\boldsymbol{\varphi}_{21}\mathbf{Z}_S)^{-1}(\boldsymbol{\varphi}_{11} - \mathbf{Z}_L\boldsymbol{\varphi}_{21}) \tag{2}$$

in which and $\mathbf{Z}_L$ and $\mathbf{Z}_S$ are the load and source matrices, respectively seen at two ends of the interconnect. Also, $\boldsymbol{\Phi}$ is the chain parameter matrix of the interconnect obtaining as follows [8-9]

$$\boldsymbol{\Phi} = \begin{bmatrix} \boldsymbol{\varphi}_{11} & \boldsymbol{\varphi}_{12} \\ \boldsymbol{\varphi}_{21} & \boldsymbol{\varphi}_{22} \end{bmatrix} = \exp\left(- j\omega d \begin{bmatrix} \mathbf{0} & \mathbf{L} \\ \mathbf{C} & \mathbf{0} \end{bmatrix} \right) \tag{3}$$

where $\mathbf{L}$ and $\mathbf{C}$ are the per-unit-length inductance and capacitance matrices of the interconnect, respectively.

In fact, the matrix $\mathbf{F}_C$ in (1) represents the amount of matching (diagonal components) and the far-end crosstalk (off-diagonal components). So, in order to investigate the overall performance of interconnects, one may define the following performance factors in frequency of f

$$\eta_{LA}(f) = 10\log(P_L(f)/P_A) \le 0 \quad [dB] \tag{4}$$

$$\eta_{CA}(f) = 10\log(P_C(f)/P_A) \le 0 \quad [dB] \tag{5}$$

in which P_A, P_L and P_C are total available power, total power delivered to the far-end loads and total far-end crosstalk power delivered to the loads, respectively when all the N sources are applied separately. These powers can be written for a resistive loaded interconnect as follows (assuming V_{si}=1)

$$P_A = \frac{N}{8R_L} \tag{6}$$

$$P_L(f) = \frac{1}{2R_L}\sum_{i=1}^{N}\left(|\mathbf{F}_C(i,i;f)|^2\right) \tag{7}$$

$$P_C(f) = \frac{1}{2R_L}\sum_{i=1}^{N}\sum_{\substack{j=1 \\ j\neq i}}^{N}\left(|\mathbf{F}_C(i,j;f)|^2\right) \tag{8}$$

In fact, the factors η_{LA} and η_{CA} are the measures for delivered and crosstalk powers respectively.

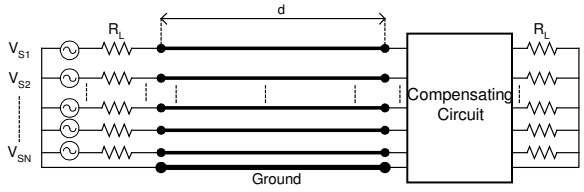

Fig. 1. A general compensated interconnect consisting of N coupled lines with length of d and a compensating circuit

III. Design of Compensating Circuit

In this section a method to optimum design of compensating circuit is presented. One sees from (1) that an ideal compensating circuit has to has the following property

$$|\mathbf{H}_C\mathbf{F}| = 0.5\mathbf{I} \tag{9}$$

in which $\mathbf{I}$ is N by N identity matrix. It is evident that the condition in (9) is not realized in a wide frequency band for all arbitrary interconnects. However, the lossless circuit shown in Fig. 2 can be considered as a practical realization of compensating circuit in a low-pass frequency band. In order to obtain the optimum values of the elements of this compensated circuit, the following error function

$$E^2 = \frac{1}{K}\sum_{k=1}^{K} 10^{\eta_{CA}(f_k)/10} = \frac{4}{KN}\sum_{k=1}^{K}\sum_{i=1}^{N}\sum_{\substack{j=1\\ j\neq i}}^{N}\left|\mathbf{F}_C(i,j;f_k)\right|^2 \tag{10}$$

has to minimized along with the following constraint in K frequencies.

$$\eta_{LA}(f) = 10\log\left(\frac{4}{N}\sum_{i=1}^{N}\left(|\mathbf{F}_C(i,i;f)|^2\right)\right) \geq R \ \ [dB] \ ; \tag{11}$$
$$\forall f = f_1, f_2, ..., f_K$$

where R is the minimum value considered for η_{LA}.

IV. Example and Results

As an example, consider a microstrip interconnect with $N = 2$ signal traces, the substrate permittivity of $\varepsilon_r = 10$, the length of $d = 10$ cm and the resistive loads of $R_L = 50\ \Omega$. Also, the width of two strips and the gaps between them are considered equal to the thickness of the substrate. The capacitance and inductance matrices are calculated as [10]

$$\mathbf{C} = \begin{bmatrix} 175.0 & -14.20 \\ -14.20 & 175.0 \end{bmatrix} [pF/m]$$

$$\mathbf{L} = \begin{bmatrix} 423.1 & 72.57 \\ 72.57 & 423.1 \end{bmatrix} [nH/m]$$

Also, two matrices $\mathbf{Z}_L$ and $\mathbf{H}_C$ are obtained versus the elements of the compensating circuit as

$$\mathbf{Z}_L = \left\{\left(\begin{bmatrix} 1/R_L + j\omega C_2 & -j\omega C_2 \\ -j\omega C_2 & 1/R_L + j\omega C_2 \end{bmatrix}^{-1} + \begin{bmatrix} j\omega L_1 & 0 \\ 0 & j\omega L_2 \end{bmatrix}\right)^{-1} + j\omega C_1 \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\right\}^{-1} \tag{12}$$

$$\mathbf{H}_C = 1/\left[1 - \omega^2(L_1C_2 + L_2C_2 + L_1L_2/R_L^2) + j\left(\omega(L_1+L_2)/R_L - 2\omega^3 L_1L_2C_2/R_L\right)\right] \times \begin{bmatrix} (1-\omega^2 L_2C_2) + j\omega L_2/R_L & -\omega^2 L_1C_2 \\ -\omega^2 L_2C_2 & (1-\omega^2 L_1C_2) + j\omega L_1/R_L \end{bmatrix} \tag{13}$$

To design the compensating circuit optimally in the frequency range of [0 – 5.9] GHz and for R = -1.5 dB, the following optimum values have been determined; $L_1 = L_2 = 1.0217$ nH, $C_1 = 0.9174$ pF and $C_2 = 0.7901$ pF. Figures 3-4 show the performance factors η_{LA} and η_{CA}, respectively for this optimum designed compensated interconnect. It is seen that, the delivered power performance factor is more than -1.5 dB and the crosstalk power performance factor has been decreased, both in the desired frequency band. So, one may satisfied about the usefulness of compensating the previously designed interconnects using the circuit shown in Fig. 2 to increase their efficiency.

VII. Conclusion

It was shown that the efficiency of an arbitrary previously designed interconnect can be increased using a suitable compensating circuit at its far end. A lossless lowpass circuit was studied and verified as a practical compensating circuit. It is expected that increasing the degree of this circuit may increase its performance.

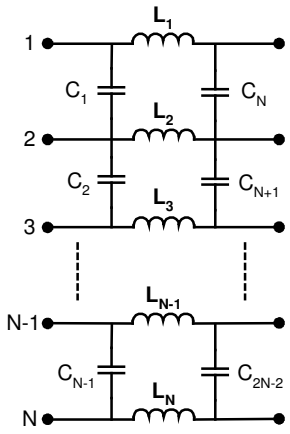

Fig. 2. A lossless and lowpass circuit suitable to compensate the interconnects

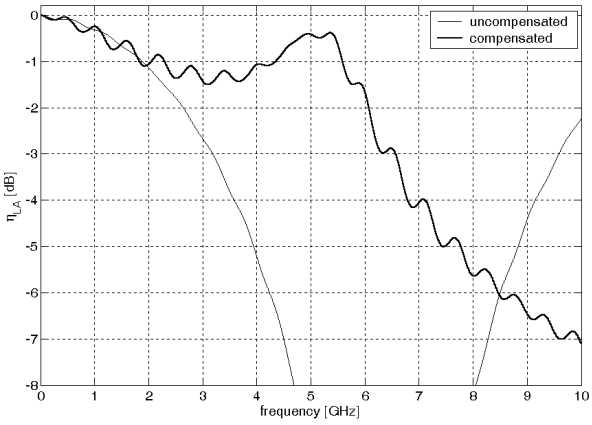

Fig. 3. The delivered power performance factor η_{LA} for the compensated and uncompensated microstrip interconnect

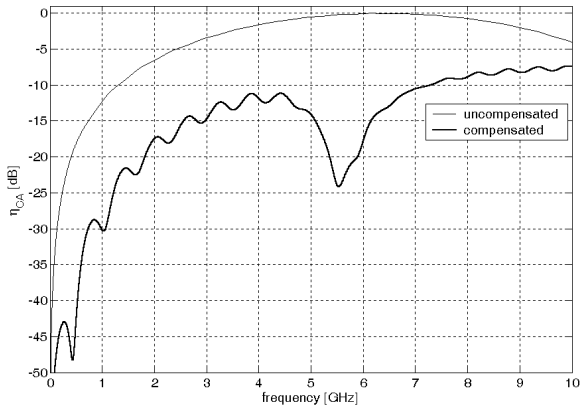

Fig. 4. The crosstalk power performance factor η_{CA} for the compensated and uncompensated microstrip interconnect

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