King Fahd University of Petroleum & Minerals, Electrical Engineering Department

EE 415: Analog Integrated Circuits Analysis And Design

Second Semester 2004-2005 (042), **Midterm Exam Part (I)**

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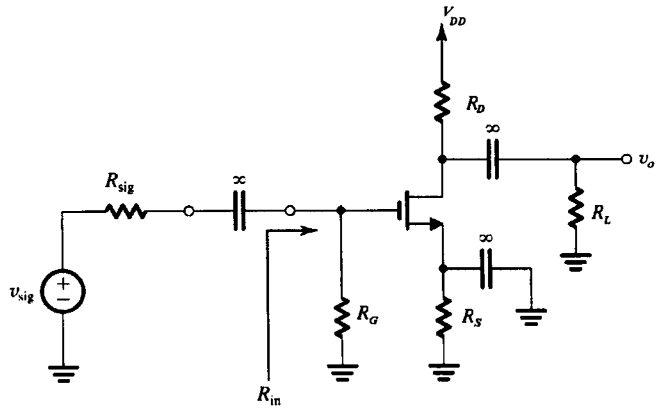
Name	Key
ID#	

Question # 1(7):

For the MOSFET amplifier shown below, R_{sig}=100 KΩ, R_G= 100 KΩ, C_{gs}=1pF, C_{gd} =.20pF, g_m=3mA/V, r_{ds}= 50KΩ, R_D = 8 KΩ, and R_L= 10 KΩ.

a) Determine the midband gain ($A_v=v_o/v_{sig}$) and the expected 3-dB cutoff frequency f_H. 4

b) To double f_H a designer considers changing either R_{out} or R_{in}, evaluate the two options in terms of the change in the midband gain. 3



a) $A_v = -\frac{R_G}{R_{sig}+R_G} g_m (R_D // R_L // r_{ds})$

$= -6.1 \; V/V$

f_H:

$\tau_1 = [C_{gs} + (1-A)C_{gd}](R_G // R_{sig})$

$A = -g_m (R_D // R_L // r_{ds}) = -12.3 \; V/V$

$\Rightarrow \tau_1 = 1.83 \times 10^{-7}$ sec

$\tau_2 = \left[\frac{C_{gd}}{(1-A)}\right](R_D // R_L // r_{ds}) = 7.348 \times 10^{-11}$ sec

$\omega_H \simeq \frac{1}{\tau_1} = 5.464 \times 10^6$ rad/s $\Rightarrow f_H = 870$ KHz

b) $\omega_H \simeq \frac{1}{[C_{gs} + (1-A)C_{gd}](R_G // R_{sig})}$ to double f_H < $\frac{A}{2}$ using R_{out}; $\frac{R_G}{2}$ which is R_{in}

Approach 1

Reducing C_i by making $A_{new} = \frac{A}{2}$ (through R_{out})

$R_{out} = R_D \,||\, r_{ds}$ if R_D is reduced to $\simeq 1.5\ K\Omega$

$A_{new} = -3.8\ V/V \Rightarrow \omega_H = 10.2 \times 10^6\ rad/s$

$f_H = \underline{1.624\ MHz}$

$A_V = \frac{R_G}{R_G + R_{sig}} A_{new} = \underline{-1.9\ V/V}$

Approach 2

Reducing $R_{G_{new}} = 33\ K\Omega$

$$\omega_H \simeq \frac{1}{[C_{gs} + (1-A)C_{gd}](R_{G_{new}} \,||\, R_{sig})} = 11.01 \times 10^6\ rad/s$$

$f_H = \underline{1.75\ MHz}$

$A_V = \frac{R_{G_{new}}}{R_{G_{new}} + R_{sig}} A = \underline{-3.05}\ V/V$

Approach 2 is better than ①. It provides higher gain.

Question # 2: (7)

a) Design the current sources in the MOS amplifier shown in Fig. 1.
Use the current steering circuit shown in Fig. 2 which is fabricated in a technology with k'_n=90uA/V^2, k'_p=30uA/V^2, V_{tn}=0.8V, V_{tp}=-0.9V, V_A=50V.
If all devices have L=2um and W_{Q1}= W_{Q3} = W_{Q4}=2um. I_{REF}= 20uA.
Find: R, W_{Q2}, W_{Q5} 3 $\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_7 = \frac{2\mu}{2\mu}$

b) Determine the upper limit of v_o.   1

c) Find an expression for the voltage gain $A_v=v_o/v_i$ in terms of g_{m6}, g_{m7}, r_{o6}, r_{o7}, r_{o2}, r_{o5}.   2

d) Calculate the voltage gain $A_v=v_o/v_i$ 1

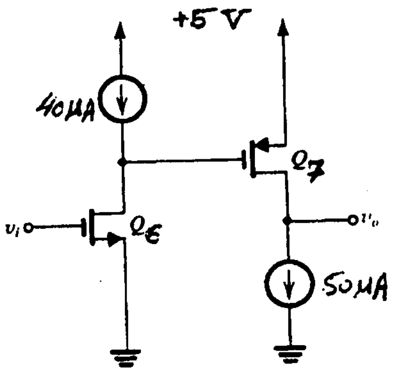


Fig. 1

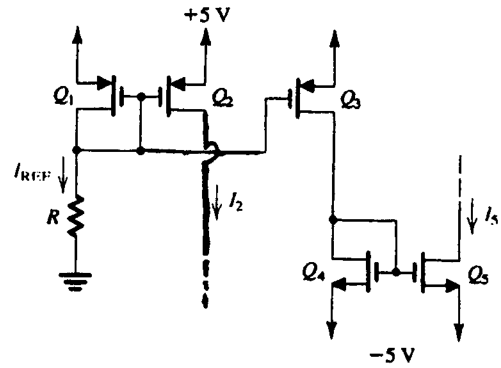


Fig. 2

Q2

a) $I_{REF} = \frac{1}{2} K_n' \left(\frac{W}{L}\right)_1 (V_{GS_1} - V_t)^2$

$20\mu = \frac{1}{2}(30\mu)\left(\frac{2}{2}\right)(V_{GS1} - 0.9)^2 \Rightarrow V_{GS1} = -2.05\ V$

$R = \frac{V_{DD} - V_{SG1}}{I_{REF}} = \frac{2.95}{20\mu} = 147.26 K\Omega$

$I_2 = 40\ \mu A \Rightarrow \frac{(W/L)_2}{(W/L)_1} = \frac{I_2}{I_1} = 2 \Rightarrow W_{Q2} = 4\mu m$

$I_5 = 50\ \mu A \Rightarrow \frac{(W/L)_5}{(W/L)_4} = \frac{I_5}{I_4} = \frac{50\mu}{20\mu} = 2.5$

$W_{Q5} = 5\ \mu m$

b) $V_{omax} = V_{DD} - V_{eff_7}$; $V_{eff_7} = V_{GS7} - V_t$

$V_{eff_7} = \sqrt{\frac{2 I_7}{K_p' \left(\frac{W}{L}\right)_7}} = \sqrt{\frac{2 \times 50\mu}{30\mu \times \left(\frac{2}{2}\right)}} = \sqrt{\frac{100\mu}{30\mu}} = 1.83V$

$V_{omax} = 5 - 1.83 = 3.17V$

c) $\frac{V_o}{V_i} = \left[-g_{m6}(r_{ds6} \| r_{ds2})\right]\left[-g_{m7}(r_{ds7} \| r_{ds5})\right]$

$= g_{m6}\, g_{m7}\, (r_{ds6} \| r_{ds2})(r_{ds7} \| r_{ds5})$

d) $g_{m6} = \sqrt{2 K_n' \left(\frac{W}{L}\right)_6 I_{D6}} = \sqrt{2 \times 90\mu \times 40\mu} = 84.8\ \mu A/V$

$g_{m7} = \sqrt{2 K_p' \left(\frac{W}{L}\right)_7 I_{D7}} = \sqrt{2 \times 30\mu \times 50\mu} = 54.8\ \mu A/V$

Q2

$$r_{ds_6} = r_{ds_2} = \frac{V_A}{I_{D2/6}} = \frac{50}{40\mu} = 1.25 M\Omega \;;$$

$$r_{ds_7} = r_{ds_5} = \frac{V_A}{I_{D_{7,5}}} = \frac{50}{50\mu} = 1. M\Omega$$

$$\frac{v_o}{v_i} = 84.8\mu \times 54.8\mu \times (1.25M \,||\, 1.25M)(1M \,||\, 1M)$$

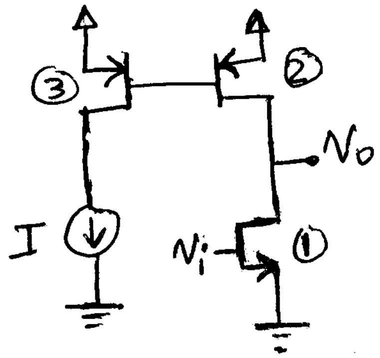
$$= 1452.2 \; V/V$$

Question # 3: (6)

Assuming that MOSFETs used in the following designs have g_m on the order of 0.75mA/V and r_{ds} on the order of 100kΩ,

a) Draw an integrated circuit common source amplifier and estimate its voltage gain. 2
b) Draw an integrated circuit cascode amplifier and estimate its voltage gain. 2
c) Compare the two configurations in terms of gain and output voltage swing. 2

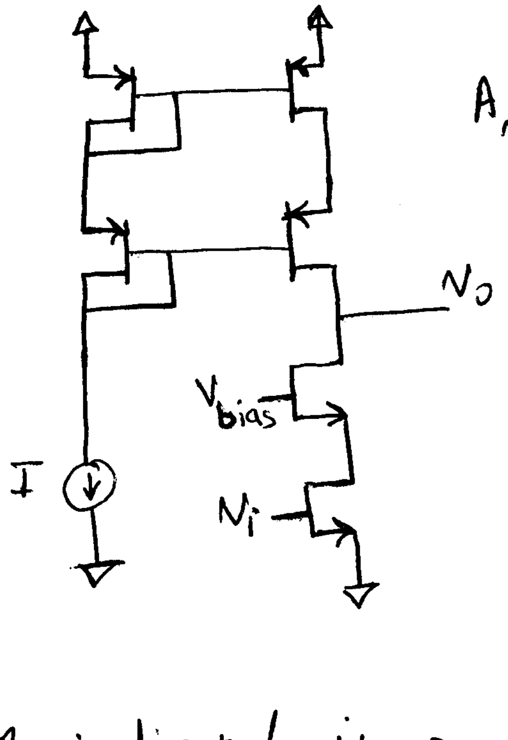
a)



$$A_V = \frac{V_o}{V_i} = -g_{m1}(r_{ds1} \| r_{ds2})$$

$$= -0.75m(100K \| 100K) = -37.5$$

b) Cascode



$$A_V = \frac{V_o}{V_i} = -\frac{g_m^2 r_{ds}^2}{2} = -703.1 \text{ V/V}$$

c) As indicated in parts a & b:

cascode amplifier has a higher voltage gain.

in terms of Voltage swing, it is known that simple Common Source Amplifier has a wider voltage swing