EE-203 : Electronics I MAJOR I EXAM

Name: Instructor: Dr. Saad Mohammad Al-Shahrani

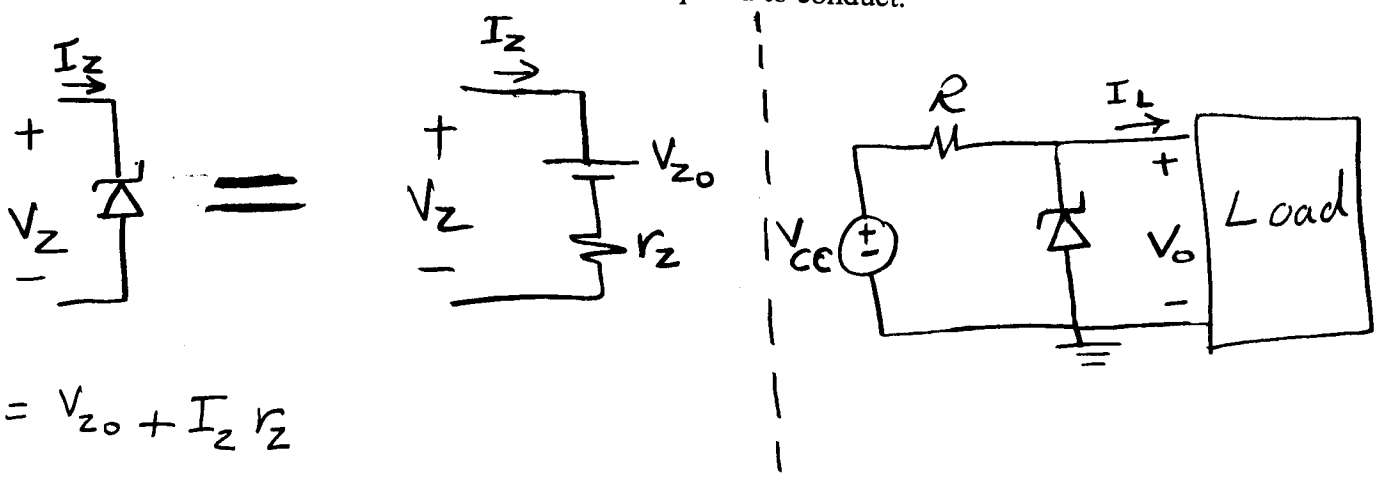
ID #

Question # 1: (5)

Design a zener shunt regulator to provide a voltage regulated of about 10V. The available zener diode is specified have $V_Z = 10V$ at $I_Z = 25$ mA, $r_Z = 10\Omega$, and $I_{ZK} = 5$ mA. The supply voltage $V_{CC}$ is nominally 20V but can vary b ±5V. The regulator is required to supply a load current of 0 mA to 20 mA.

a) Find $V_{ZO}$ for this zener diode.
b) Find R.
c) Find the change in $V_O$ resulting from the ±5V change in $V_{CC}$.
d) Find the load regulation.
e) What is the maximum current that zener diode is required to conduct.

a)




$$V_Z = V_{Z_o} + I_Z r_Z$$

$$10 = V_{Z_o} + 25m \times 10 \Rightarrow V_{Z_o} = 9.75\,V$$

b) $$R \leq \frac{V_{CC_{min}} - [V_{Z_o} + I_{ZK} r_Z]}{I_{ZK} + I_{L_{max}}} = \frac{15 - [9.75 + 50m]}{5m + 20m}$$

$$R \leq 208\,\Omega$$

I will use $\underline{\underline{R = 180\,\Omega}}$

c) $$\Delta V_o = \mp 5 \times \frac{r_Z}{R + r_Z} = \mp 0.25\,V$$

d) Load regulation $= -r_Z // R = -9.47\,mV/mA$

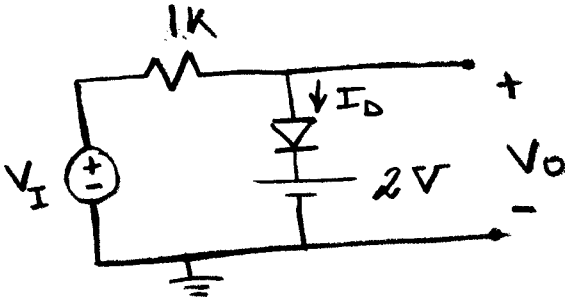
e) $$I_{Z_{max}} = \frac{V_{CC_{max}} - [V_{Z_o} + I_{Z_{max}} r_Z]}{R} = \frac{25 - [9.75 + 10\, I_{Z_{max}}]}{180}$$

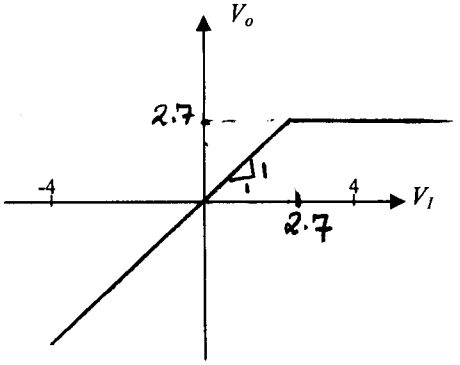
$$I_{Z_{max}} = 80.3\,mA$$

Question # 2: (5)

Assuming that diodes in the circuit shown below are modeled with the constant voltage drop model ($V_{DO}$=0.7V).

1. Sketch the transfer characteristic $V_O$ versus $V_I$ (including slope and important points).
2. Sketch the transfer characteristic $I_D$ versus $V_I$ (including slope and important points).
3. Sketch and clearly label the waveform $V_O$ for the input voltage $V_I$.
4. Find the average value of $V_O$ (DC)?

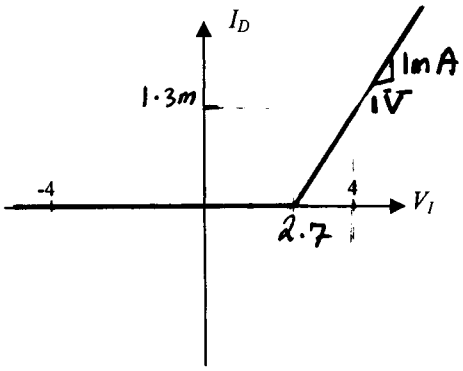



For $V_I < 2.7$ Diode off

$V_o = V_I$

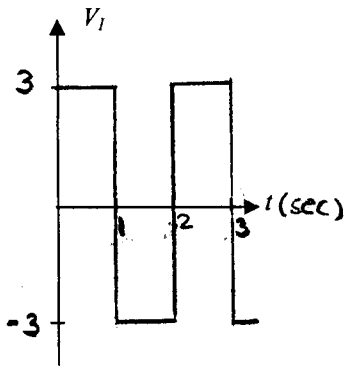
$I_D = 0$




For $V_I \geq 2.7$ Diode ON

$V_o = 2.7\ V$

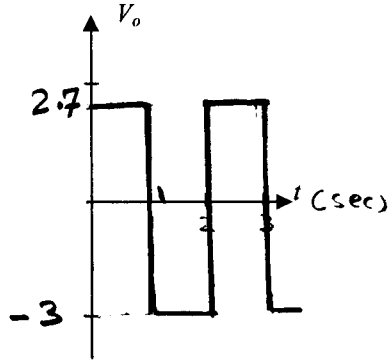
$I_D = \frac{V_I - V_o}{1K} = \frac{V_I - 2.7}{1K}$




4. DC = Average of $V_o$ = $\frac{\text{Area}}{\text{Period}}$

$V_{o_{DC}} = \frac{(2.7 \times 1) + (-3 \times 1)}{2}$

$= -0.15\ V$

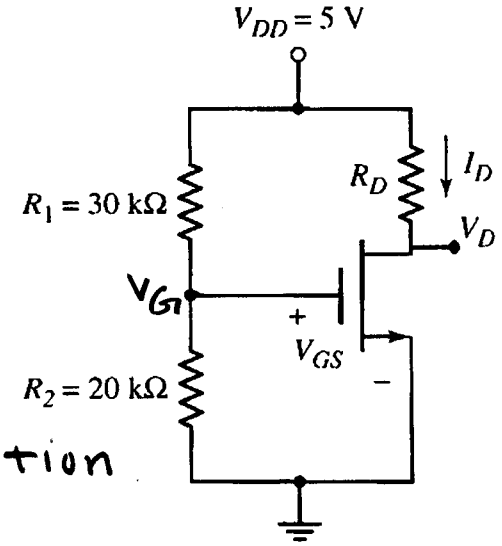


stion # 3: (3+2)

) For the circuit shown below, the enhancement NMOS transistor parameters are: $V_t = 1V$, **and** $K_n'(W/L)=0.1mA/V^2$.

Design $R_D$ so that $V_D$=3V;

Calculate drain current $I_D$, and voltage $V_{GS}$.




$V_G = V_{GS} = 5 \frac{20K}{20K+30K} = 2\ V$

$V_{GS} > V_t$ NMOS is ON

$V_{GD} = V_G - V_D = 2 - 3 = -1$

$V_{GD} < V_t$ NMOS in Saturation

$I_D = \frac{1}{2} K_n' \frac{W}{L} [V_{GS} - V_t]^2 = \frac{1}{2}(0.1m)(2-1)^2 = 0.05mA$

$= 50\mu A$

$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5-3}{50\mu} = 40K\Omega$

b) Fill in the table below for MOS transistors circuits. Assuming that $k'=100uA/V^2$, $|V_t|=1.2$ V, *(W/L)= (20um/2um)* for all transistors.

| Case | MOS Type | VG | VD | VS | Operation Mode | $I_D$ |
|---|---|---|---|---|---|---|
| 1 | Enhancement NMOS | 3 | 2 | 1 | Saturation | 0.32 mA |
| 2 | Enhancement NMOS | 3 | 1 | 1.5 | Triode | 12.5 uA |
| 3 | Enhancement PMOS | 1 | 2 | 2.5 | Triode | 12.5 uA |
| 4 | Enhancement PMOS | 1 | 1 | 1.5 | Off | 0 |