King Fahd University of Petroleum & Minerals

Excellent
5.0
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EE- 205

Project #1
Transient Response of Second Order RLC Circiuts

Prepared for:
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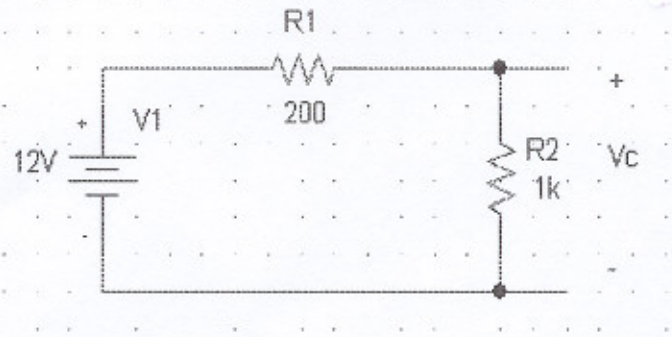
➢ Designing the value of R_1:

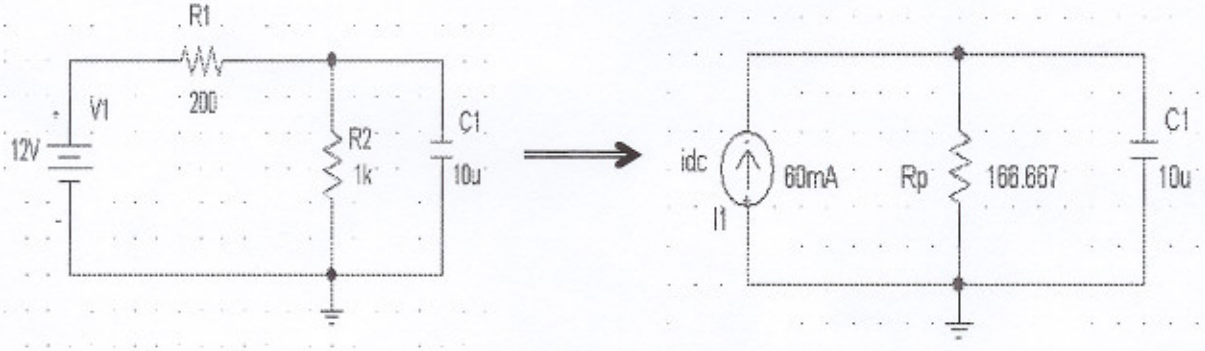
If we want to design a value of R_1 to achieve a full charge of 10V across the capacitor, we have to consider the capacitor as an open circuit and the voltage across the R_2 is 10V. Then, using voltage divider rule we can obtain the value of R_1:

$$V_{R2} = \frac{R_2}{R_1 + R_2} V_S \longrightarrow 10 = \frac{1000}{1000 + R_1} 12 \longrightarrow R_1 = 200\ \Omega$$



➢ Designing the time of closing the switch:

Actually if we want to close the switch when the capacitor is fully charged, this means it will close at ∞. But because this is a parallel RC circuit, we can say that the capacitor is fully charged at about 7τ which is 7*R*C.
So, $7\tau = 11.667$ ms. Then the switch will close at 11.667 ms.



➢ Designing the value of the inductor:

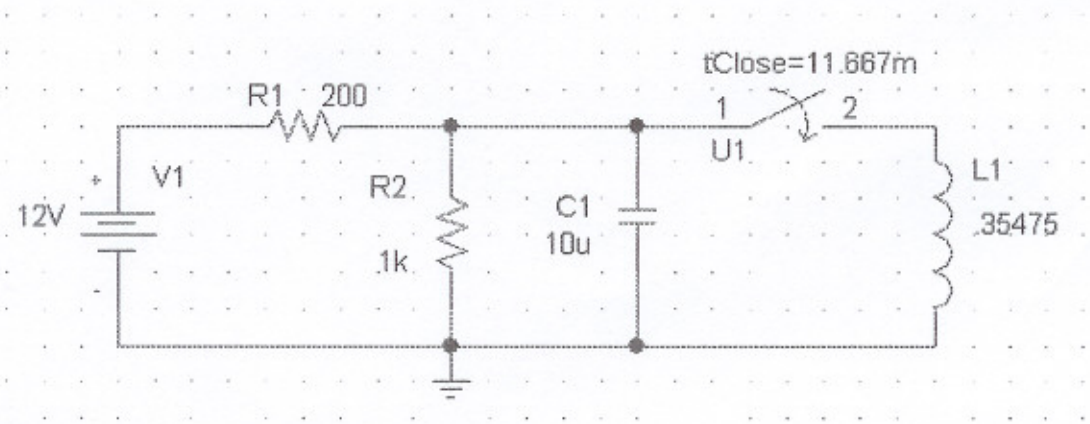
To achieve the final current value as fast as possible with an overshoot of 20%, we consider the under-damp situation. The final value is 60 mA (short-circuit so the whole current will pass) and with 20% it means 72 mA as maximum. But first we can obtain the value of L by considering the critical situation where: $w_n = \alpha$:

$$\frac{1}{\sqrt{LC}} = \frac{1}{2RC} \longrightarrow L = 4R^2C \longrightarrow L = 1.11\ \text{H}$$

To achieve the under-damped situation, w_n must be greater than α. So we can decrease the value of L until we reach the maximum current of 72 mA. Using PSpice, I found that the best value I could have of L is: 354.75 mH and it takes 14.399 ms to achieve 60 mA which is the final value.

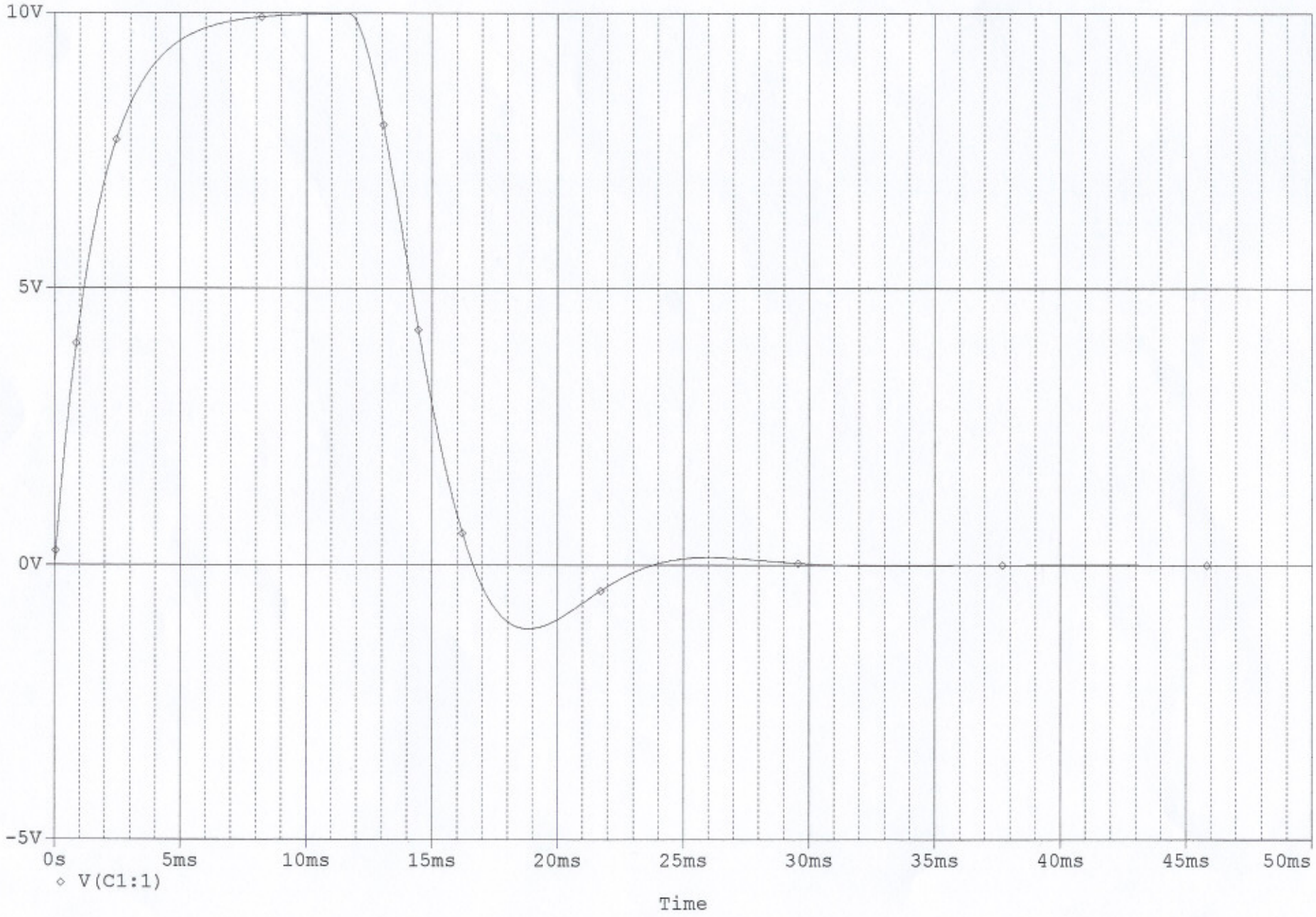
(PSpice specification: Transient analysis: print step = 20 ns, final time= 50 ms, step ceiling = 100 μs)

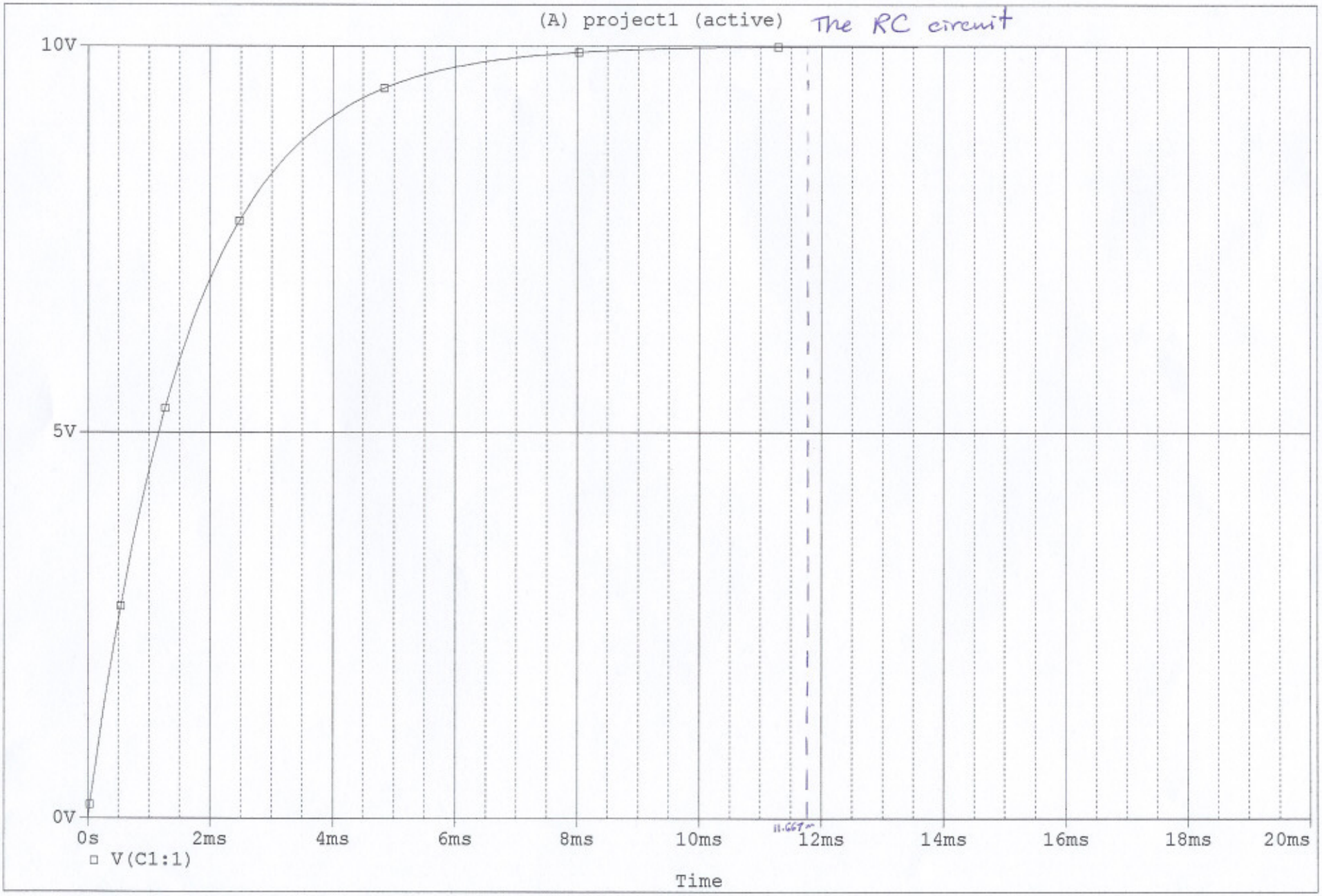
Final Circiut Design:

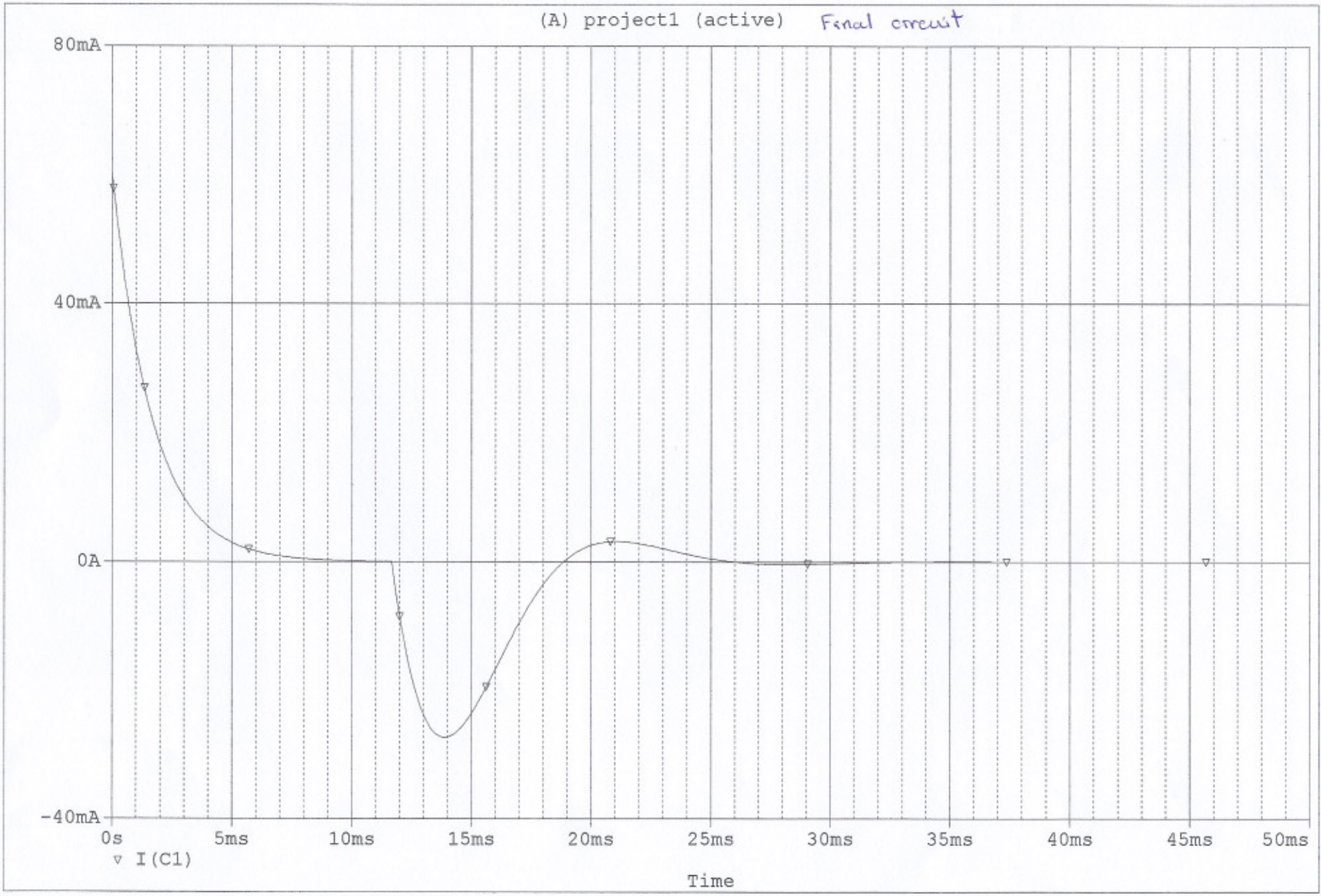


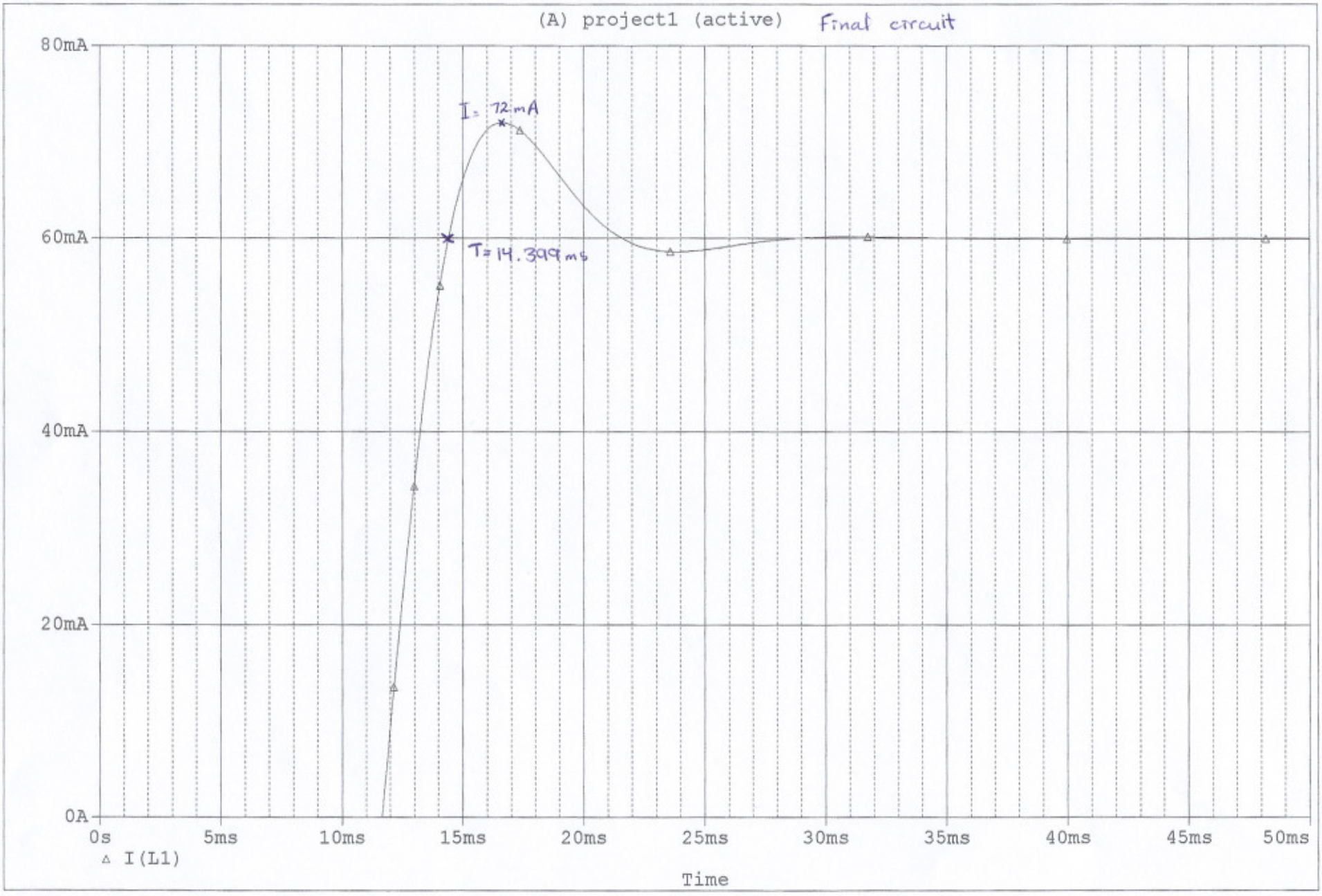
$V_s = 12$ V dc
$R_1 = 200\ \Omega$
$R_2 = 1\ \text{k}\Omega$
$C_1 = 10\ \mu\text{F}$
$L_1 = 354.75$ mH

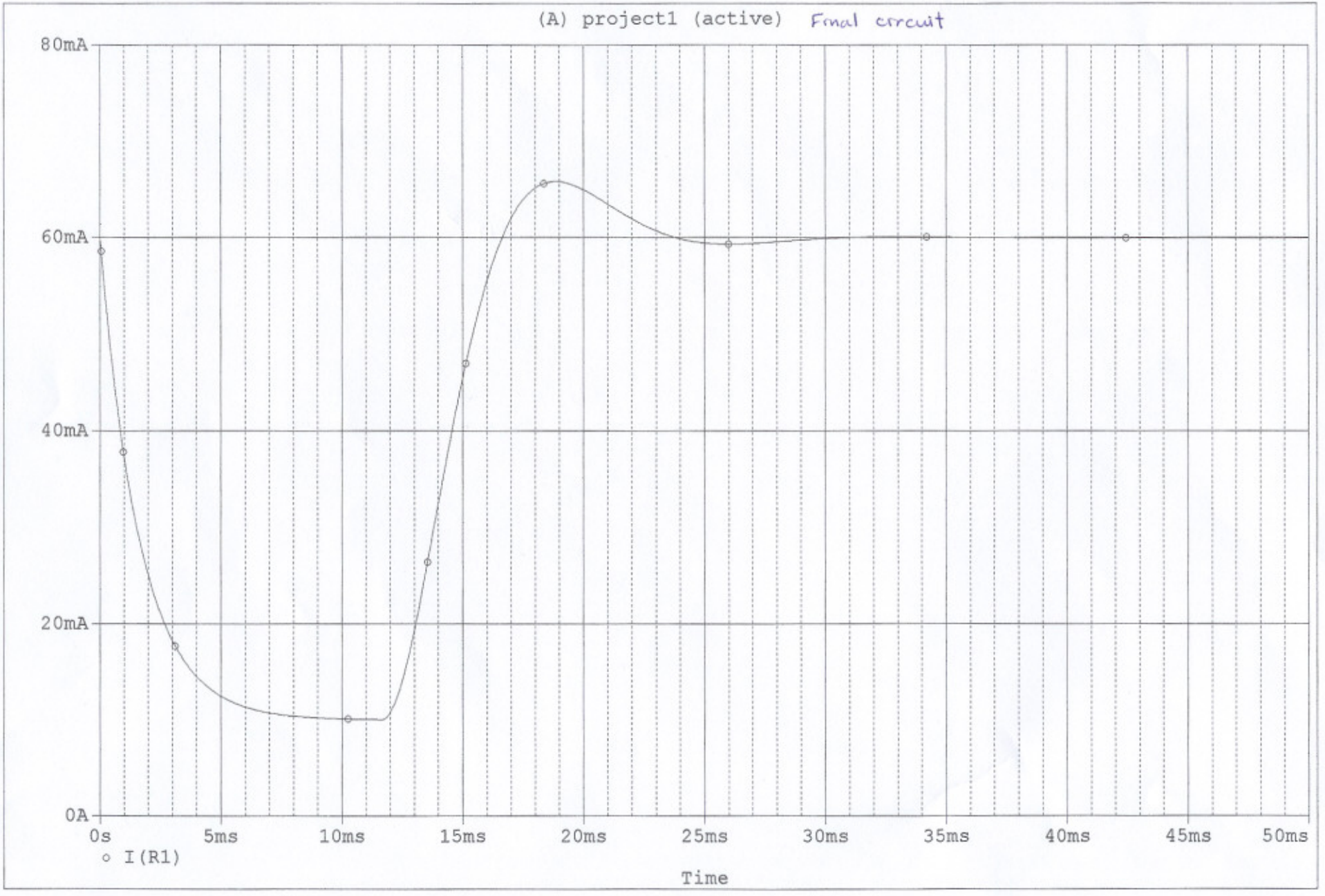
Final circuit

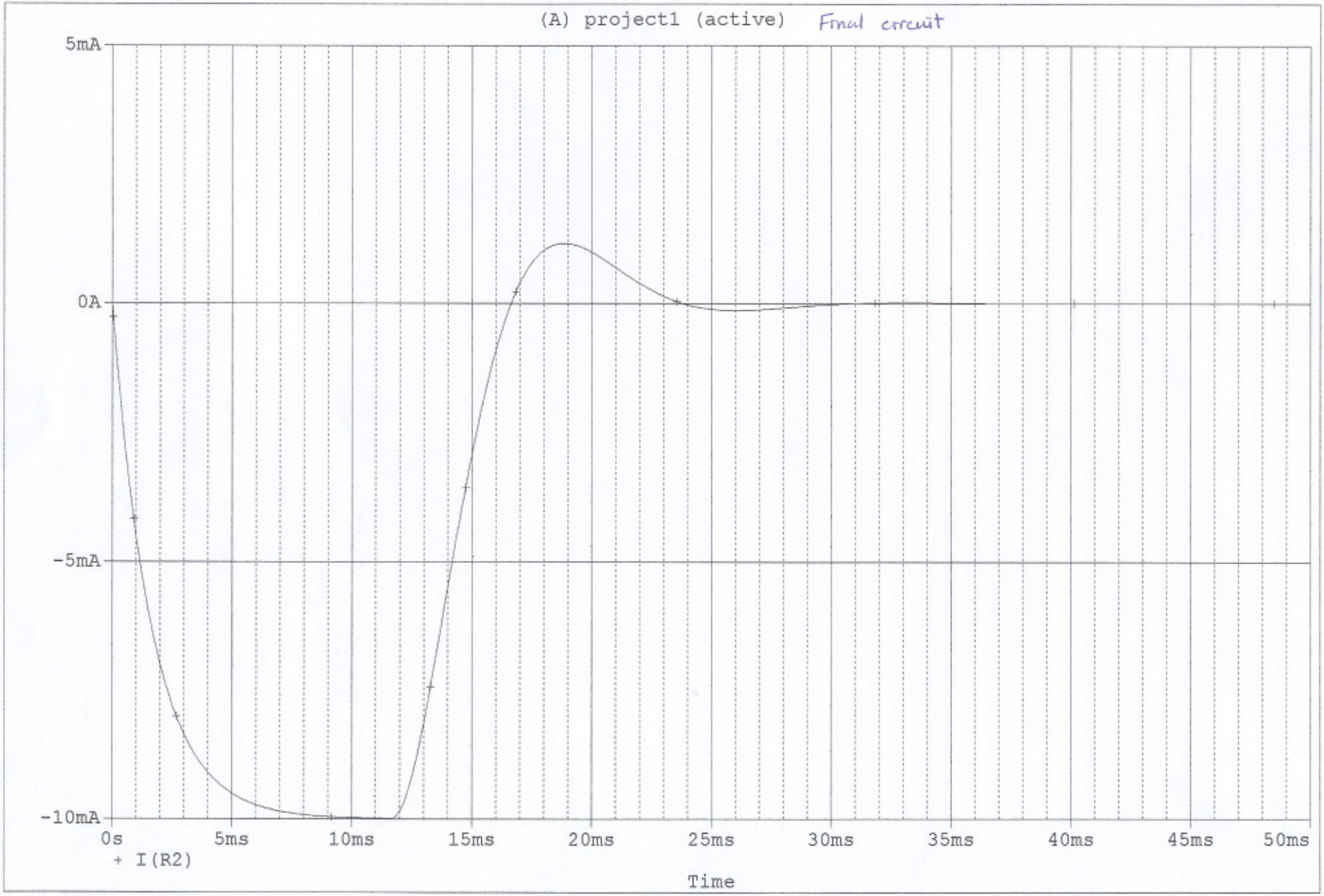


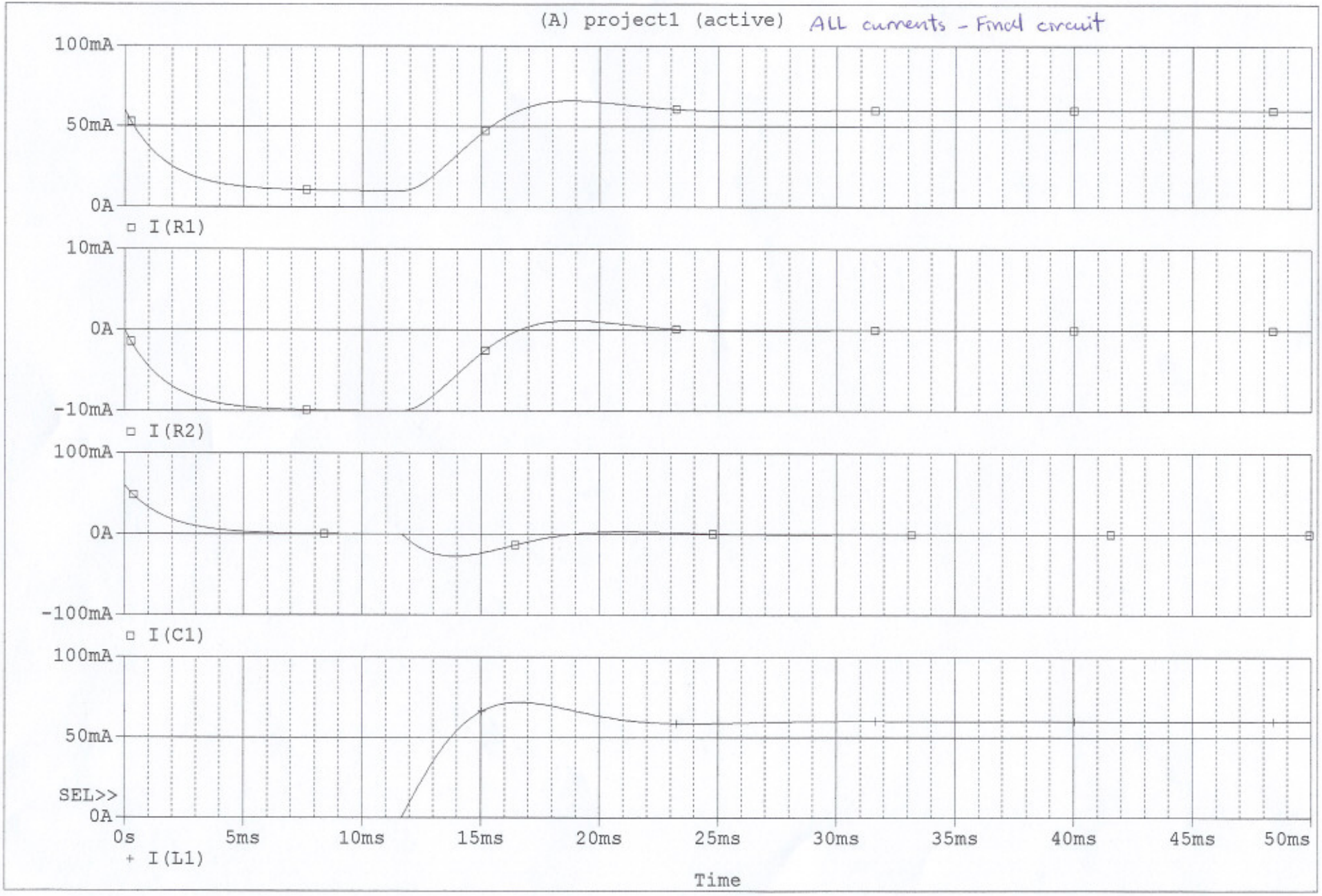

(A) project1 (active)
The RC circuit
10V
5V
0V
0s
2ms
4ms
6ms
8ms
10ms
12ms
14ms
16ms
18ms
20ms
V(C1:1)
Time


(A) project1 (active)
Final circuit
80mA
40mA
0A
-40mA
0s
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms
I(C1)
Time


(A) project1 (active)
Final circuit
80mA
60mA
40mA
20mA
0A
I= 72mA
T= 14.399ms
0s
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms
I(L1)
Time


(A) project1 (active)
Final circuit
80mA
60mA
40mA
20mA
0A
0s
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms
I(R1)
Time


(A) project1 (active)
Final circuit
5mA
0A
-5mA
-10mA
0s
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms
+ I(R2)
Time


(A) project1 (active)
ALL currents - Final circuit
100mA
50mA
0A
I(R1)
10mA
0A
-10mA
I(R2)
100mA
0A
-100mA
I(C1)
100mA
50mA
SEL>>
0A
0s
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms
I(L1)
Time