Tutorial on
Simulation
using
Aldec Active-HDL

Ver 2.0

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Introduction

Active-HDL is an integrated environment designed for development of VHDL designs. The core of the system is a VHDL simulator. Along with debugging and design entry tools, it makes up a complete system that allows you to write, debug and simulate VHDL code. Based on the concept of a design, Active-HDL allows you to organize your VHDL resources into a convenient and clear structure.

Students can use Active-HDL to perform following tasks:

- development of the VHDL based designs,
- functional simulation of their code,
- functional simulation of the synthesized code,
- timing simulation of the hardware implementation.

Objective

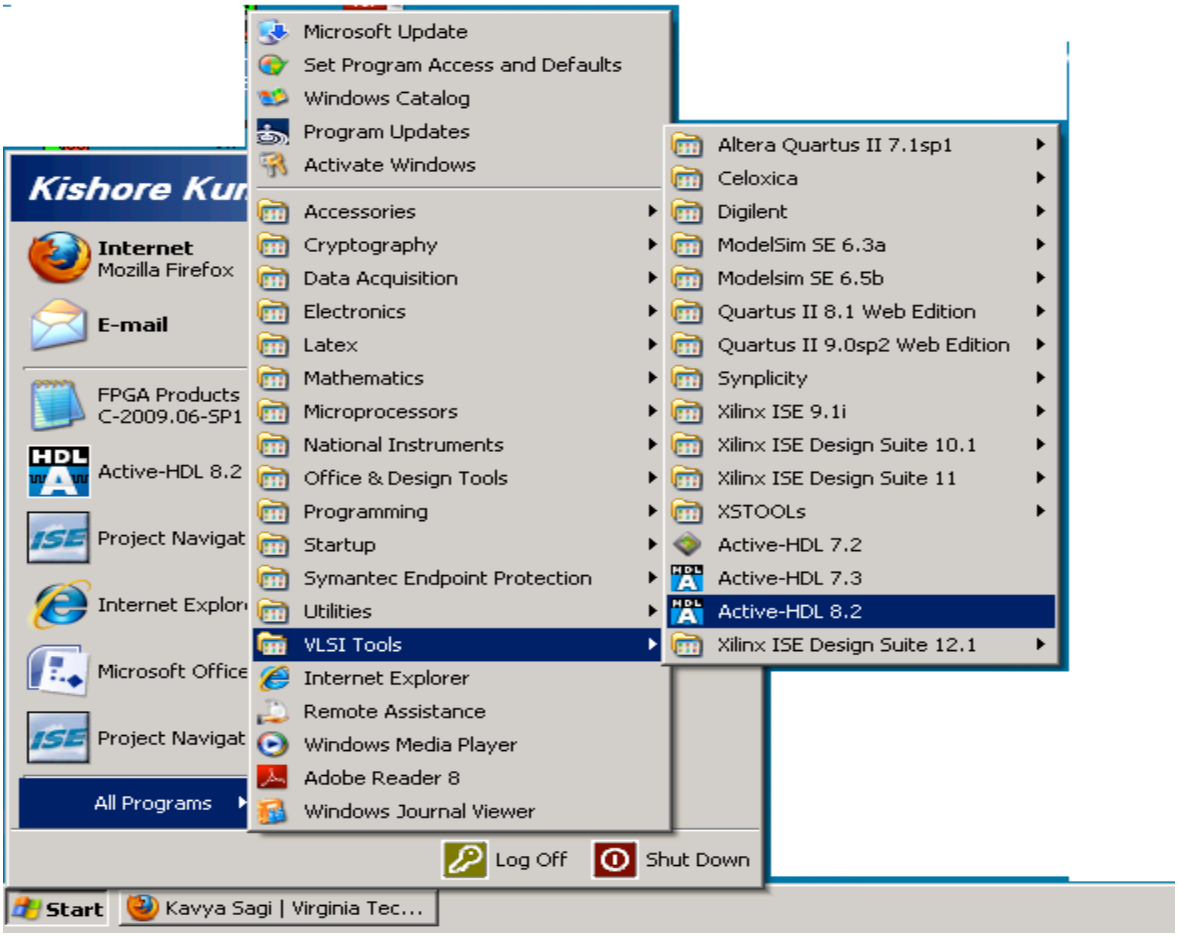
This tutorial helps you to

- Create a new design or add .vhd files to your design
- Compile and debug your design
- Perform simulation

Note : This tutorial does not explain the synthesis or implementation steps.

Start-up

1. Start >> VLSI Tools >> Active-HDL 8.2


Kishore Kur
Internet
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Active-HDL 8.2
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Microsoft Office
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Microsoft Update
Set Program Access and Defaults
Windows Catalog
Program Updates
Activate Windows
Accessories
Cryptography
Data Acquisition
Electronics
Latex
Mathematics
Microprocessors
National Instruments
Office & Design Tools
Programming
Startup
Symantec Endpoint Protection
Utilities
VLSI Tools
Internet Explorer
Remote Assistance
Windows Media Player
Adobe Reader 8
Windows Journal Viewer
Altera Quartus II 7.1sp1
Celoxica
Digilent
ModelSim SE 6.3a
Modelsim SE 6.5b
Quartus II 8.1 Web Edition
Quartus II 9.0sp2 Web Edition
Synplicity
Xilinx ISE 9.1i
Xilinx ISE Design Suite 10.1
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Xilinx ISE Design Suite 12.1
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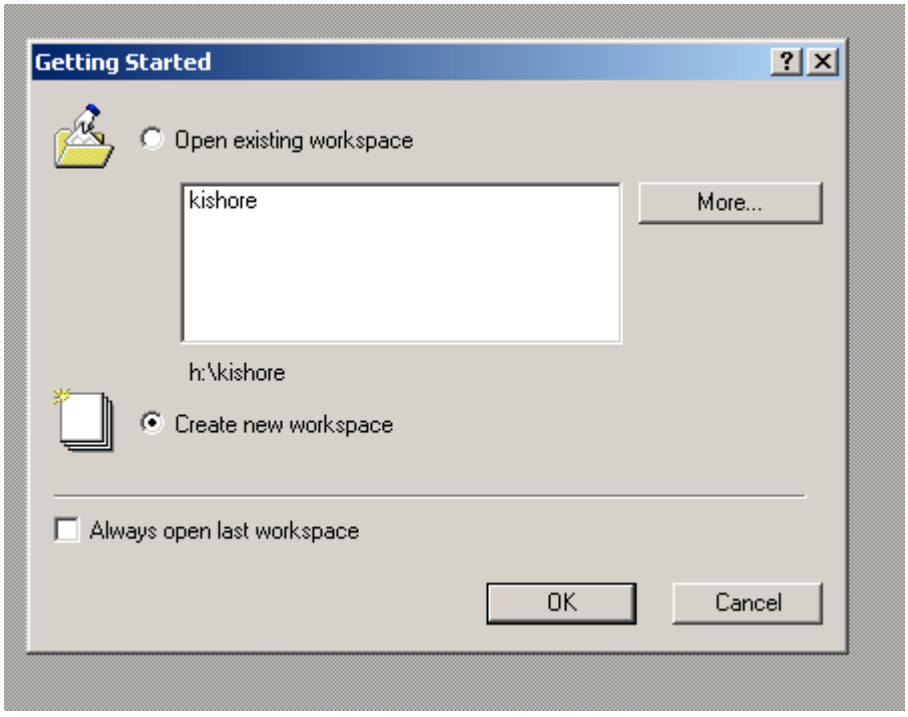
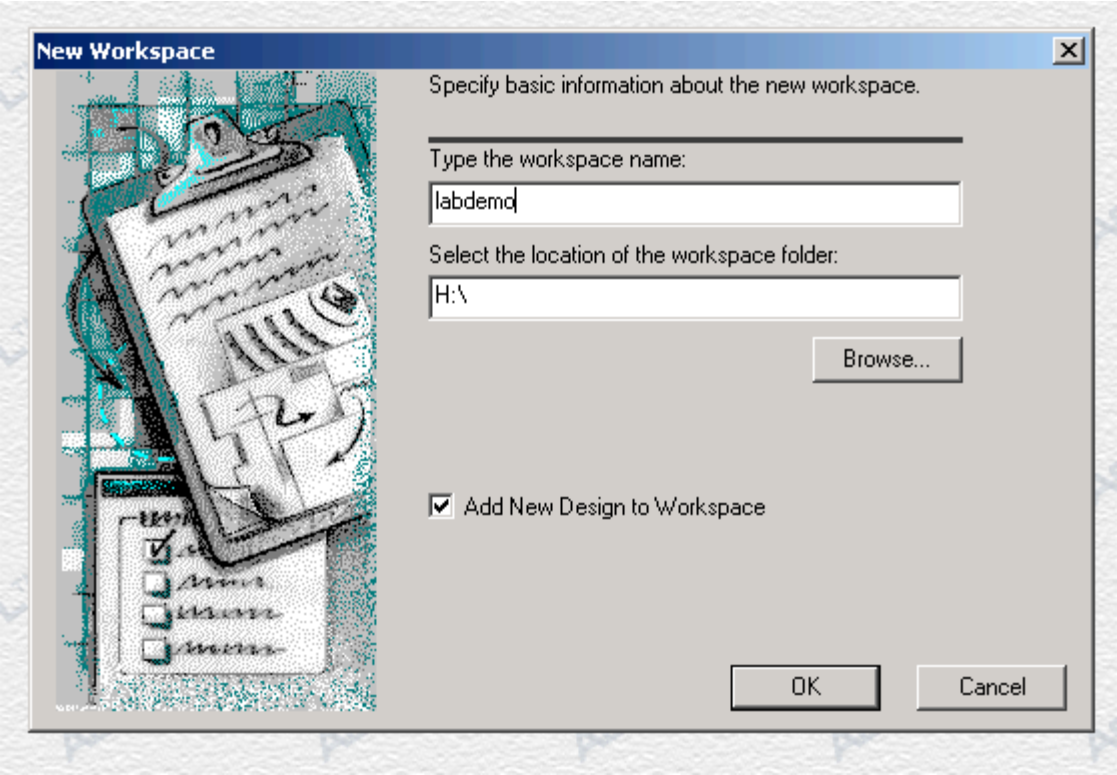
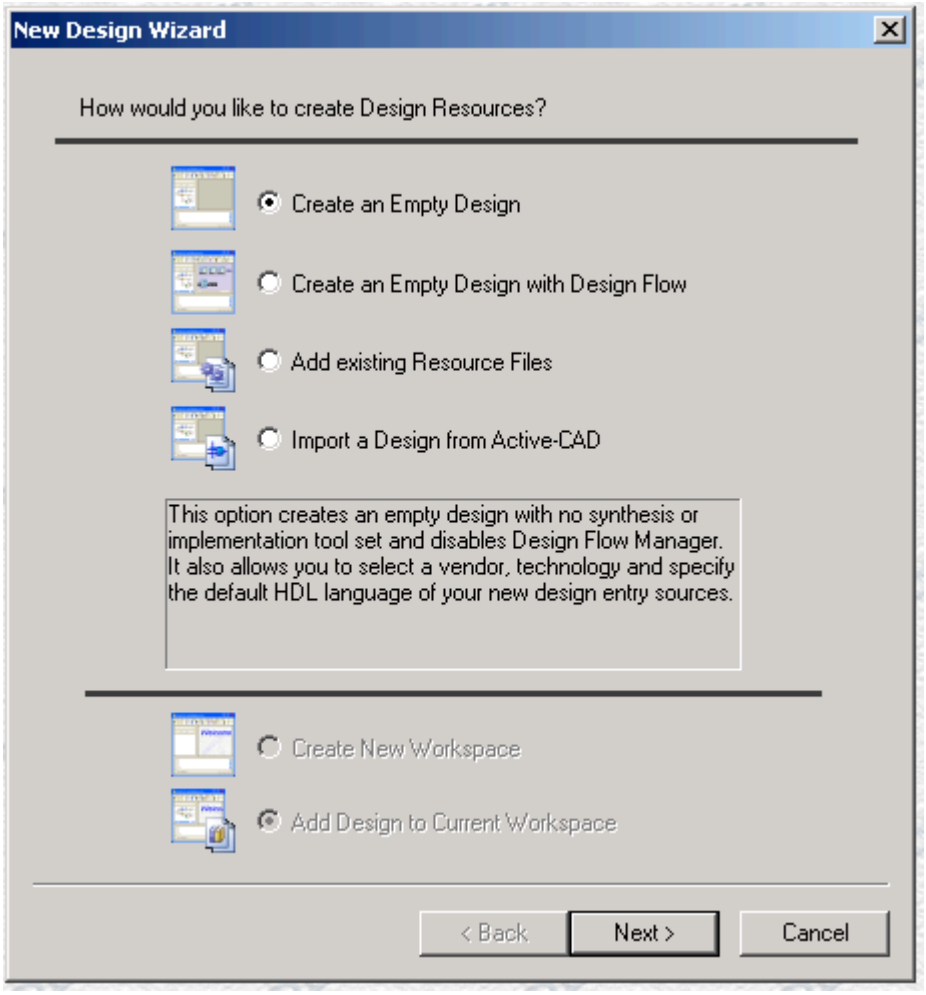

Getting Started
Open existing workspace
kishore
More...
h:\kishore
Create new workspace
Always open last workspace
OK
Cancel

a. Select create new workspace and click OK, creates new workspace in your directory.
b. Selecting open existing workspace gives you the option to choose from your previous Workspace's.

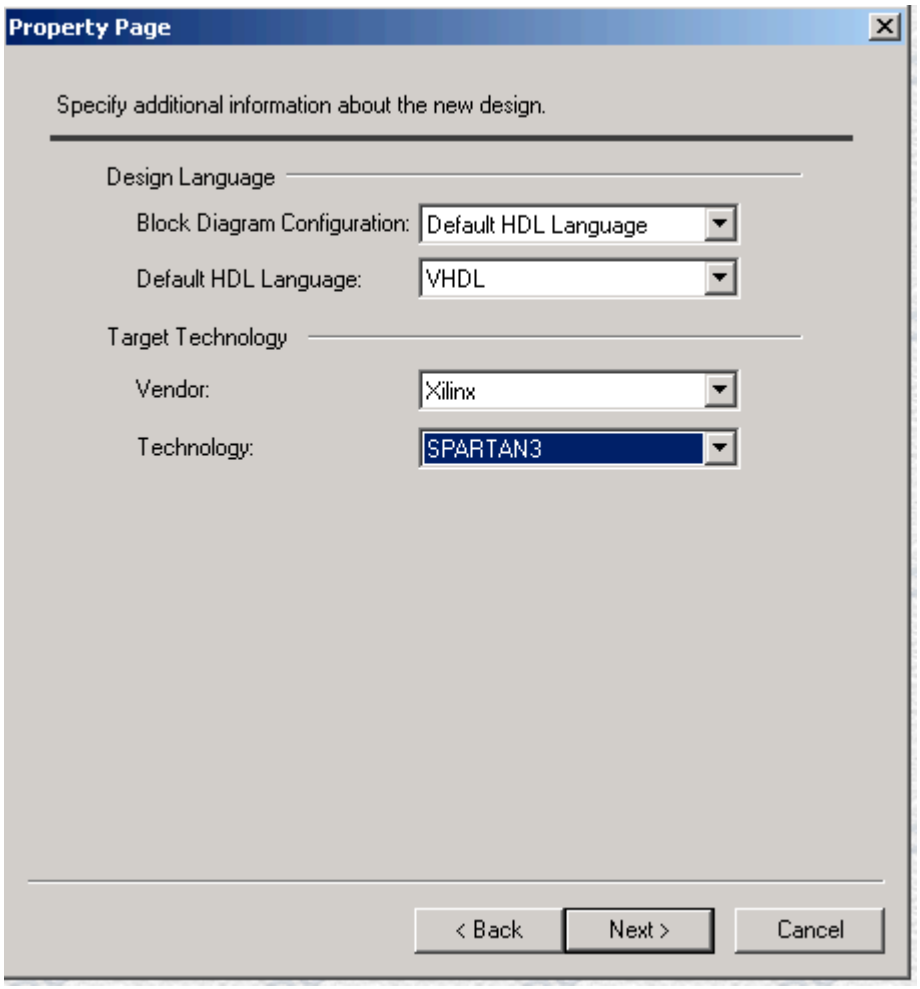
2. Type the name and select location of your desired workspace and click **OK**. If you're using school's lab, it is recommended to work in your local's drive (D drive), as your thumb drive and your network drive (K drive) are slow. For now, use "labdemo" as your workspace.



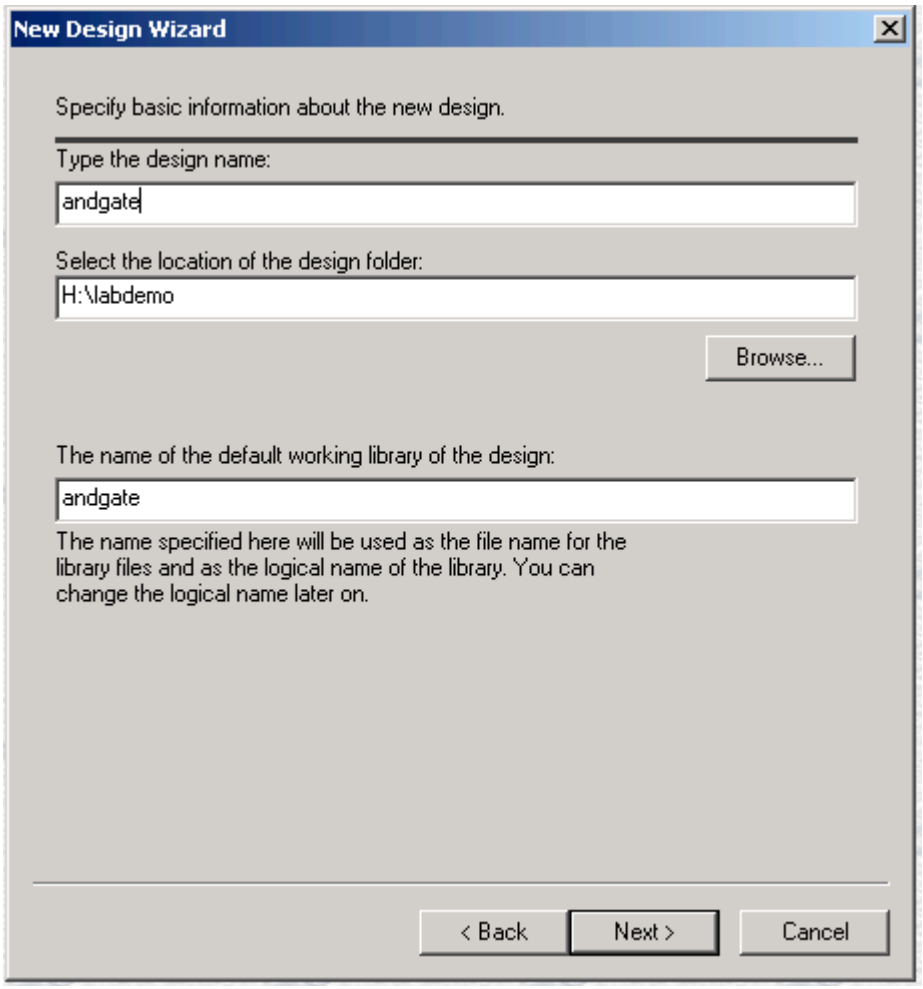
3. Select **Create an Empty Design**, and click **Next**.



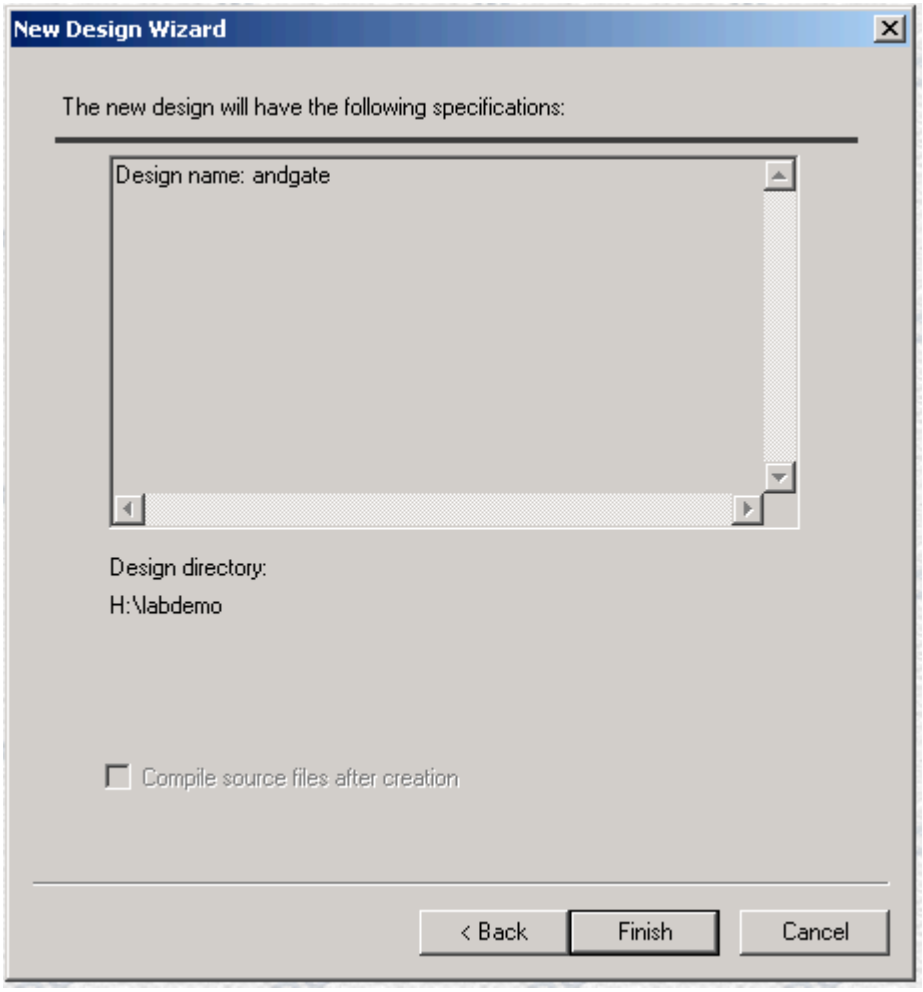
4. Choose block diagram configuration as **Default HDL language** and Default HDL language as **VHDL**; Leave the Target Technology blanks as not defined; Click **Next**.



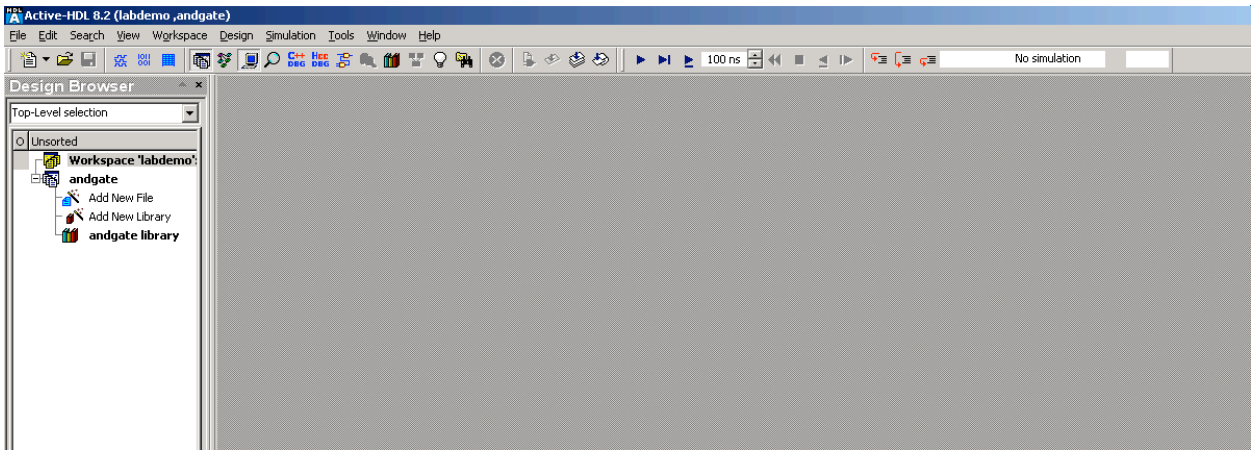
5. Type the design name you want to create and Click **Next**. For this tutorial, use “andgate” as your design name.



6. Design name and design directory will be displayed proceed further by clicking **Finish**.



7. To the left workspace and new design are displayed.



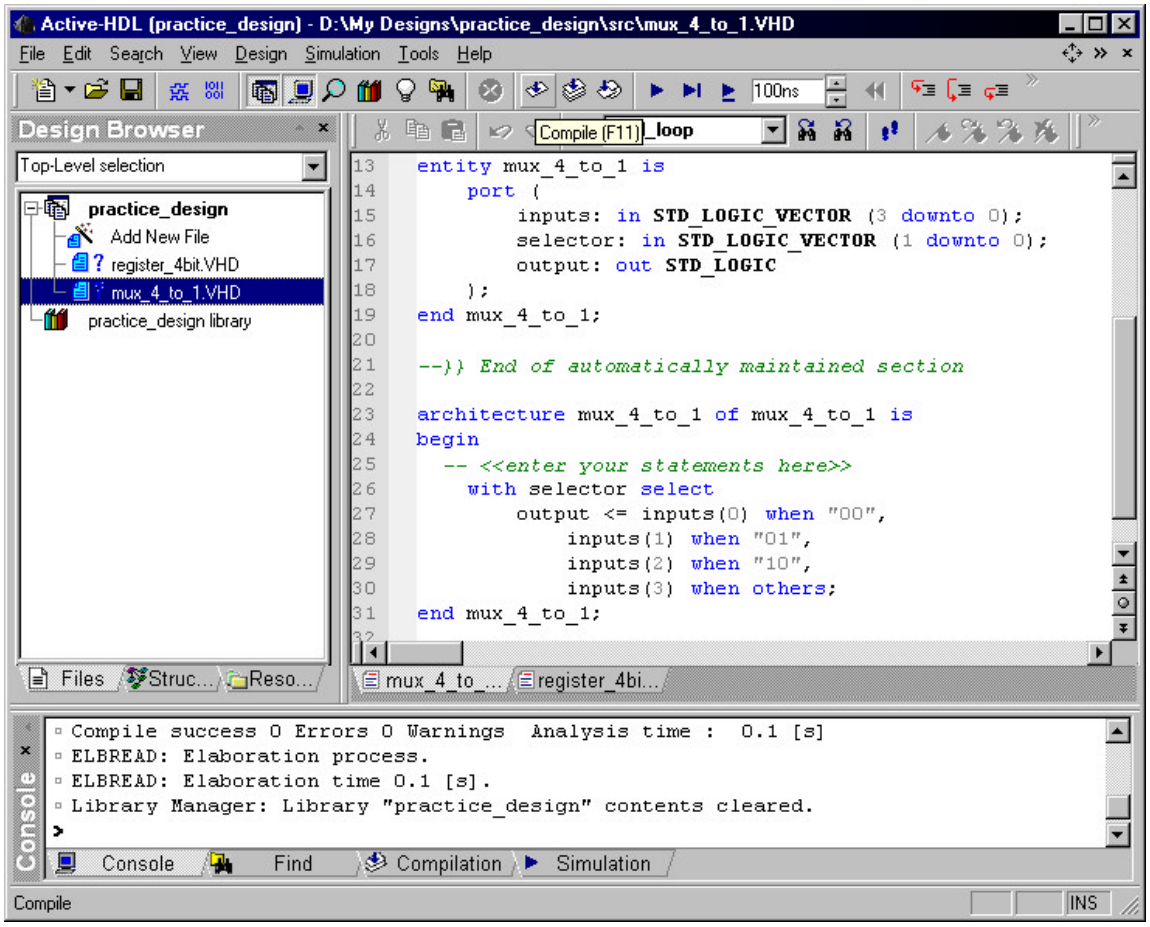
8. You can add already existing VHDL source files. To create a new VHDL source file using the source code wizard **GO TO 9**

2. Compiling designs

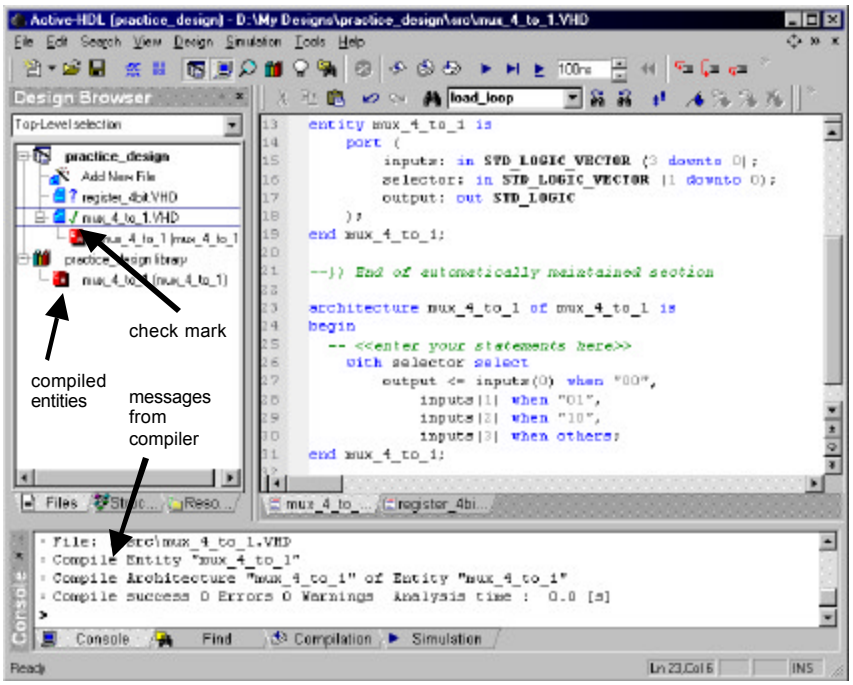
Compilation of the VHDL code is necessary to create simulation model of the described circuit. The compiler checks all the syntax and writes all the necessary information in the internal binary format. It should be clearly noted that the compiler's ability to find errors is limited to syntax errors only. Many other errors and mistakes can be found only when performing thorough simulation. It is also important to understand that the compilation does not produce any synthesized code for implementation purposes. This task is performed in Foundation Series exclusively.

2.1 Compiling selected files

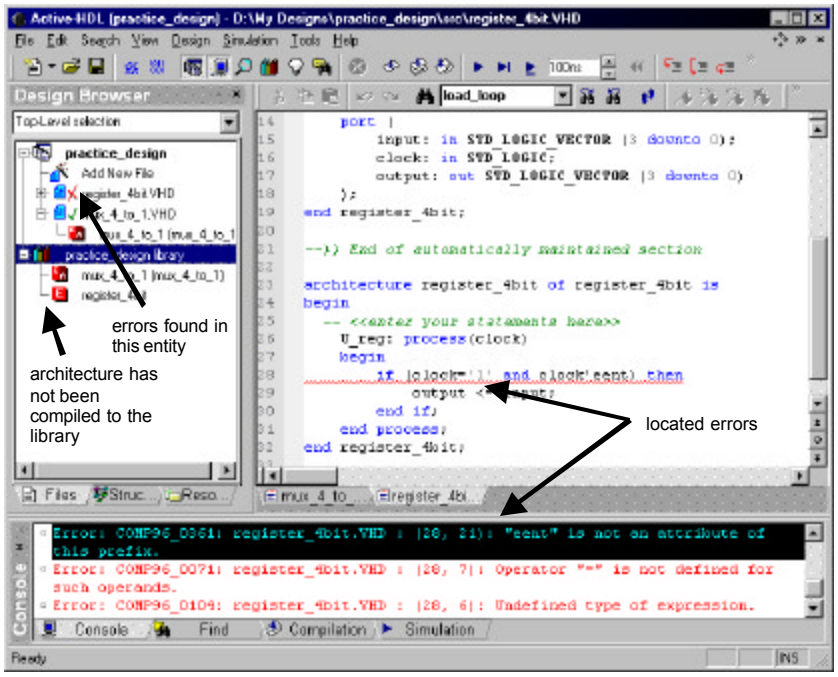
Select the file you want to compile and press button  or press F11 on the keyboard. This will start compilation.



If everything went right during the compilation, you should see check mark near your file. You can also expand the branch headed by the library icon to see that all compiled entities and architectures have been added to the project library.

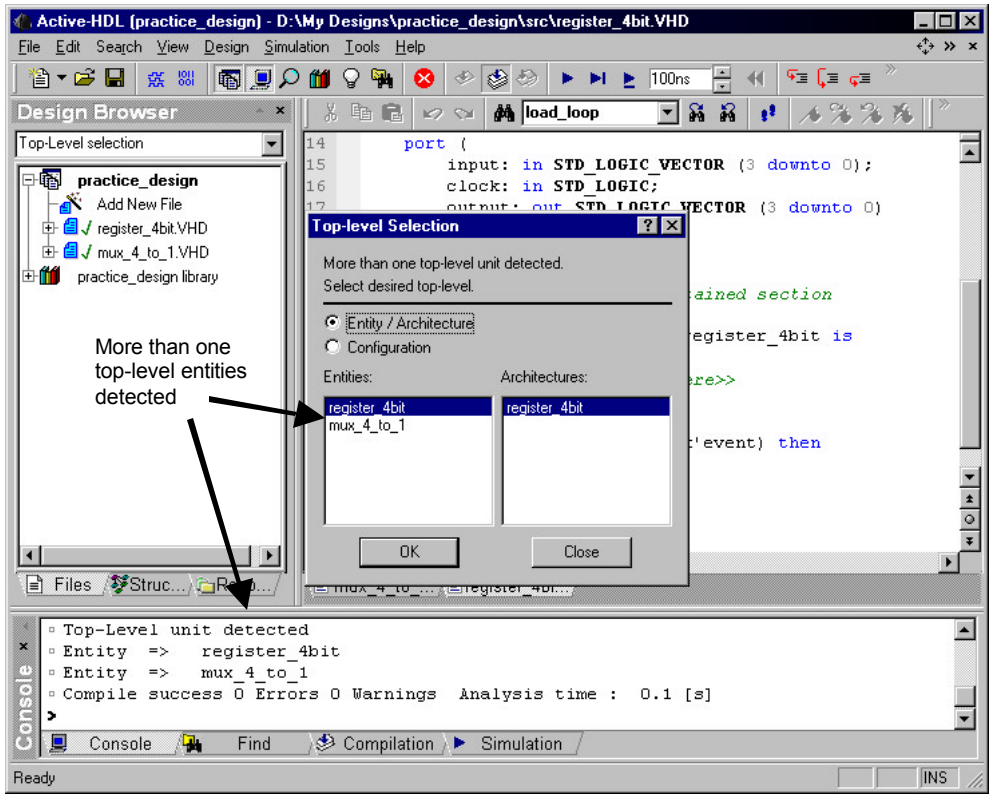


If the compilation process did not end with success, the compiler will produce meaningful descriptions of errors. All places in your code where errors were found will be highlighted.



2.2 Compiling all files

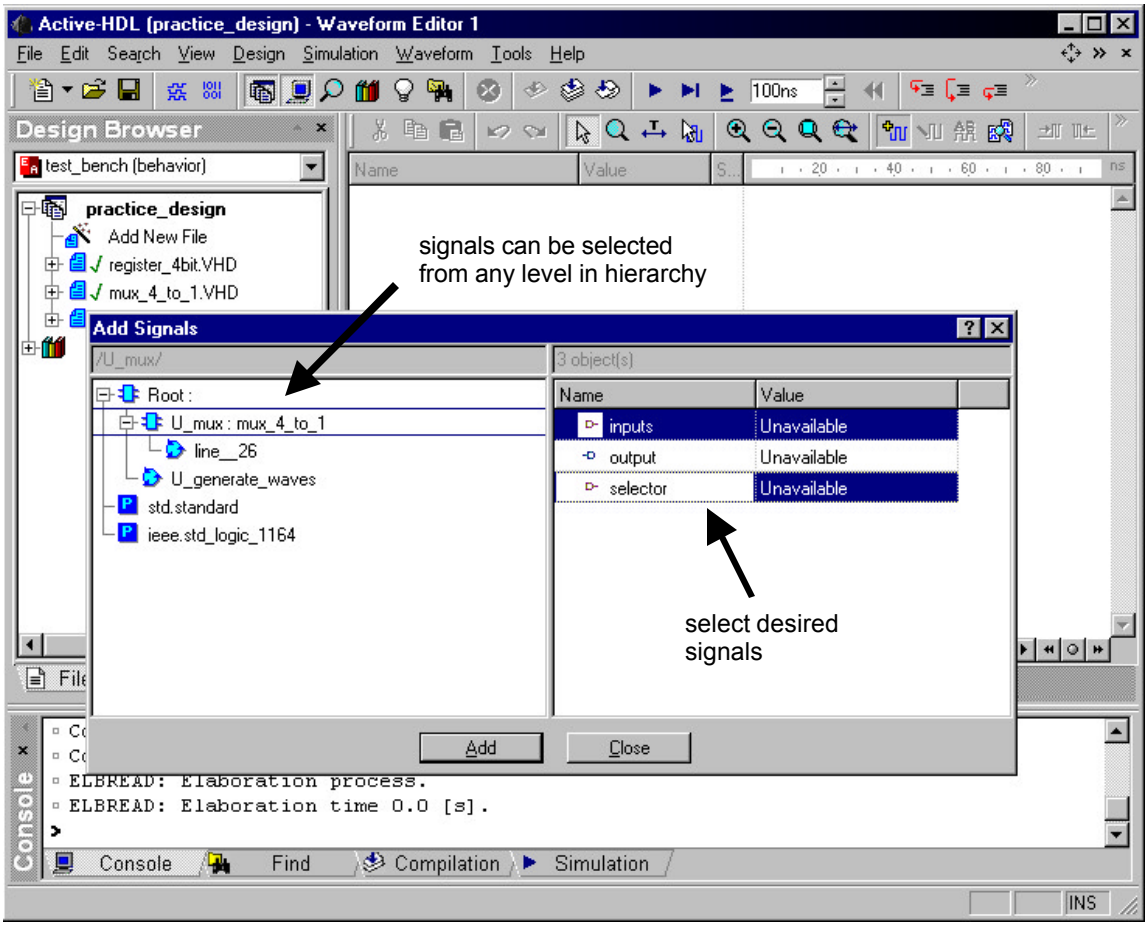
The entire design can be compiled at once by pressing buttons:  or  . If all the entities in the design are organized in the clear hierarchical structure, the compiler will automatically recognize the top-level entity. However, if distinct hierarchies of entities exist, the compiler will leave the choice of the top-level entity for you.



3. Simulating the design

Simulation can be performed when the entire design has been successfully compiled. It means that the simulation model of all elements has been created. Simulator can be configured to stimulate all inputs to the circuit, however students should learn to write test benches – top-level testers described behaviorally. The task of test bench is to produce all the stimulation to the tested circuit to verify its correctness. Once the test bench is created, performing simulation becomes an easy task.

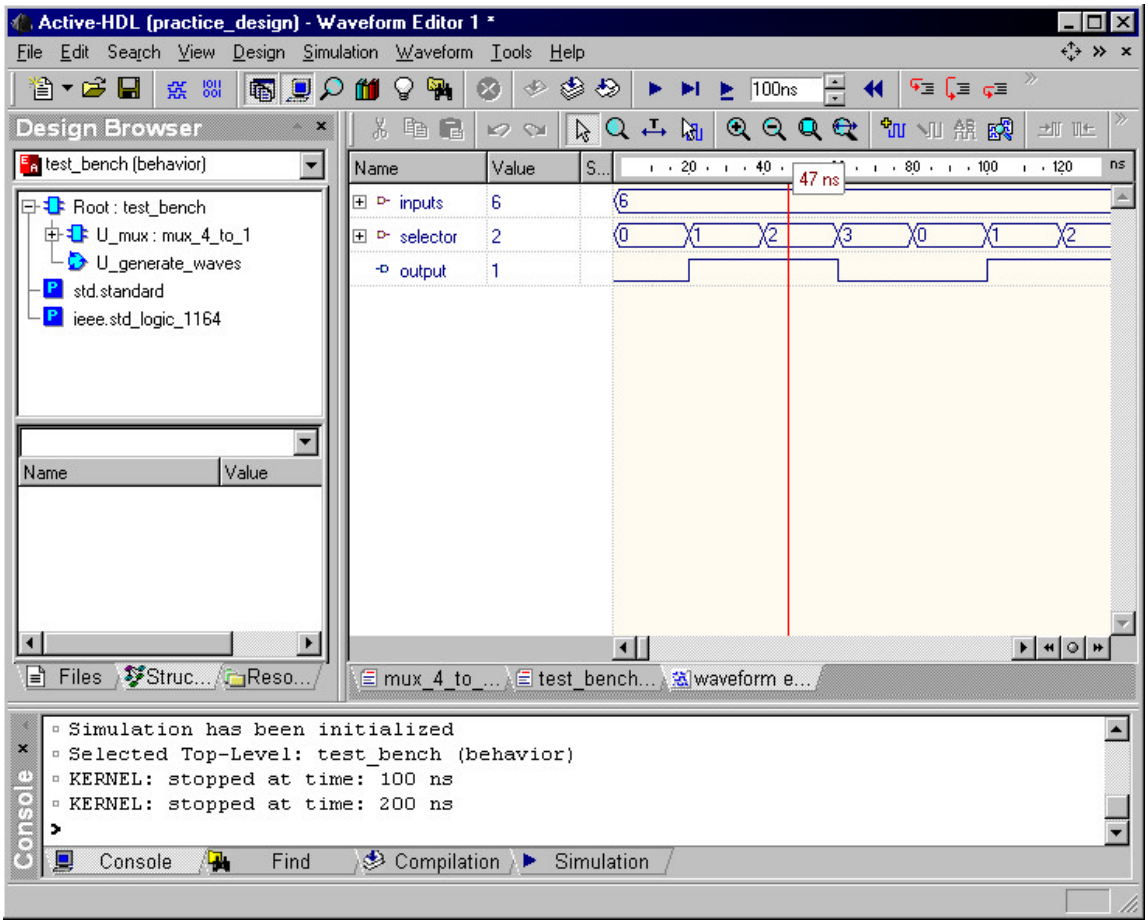
Simulation is performed in a graphical way – simulator plots waveforms of all signals being of designer's interest. To create an empty waveform click on the button  . Next add desired signals by clicking on the button  .



When you are done with adding signals, you can attempt to perform simulation. There are three slightly different ways to run it:

- by pressing button  - the simulation will run until you will stop it by pressing  .
- by pressing button  - the simulation will run until specified point of time will be reached.
- by pressing button  - the simulation will run for specified amount of time.

The result of simulation is represented in the form of waveforms.



You can always restart simulation by pressing button  .