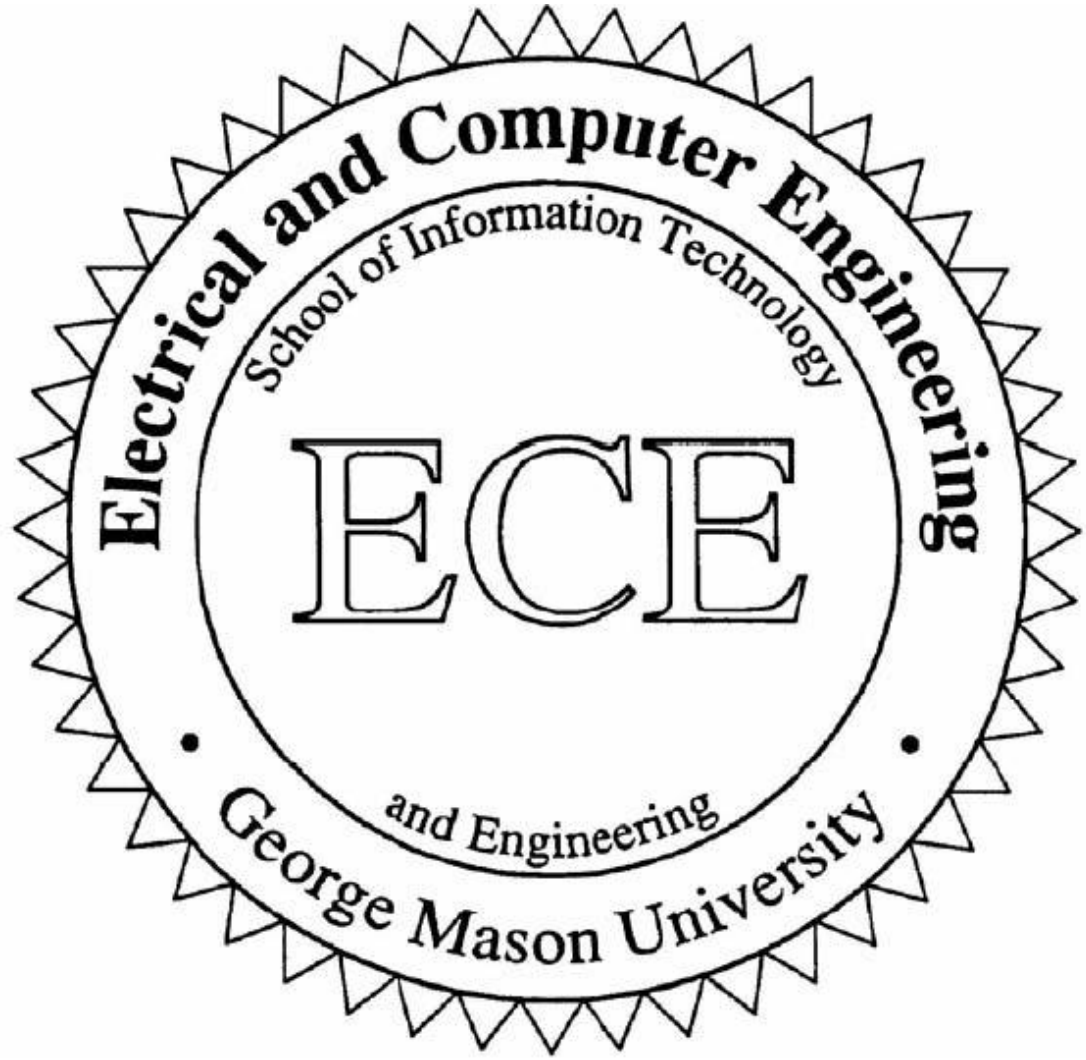
ECE 332

Digital Electronics and Logic Design Lab

Laboratory and Experiment Guide
FALL 2007



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FALL 2007

Experiment #	Date Completed	Student Signature	TA Signature
1			
2			
3			
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8			
9			
10			
11			
12			
Bonus			

Electronics Safety

Exercise of good judgment and knowledge will ensure you a safe laboratory experience.

Do not defeat any safety device such as a fuse or circuit breaker, by shorting across it or by using a higher amperage fuse than that specified by the manufacturer.

Avoid direct contact with any voltage source. Do not wear rings, watches, bracelets, or dangling necklaces while working on equipment. Do not grasp any exposed metal in your circuit when the power is on.

Keep hands dry. Water and perspiration increase conductivity.

Wear shoes with insulating soles.

Measure voltages with one hand held behind you or in your pocket.

Avoid eye injury when cutting off excessive wire lengths. Point the wires downward toward your table top so the cut pieces cannot fly toward your eyes or another person's.

Shut off the power when connecting components or test equipment to a circuit. Double check your wiring before you apply power.

Make sure your circuit is properly grounded. Beware of a possible floating ground. It is a good idea to connect all grounds together before applying power.

To prevent power terminals from shorting, keep the leads coming from those terminals apart.

Your exercise of common sense, safety precautions and knowledge will help you avoid the dangers of electricity. The amount of current required to become lethal depends upon:
1. the person involved and state of health,
2. area of the body involved,
3. length of time the shock is received, and
4. type of electrical current.

Severe electrical shock will cause burns and/or paralysis. A small current passing through the chest can kill. With even minor electrical shock, some people react by going into traumatic shock.

In case of accident, turn off power immediately and call 911. If you suspect someone is touching a "live" wire, do not touch them. Use something non-conductive to push, rather than pull, them away from the wire. An injured person should be kept lying down until medical personnel arrive, and should be kept warm to help prevent traumatic shock. Be sure nothing is done to cause further injury.

Laboratory Information

Sue Davies
Instructional Laboratories Manager
Room 120D, Science and Technology I
(703) 993-1608
email - sdavies@gmu.edu

Purchase all laboratory kits from the above. Replacement parts for all of the labs are available. Special order kits will be filled, time permitting. Room 120D houses a fairly complete inventory available to the University community. It is non profit, operated as a service to our students. It means considerable savings when purchasing parts for your Engineering senior projects. Juniors, NOW is the time to begin planning your senior project.

Also located in the Manager's Office is a reference library including data books (not available in the main library), magazines, hardware, software and equipment catalogs. There are reference books of manufacturer information (address, phone no., etc.). Magazines may be checked out. Data books may only leave the office if you first leave a deposit.

Equipment repair is handled from this office. Please notify me of malfunctioning equipment. Leave a note with symptoms or bring the equipment to my office.

All Teaching Assistants have mailboxes in ST II, in the hallway near room 208. Leave messages there, not under the lab doors. Many students use the labs and your TA likely will not receive material pushed under doors. Hand assignments and anything of value directly to the TA's since the mailboxes aren't in a secure area. Email is the best way to contact your TA. Be sure to activate your University account to receive all official notices.

Teaching Assistants' office hours will be posted in ST I on the room 2 entry way bulletin board, and room 120D entry door. In ST II, hours will be posted on the bulletin board across from room 230 (ECE office), and on the door of rooms 203 and 265. Whenever anyone is having office hours, it is also open lab time in that area.

The Engr. Computation and Test Lab needs ECE and CpE student volunteers to be Lab
Monitors. By signing up for three hours per week to open and monitor the lab, volunteers obtain a door code and priority on one of the newest computers there. They have 24 hr./day, 7days/week access. This requires serious commitment for the semester. Successful volunteers put this work on their resumes.

Laboratory Rules

1. There will be **NO FOOD OR DRINKS** in the laboratory at any time. Students will be held liable for any damage to equipment resulting from abuse of this rule.

2. Students are not allowed in the laboratories without a Lab Instructor or Lab Monitor present, unless signed in with the Lab Manager. Open lab times for make-up or project work will be posted. When a Teaching Assistant is holding office hours, he/she is also monitoring an open lab which any student may use. ECE/CpE students have priority in the Computation and Test Lab, Room 265, ST II.

3. If you suspect a problem with the equipment, notify the TA or Room Monitor. Then, leave a note on it with a brief description of the problem/symptoms, or bring the equipment to the Lab Manager, Room 120D, ST I.

4. Handle equipment with care. Equipment out for repair means less available for your use.

5. **YOU** are responsible for leaving your workstation clean and in good condition when you leave. Failure to do this will negatively impact your final lab grade.

Before leaving:

a. Hang up all test leads neatly under appropriate connector combination.

b. Tidy workstation.

c. Throw away all trash.

d. TURN OFF equipment and lab table SWITCHES.

This is a non-smoking university. This building has **NO** designated smoking areas so you must go outdoors if you choose to smoke.

Lab Tips

1. Instruction manuals for the laboratory equipment may be checked out in room 120D, S&T I. The oscilloscope manual is available for purchase in the book store. It is essential that you become familiar with the correct way to use the basic equipment in your first lab course. Wire cutters/strippers are available for sale or you may bring your own.

2. Twenty-two gauge wire (22AWG) is the best size to use with the trainers and solderless breadboards. Solid wire only, never stranded, is used. There are spools of wire cabled to the back shelf or table. You will need to cut some and strip the insulation at both ends.

Keep jumper wires short. Strive for a neat and logical layout. This will make troubleshooting easier and successful circuits more likely. (See ex. posted in lab.)

Strip no more than approximately 3/8 inch of insulation from your jumper wires. Exposed wire increases the risk of short circuits.

3. Using more than one color of wire will help you debug your circuits. Normally RED and BLACK are reserved for power and ground.

4. Probe tips should not be inserted into the solderless breadboard. Wrap a wire around your probe hook tip twice for stability and insert the other end into the connector block. Alligator clips on the equipment leads also need a wrapped wire for connection to the trainers and breadboards.

5. Always ground your probe, but keep the ground wire short. Use the method of wire wrapping described in the previous tip to attach to the alligator clip of the probe ground wire.

6. For any potentiometers (such as most multiturn) which require adjusting, a trimpot tool is available for purchase from room 120D, S & T I. It is included in appropriate kits.

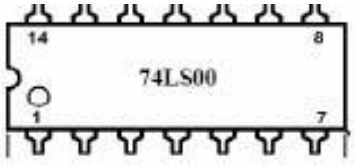
7. Most of the chips used in your lab are not overly static sensitive. However, you should observe some precautions when handling them. If you were issued a tube, it protects the chips from static charges, and is sturdy enough to provide protection to the delicate, metal pin legs.

8. Keep your chips away from magnets, motors and high temperatures. Don’t leave them in your car in the sun or extreme cold. They do best in the moderate temperatures most humans prefer.

9. Bent pins may be gently straightened with fingernails or needlenose pliers. If the pins break, you will need to purchase a new IC.

10. A small, narrow-blade, flathead screwdriver is useful in removing not so sensitive chips from breadboards. Using a side-to-side rocking motion as you insert the blade under the chip, keep a finger lightly on top of the chip to prevent it suddenly popping up on one end, bending the pins.

11. To locate pin 1 on an integrated circuit (IC, chip), look for one of the following



• A semicircle at one end, cut into the top layer of the chip - With this at the top, pin 1 is at the left of the half circle.
• A tiny spot in the corner of the chip beside pin 1 -There may or may not be other marks on the chip.
Always count pins from pin 1 around the chip so that the last pin is straight across from pin 1. Common chip sizes are 8 pin, 14, 16, 18, 20, 24, 28, and 40 pin. Your TTL ICs (Transistor-Transistor Logic Integrated Circuits) will be in dual inline packages DIP).

12. Chip leads are slightly flared to help hold them in printed circuit boards while being soldered. You will need to reduce the flare to allow them to be inserted into the breadboard. Use a pair of needlenose pliers, or press the leads against a table top, while rotating the body of the chip towards the lead points to reduce the lead angle of all evenly. The pin legs should be at a 90 degree angle to the plastic package base. Don't bend too far; there is no easy correction.

Lab Report Outline

The lab reports for the experiments in the ECE 332 Lab (as applicable) must contain the following information:

- Title Page
- Title & Number of the Experiment
- Course & Section Number
- Name
- Date
- Signed Honor Code Pledge

- Brief Description of the Experiment
- Approach used if the experiment is a word problem
- Description of the techniques (QM, K-maps etc.) used to arrive at the final logic expression

- Software Implementation of the Logic Expression
- Compiled version of the VHDL source code
- Compiled version of the test bench
- Simulation results (Timing Diagrams)

- Hardware Implementation of the Logic Expression
- List of IC chips used to implement the logic expression
- Detailed circuit diagram (including pin numbers) of the IC interconnections
- Print outs of the outputs of the experiment

- Conclusion
- Comparison between the hardware and software implementations

A lab report template and sample report (in MS Word format or PDF) can be found on the ECE 332 Administration web page.

Parts List

ECE 332 Laboratory Parts List

- 1 74LS00 Quad 2 input NAND gate
- 1 74LS02 Quad 2 input NOR gate
- 1 74LS04 Hex Inverter
- 1 74LS08   Quad 2 input AND gate
- 1 74LS10 Triple 3 input NAND gate
- 1 74LS11 Triple 3 input AND gate
- 1 74LS32 Quad 2 input OR gate
- 2 74LS73 Dual JK Flip-flop with clear
- 1 74LS86 Quad 2 input XOR
- 1 74LS151 8 to 1 Multiplexer
- 1 74LS155 Dual 2/4 Demultiplexer (Decoder)
- 1 74LS157 Quad 2 to 1 Multiplexer
- 1 74LS163 4-Bit Binary Counter
- 1 74LS283 4-Bit Adder
- 1 74C08 Quad 2-input AND gate

ALDEC ACTIVE HDL TUTORIAL

Introduction

This document is intended to assist ECE students taking ECE 331, Digital System Design and ECE 332, Digital Electronics and Logic Design Lab, in setting up their computing environment for using Aldec tools.

Active-HDL is an integrated environment designed for development of VHDL designs. The core of the system is a VHDL simulator. Along with debugging and design entry tools, it makes up a complete system that allows you to write, debug and simulate VHDL code. Based on the concept of a design, Active-HDL allows you to organize your VHDL resources into a convenient and clear structure.

Students can use Active-HDL to perform following tasks:

- development of the VHDL based designs,
- functional simulation of their code,
- functional simulation of the synthesized code,
- timing simulation of the hardware implementation.

Objective

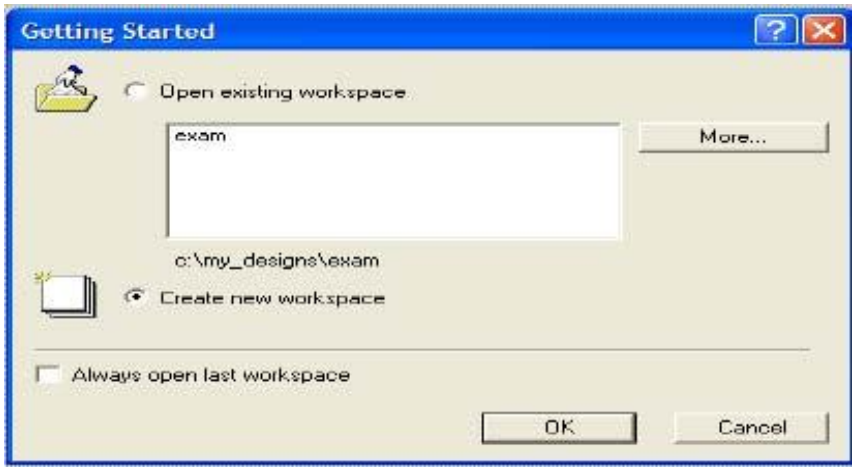
This tutorial helps you to

- Create a new design or add .vhd files to your design
- Compile and debug your design
- Perform simulation

Start-up

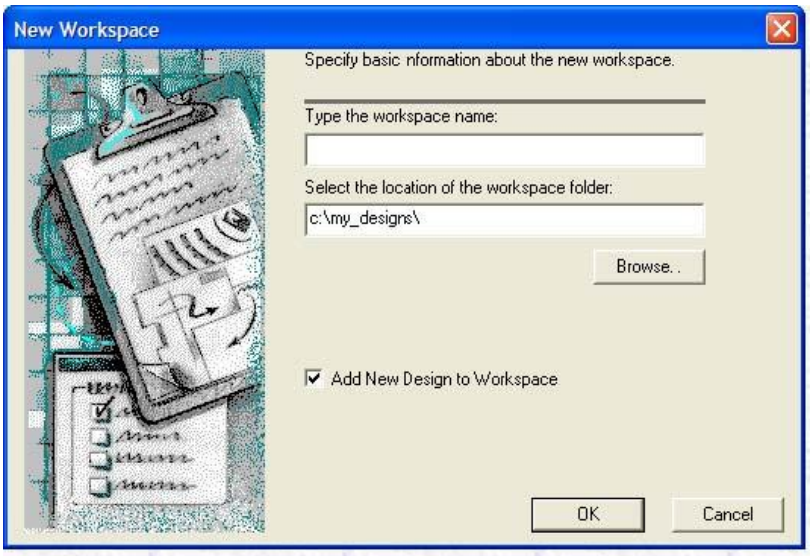
Note: Before getting started have the or3.vhd and or3_TB.vhd files downloaded from the course webpage.

1. Double click on the Active HDL icon on the desktop; it comes up with a getting started window.

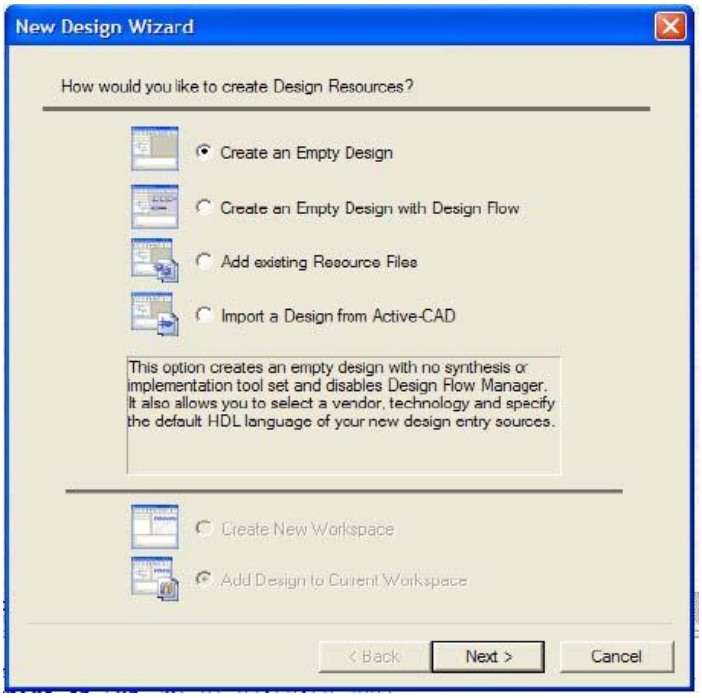


a. Select **create new workspace** and click **OK**, creates new workspace in your directory.
b. Selecting **open existing workspace** gives you the option to choose from your previous Workspace's.
c. Always open last workspace takes you to the last workspace.

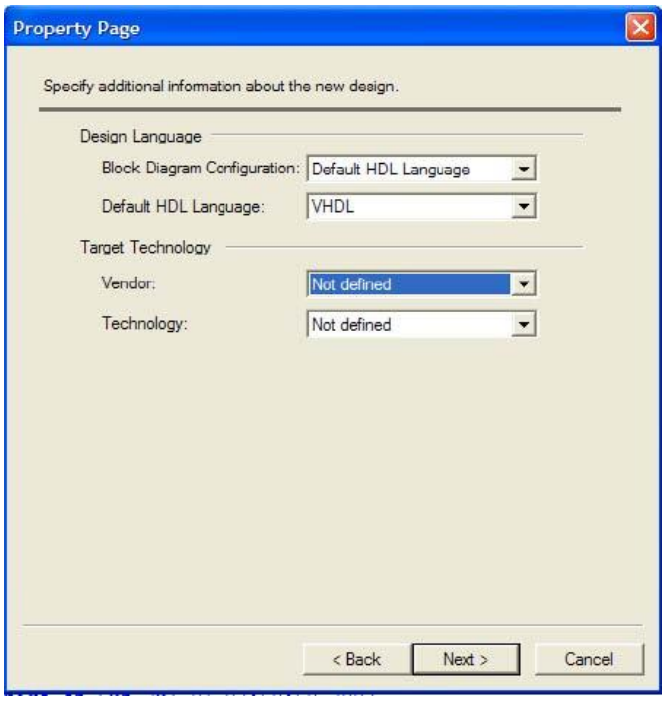
2. Type the workspace name you want to create and click **OK** and the default location of your workspace will be your **network drive\my_designs.**



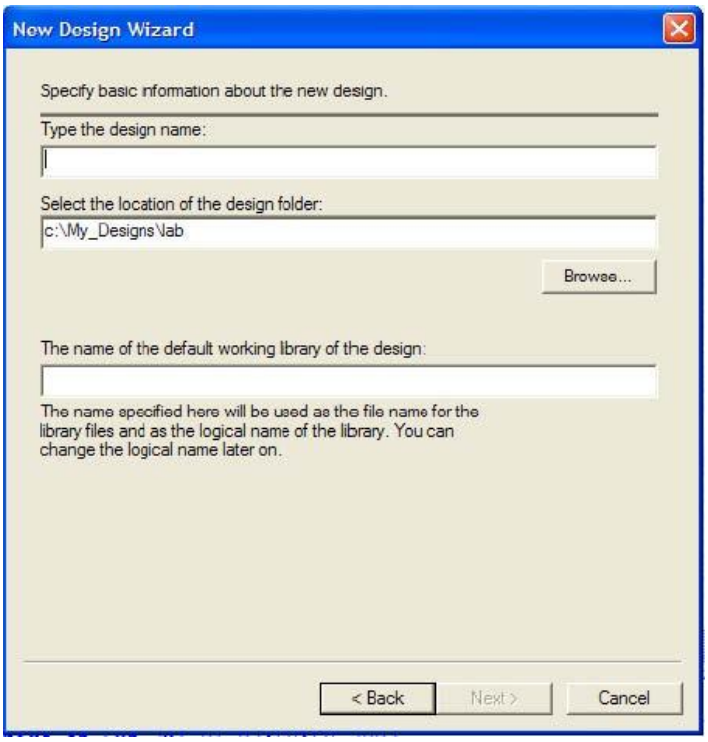
3. Select **create an empty design**, creates a new design in your workspace and click **Next.**



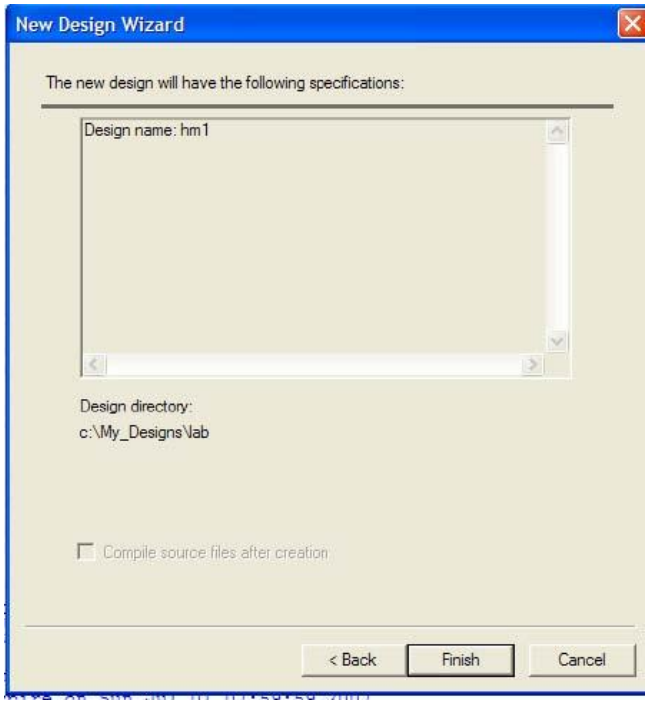
4. Choose block diagram configuration as **Default HDL language** and Default HDL language as **VHDL**; Leave the Target Technology blanks as not defined; Click **Next.**



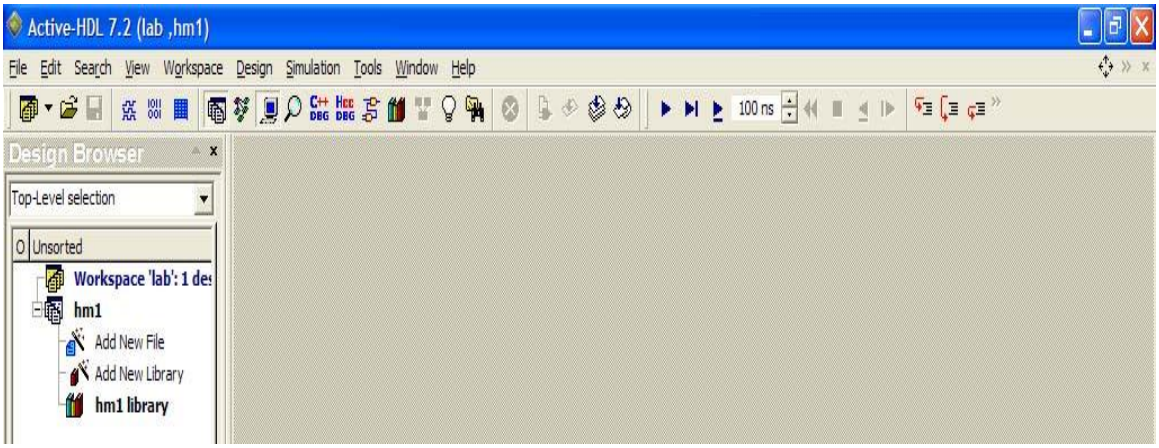
5. Type the design name you want to create and Click **Next** and the default location of your design will be your **network drive\my_designs\workspace name. "lab"** is just a placeholder for any workspace name you typed in at step 2.



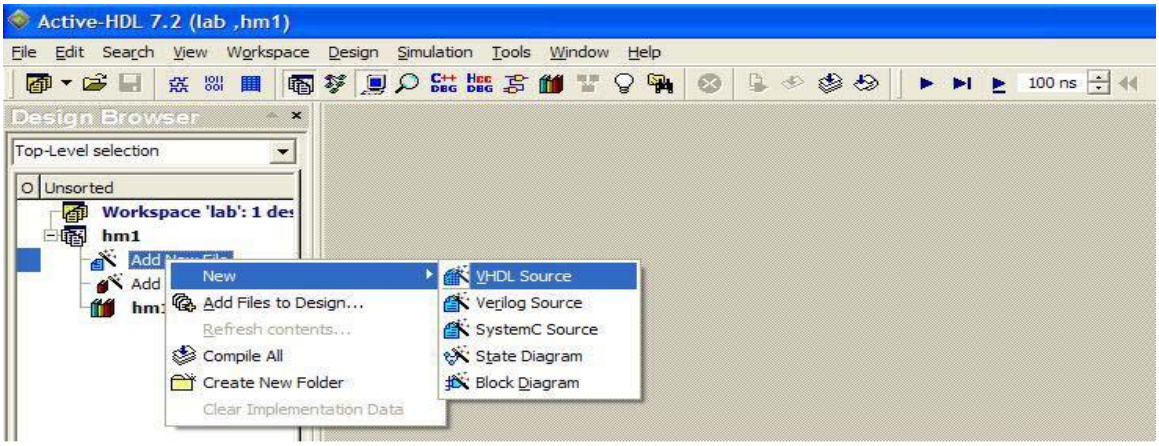
6. Design name and design directory will be displayed proceed further by clicking **Finish. "hm1"** is just a placeholder for any design name you typed in at step 5.



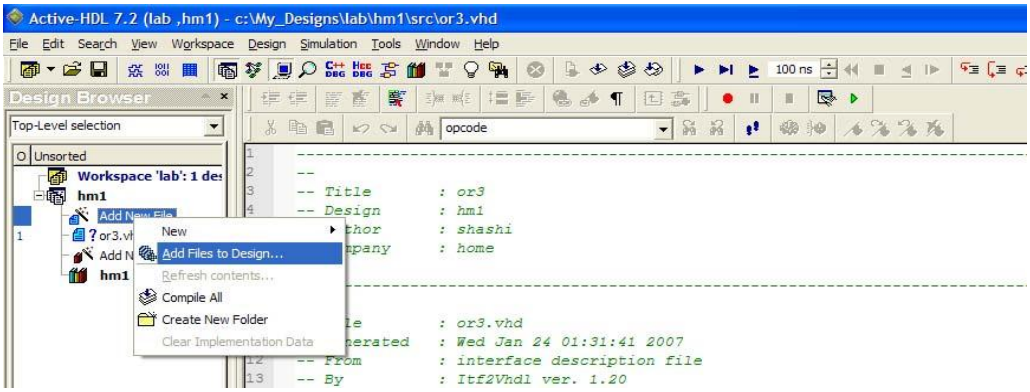
7. To the left workspace and new design are displayed.



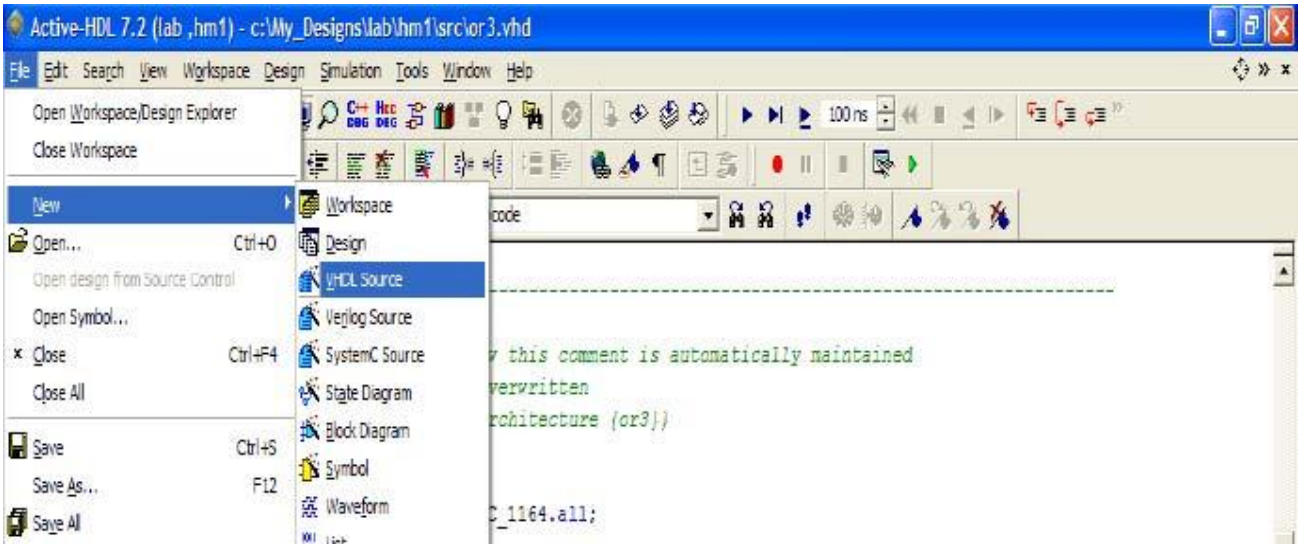
8. To start with your VHDL source right click on **Add New File > New > VHDL source,** then **GO TO 9.**
To add existing files to your design **GO TO 8A.**



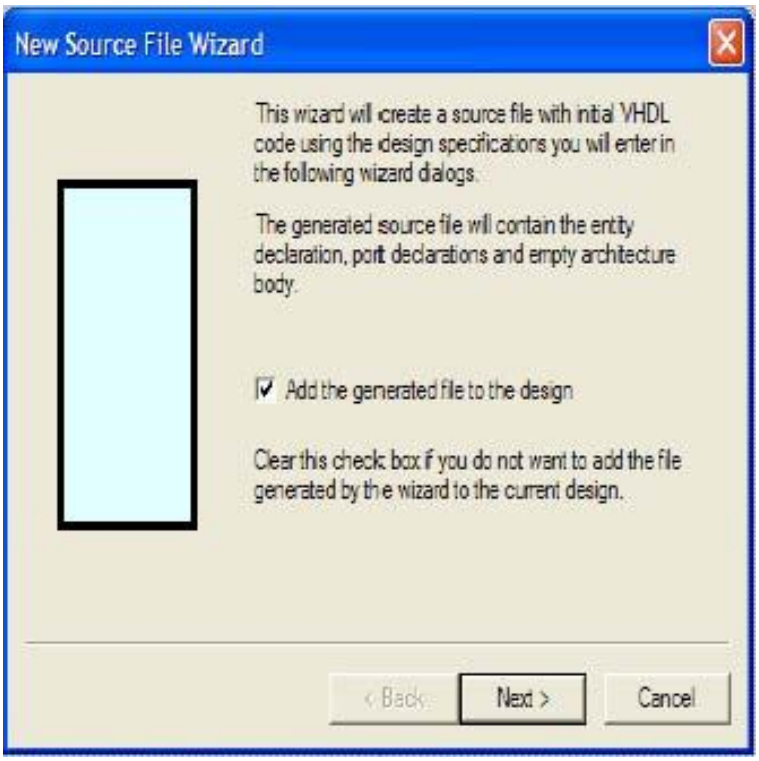
8A. To add existing files to your design, select **Add New File> Add Files to Design.**



8B. New VHDL source can also be added by following up **File > New > VHDL source.**



9. Click **Next** on the new source file wizard.



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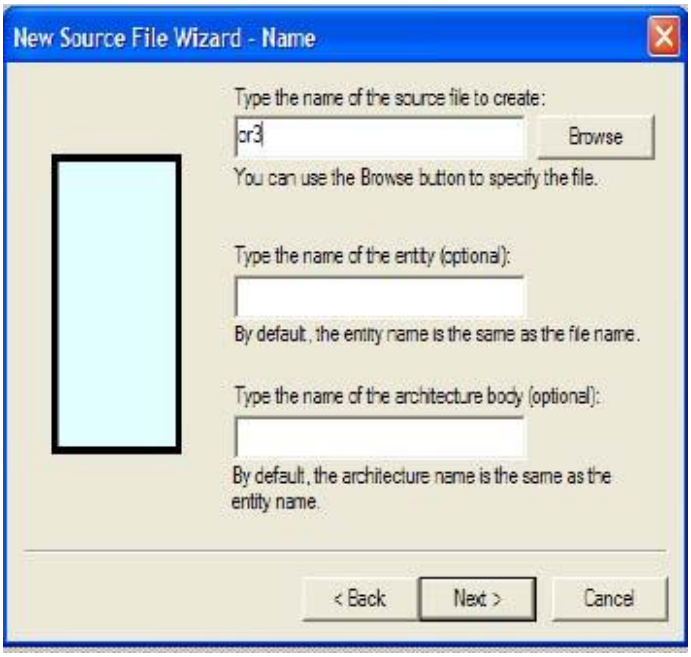
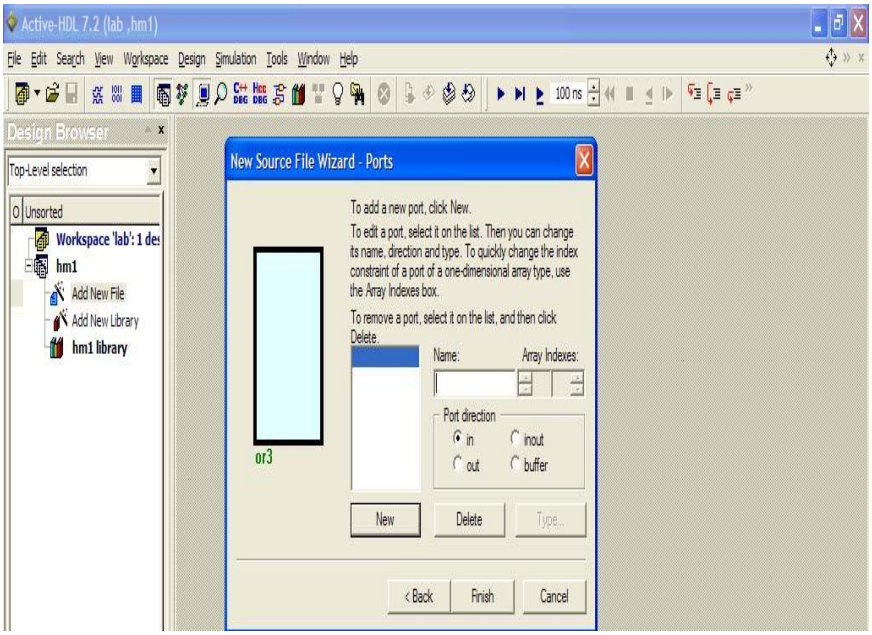
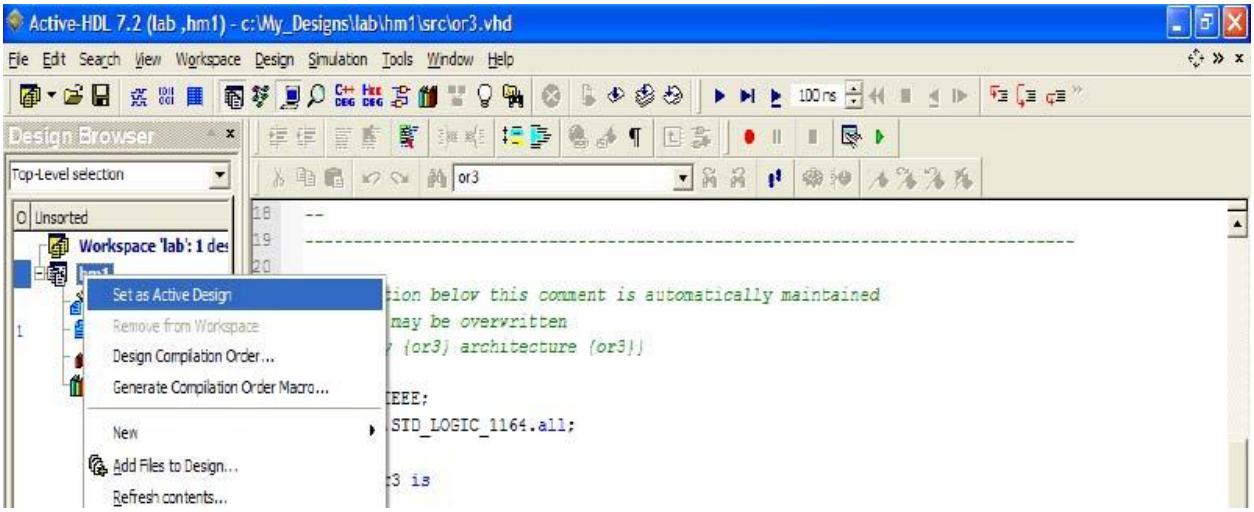
10. Type the source file name you want to create; you can choose to give a different name for entity and architecture else the default name for entity and architecture will be your source file name. Click **Next. "or3"** is just a placeholder for any source file you want to create, but for now type in "or3" to go ahead with this tutorial, follow up with the rest to get to an "or3" gate.



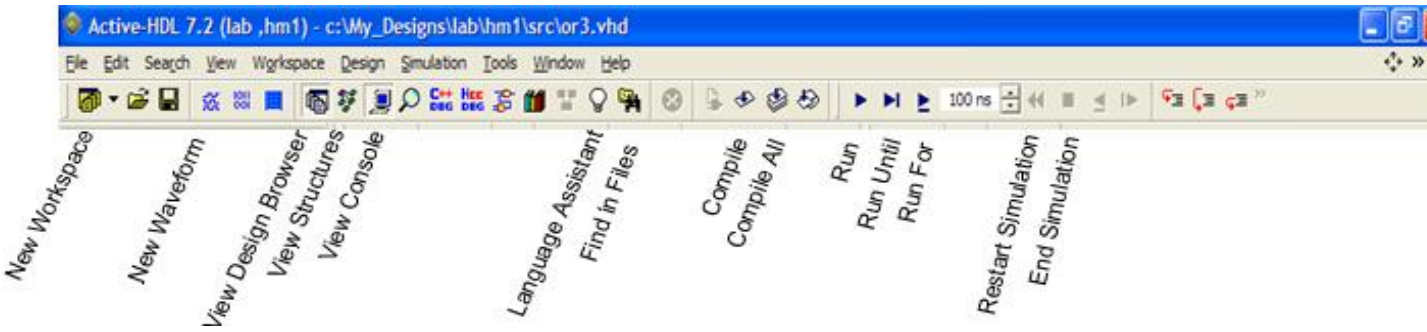
11. Select **New** in the New Source File Wizard-Ports, start declaring your input and output ports by naming them, choosing the port direction, choose the type by indicating the array indexes. Click **Finish**.



12. If you have multiple designs in the same workspace you need to set an active design and this can be done by a right click on your design and select **Set as Active Design.**



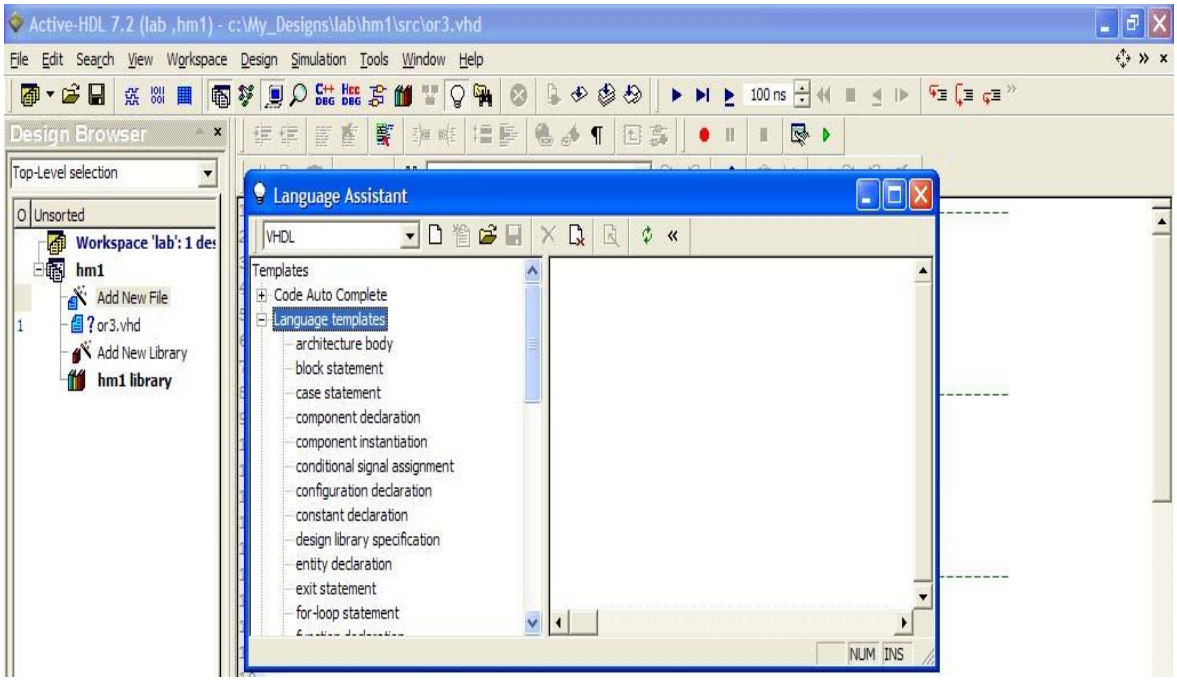
Main Window Toolbars



New Workspace	Enables you to craete a new workspace
New Waveform	Enables you to create a new waveform
View Design Browser	Lists the files in your design, can be seen to the leftmost corner
View Structures	Lists the availabe signals in your design, can be seen to the leftmost corner
View Console	Display screen, can be seen at the bottom
Language Assistant	Helps you with the syntax of VHDL data types
Find in files	Search engine with in your design
Compile	Compiles the design file selected
Compile All	Compiles all the files in your design
Run	Runs the simulation until you stop
Run Until	Runs simulation until specified point of time is reached
Run For	Runs simulation for specified amount of time
Restart Simulation	Reloads the design and resets the simulation time to zero
End Simulation	Stops simulation

Comment	Comments the selected portion of your code
Uncomment	Uncomments the selected portion of your code

- **Language Assistant** helps you with the syntax of the VHDL data types.

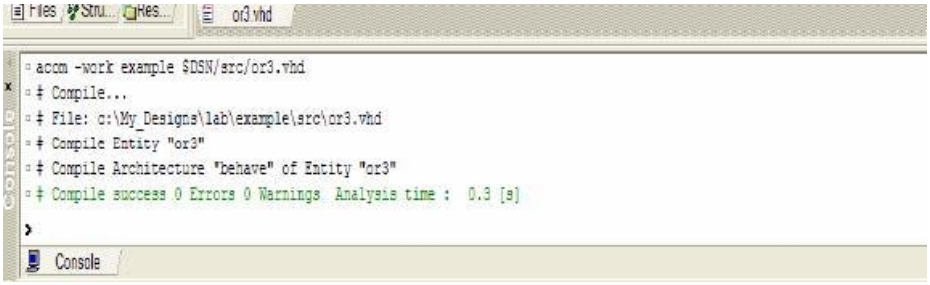


Compiling the Design

- Once the design is ready, compile it either by clicking on the toolbar as shown or hit **F11** or choose **Design > Compile.**

Console window

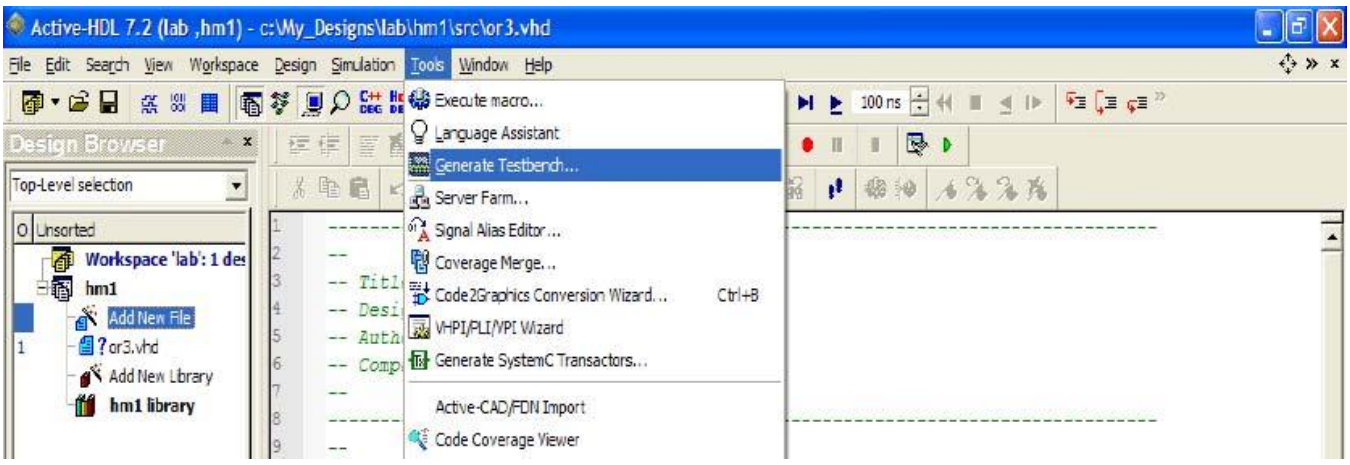
- Console window appears at the bottom of the page with a **success** message if design is free of errors.



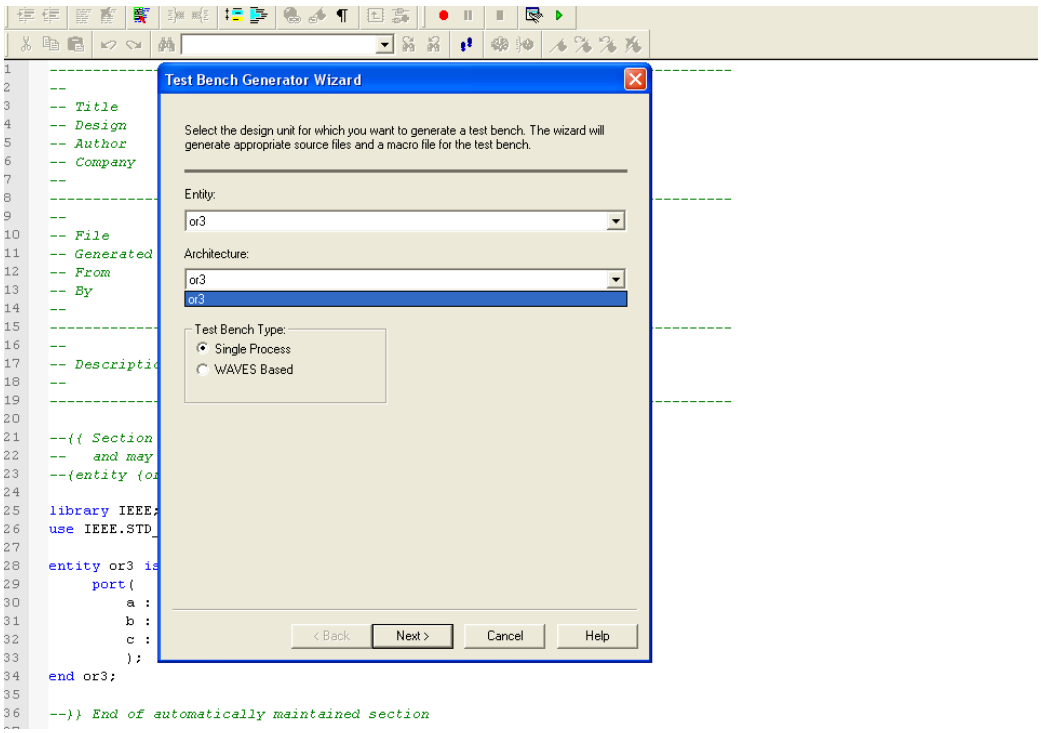
Generating Testbench

NOTE: To add your testbench, click **Add New File>Add Files to Design** as in 8A.

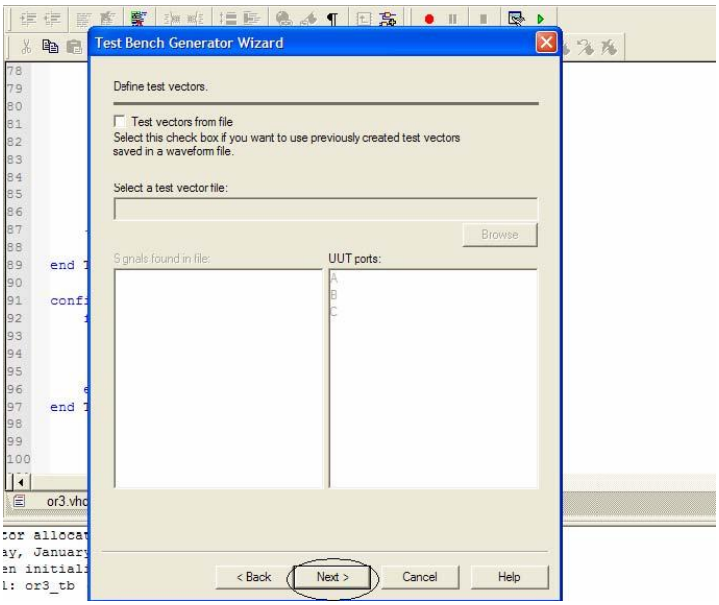
- Testbench is a .vhd file that applies stimulus to your design in order to analyze the results or to Verify the functional simulation of your design.
- Once your design is compiled, Testbench can be generated as **Tools > Generate Testbench.**



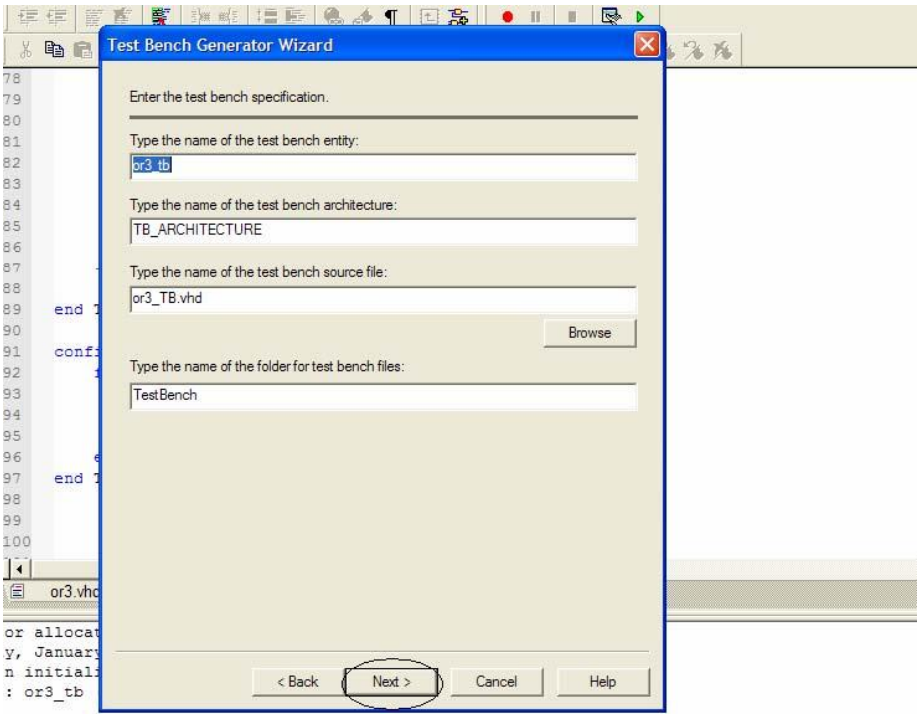
- Select the Design Unit (Entity and Architecture names of your design for which Testbench has to be generated from the drop down menu as shown below).
- select testbench type as **Single Process;** Proceed by clicking **Next.**
- In start up step 10 we chose entity & architecture name to be default as source file name Which is “or3”, if they are different from or3 select appropriate one from the drop down list.



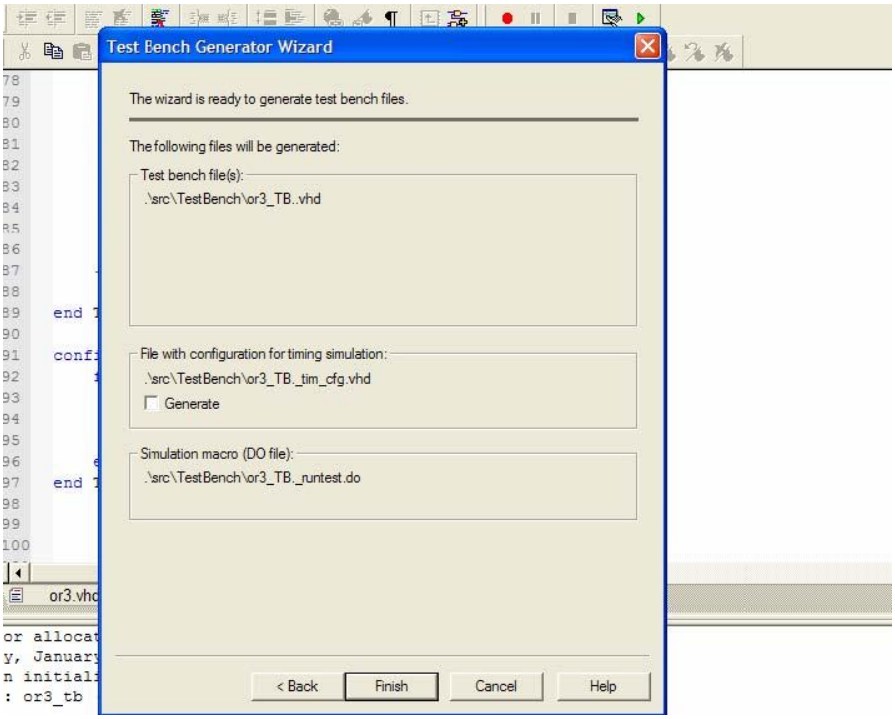
- Testbench generator wizard appears with all your input ports under UUT (Unit under test) ports.
- Proceed by clicking **Next.**



- Click **Next** as the tool generates the names for all the design units, you can change them (Not Recommended).



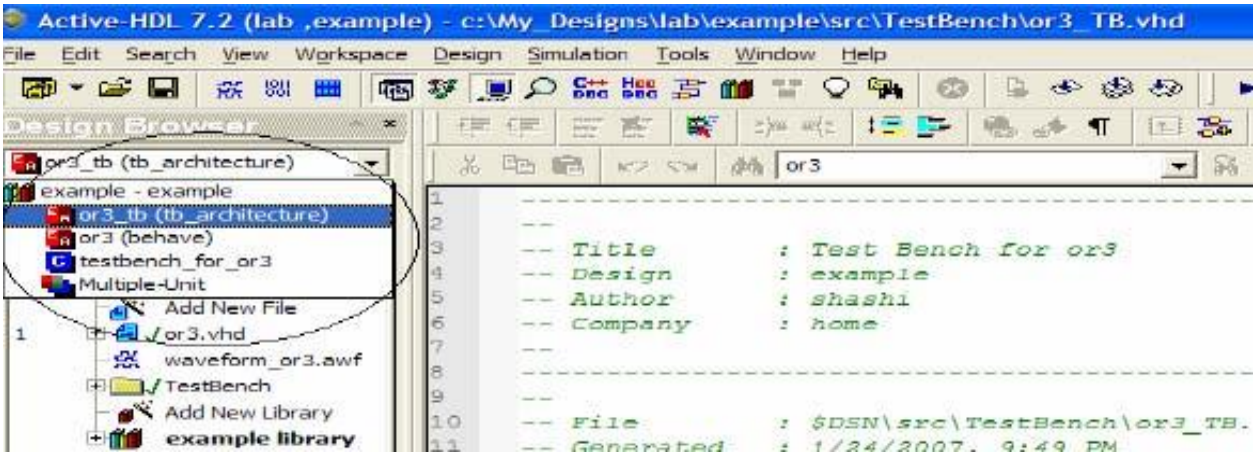
- Click **Finish** to proceed, the window below shows the files generated by the Testbench.



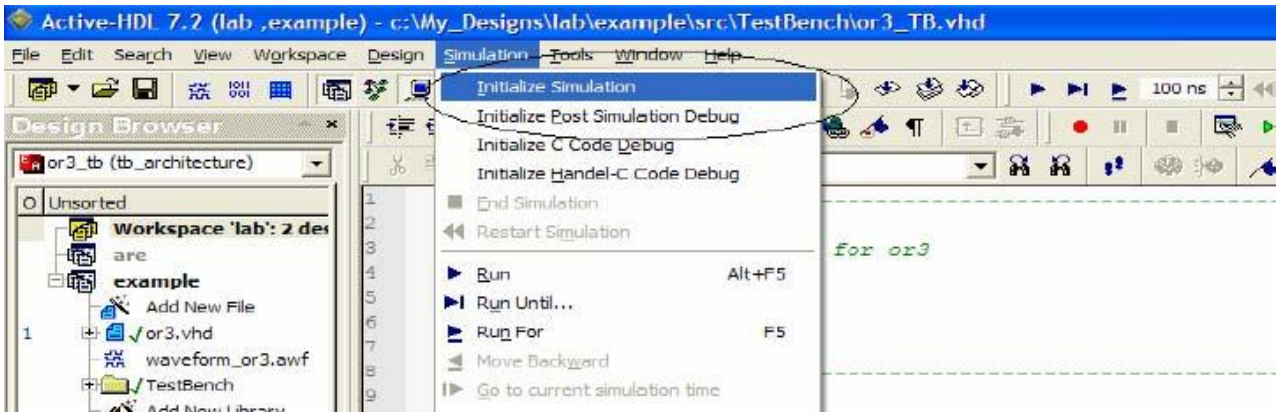
NOTE: Add your test conditions to the Testbench, **Hit F11** to compile.

Getting Started with the Simulation

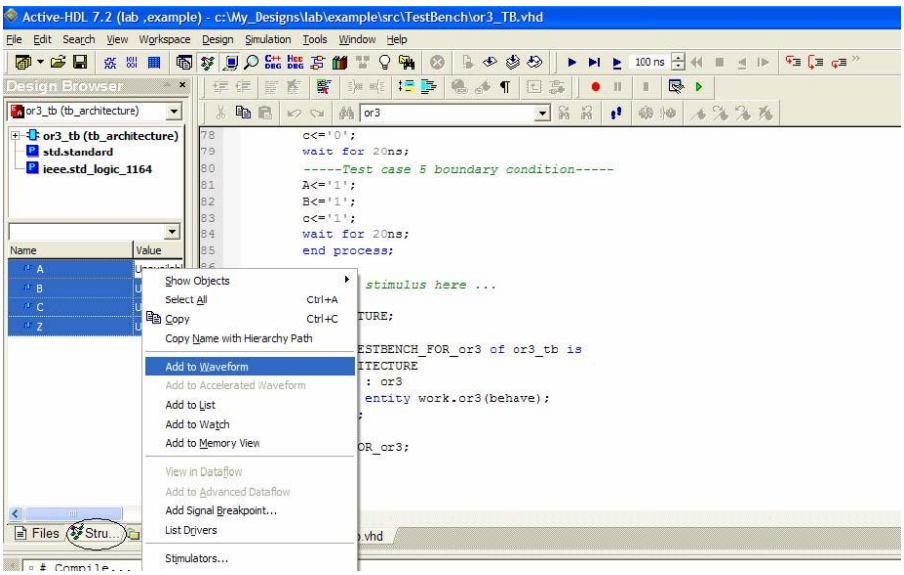
- Simulation allows you to test the behavior of your design under the given input conditions and specifications.
- Once your design files (source code & testbench) are compiled without any errors, select the **Top level** unit as your testbench as shown below in the design browser.



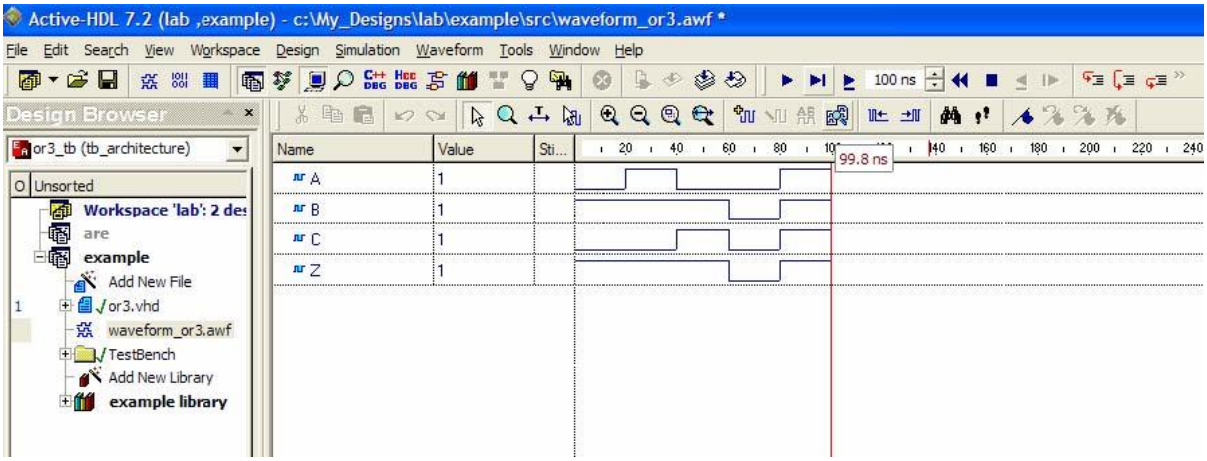
- Initialize simulation by selecting **Simulation > Initialize Simulation.**



- Click **Structures** (circled below) to see all the ports, select all the signals you want to add to a waveform, right click on the signals selected and add them to the waveform as shown below.



- Hit F5 to run or select **Simulation > Run For.**



Wave Window Toolbar

Zoom in	Zoom in from the current view
Zoom out	Zoom out from the current view
Zoom to fit	Zoom to fit the screen
Add signals	Adds signals to your waveform