KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
DEPARTMENT OF ELECTRICAL ENGINEERING

EE 200 DIGITAL LOGIC CIRCUIT DESIGN

EXAMINATION II

May 17, 2007

NAME :	
I.D. # :	
SECTION :	

PROBLEM #	SCORE	MAXIMUM
1.		25
2.		25
3.		25
4.		25
TOTAL		100

Q # 1)

Simplify the following function and implement it using

(i) NOR gates only
(ii) NAND gates only
(iii) OR-NAND
(iv) AND-NOR

$$F(w,x,y,z) = wx' + y'z' + w'yz'$$

Q.# 2)

a. Design a combinational circuit incrementer. (a circuit that adds one to a 3-bit binary number x, y, and z). Determine the required number of outputs (assign letters A,B,C,… for the outputs). Simplify the output functions Use Karnaugh maps and draw the logic circuit.

b. Design the circuit in (a) using a ROM. Determine the size of the ROM and its truth table.

Q # 3)

Design a combinational circuit that implements the following Boolean functions:

$$\boldsymbol{F_1(A,B,C,D) = A'BC' + ABC'D' + ABC' + A'B'C + AB'C}$$
$$\boldsymbol{F_2(A,B,C,D) = \Sigma(0,1,6,7,9,14,15)}$$

1. using a decoder and OR gates
2. Using a PLA with the minimum number of product terms. Determine the size of the PLA and its program table.

Q # 4)

a. Implement the following four variable function using an 8X1 multiplexer. Connect the variables <u>A, B, and C</u> to the selection lines S_2, S_1, and S_0 respectively.

$$F(A,B,C,D) = \sum(3,4,6,9,11,12,13,14,15)$$

b. AN 8X1 multiplexer has inputs <u>B, C, and D</u> connected to the selection lines S_2, S_1, and S_0 respectively. The data inputs I_0 through I_7 are as follows: $I_1=I_2=I_7=0$; $I_3=I_5=1$; $I_0=I_4=A$, and $I_6=A'$. Determine the Boolean function that the multiplexer implements in a sum of minterms form.
