**KING FAHD UNIVERSITY OF PETROLEUM & MINERALS**
**DEPARTMENT OF ELECTRICAL ENGINEERING**

EE 200 EXAMINATION

# DIGITAL LOGIC CIRCUIT DESIGN

**EXAMINATION TYPE:** Major Examination II

**DATE**: December 17, 2005

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| **Student's name:** | |
| **I. D. #:** | |
| **Section:** | 03 |

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| **Total** | **/ 100** |

***Instructor: Dr. Mahmoud M. Dawoud***

***Q.1)***

Design a combinational circuit that implements the following Boolean functions using a decoder and OR gates.

$$F_1(w,x,y,z) = w'xy + wy'z' + wx'$$
$$F_2(w,x,y,z) = \Pi(0,1,2,3,5,6,7,8,9,13)$$

***Q.2)***

a. Design a logic circuit that will add one to the decimal equivalent of a 3 bit input binary number(x,y,z) if the number is even. If the number is odd, three will be added. Determine the required number of outputs and call them (A, B, …etc.). Obtain a minimal expression for each output and draw the logic circuit using only NAND gates. Use Karnaugh maps for simplification.

b. Design the circuit in (a) using a ROM. Determine the size of the ROM and its truth table. Do not include any output that is equal to an input.

***Q.3)***

Construct the PLA program table to implement the following functions:

$$f_1(A,B,C,D) = \sum m(0,1,4,5,8,9,13)$$
$$f_2(A,B,C,D) = \sum m(2,3,6,7,8,10,11,12)$$

Realize the functions such that the number of product terms is minimised.

***Q. 4)***

Analyse the clocked sequential circuit below, by finding:

i. The flip-flop input functions
ii. The output functions
iii. The state table
iv. The state diagram