Ne Realizations of CMOS Current Controlled Conve ors ith ariable Current Gain and Negative Input Resistance

S. M. Al-Shahrani and M. A. Al-Absi

Department of Electrical Engineering,

King Fahd University of Petroleum and Minerals

Box 185, Dhahran 31261, Saudi Arabia **saadms fupm.edu.sa**

Abstract- *In this paper two new second-generation current controlled current-conveyors (CCCIIs) – based circuits are proposed. The proposed circuits are variable gain CCCII and CCCII with negative resistance. The design of these circuits is based on a simple CMOS CCCII that has high bandwidth with -3 dB cutoff frequency of 580 MHz. With no signal mirroring used in these configurations, lower harmonic distortion can be achieved. HSPICE simulation results for the proposed circuits are included.*

I. Introduction

The current conveyor is considered one of the most useful active devices for analogue signal processing. This is attributed to its high performance, particularly linearity and bandwidth. The current conveyor was used extensively to realize useful applications, like active filters, oscillators, and immittance function simulators.

Another version of the CCII is the current controlled current conveyor (CCCII). It exhibits the same features of the CCII plus the controllability. It has been realized in different technologies, BJT, CMOS, and BICMOS [1-5]. At present, there is a growing interest in using the CCCII in various analogue signal processing applications [6-10].

This paper presents new implementations for variable gain CCCII and CCCII with negative resistance. HSPICE simulation results which confirm the analysis are given.

II. Circuit Description

Fig. 1 shows the circuit diagram of the core circuit used in the design of the proposed applications. In fact, this structure was first introduced as simplified current-conveyor (CCII-) with poor voltage tracking coefficient between terminals x and y compared to other modified structures [11]. However it shows an excellent current following behavior between port X and port .

Using small signal analysis, it can be easily proven that the voltage difference $_{xy}$ can be described as:

$$_{xy} = i_x r_x \qquad (1)$$

where

$$r_x = 1/g_{m3} \quad 1/g_{m4} \qquad (2)$$

g_{mi} is the transconductance of transistor i and is given by:

$$g_{mi} = \sqrt{2 \;_{n}(\; / \;)_i I_B} \qquad (3)$$

Equation (1) indicates that this structure can be considered as a CCCII which exhibits an intrinsic controlled resistance r_x. Equations (2) (3) show that r_x is inversely proportional to the square root of the bias current I_B. The CCCII characteristic can be modeled as:

$$\begin{matrix} i_y \\ v_x \\ i \end{matrix} = \begin{matrix} 0 & 0 & 0 \\ 1 & r_x & 0 \\ 0 & -1 & 0 \end{matrix} \cdot \begin{matrix} v_y \\ i_x \\ v \end{matrix} \qquad (4)$$

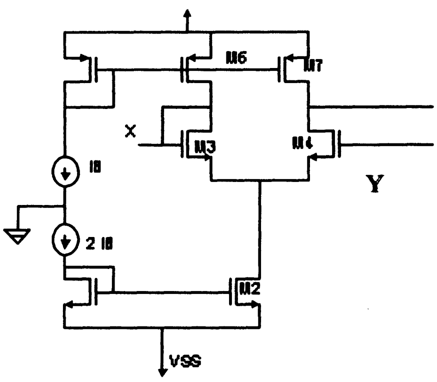


Figure 1
Circuit diagram of the CMOS CCCII

The CMOS CCCII circuit was simulated using the HSPICE to verify its performance. The simulations are based on 1.2 m BSIM3V3 CMOS models made available through MOSIS (AMI). The transistors aspect ratios used are: M_1 = M_2 =18/9 m, M_3 = M_4 =150/1.2 m and M_4 = M_6 = M_7 =10/10 m. The supply voltages are V_{DD} = -V_{SS} = 2.5V.

0-7803-8294-3/04/$20.00 ©2004 IEEE

The short circuit current gain frequency response i i_x of the CCCII is shown in Fig. 2. As depicted from this figure, it has -3 dB cutoff frequency at 580 MHz. Fig. 3 compares the calculated and simulated r_x at different values of the bias current I_B. This shows a good agreement between them over a wide range of I_B.

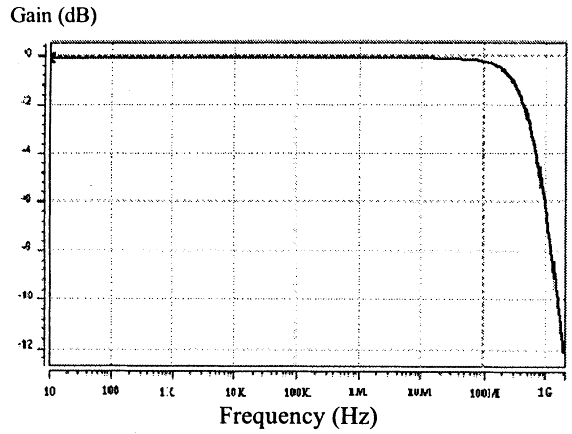


Figure 2

Current gain characteristics i / i_x

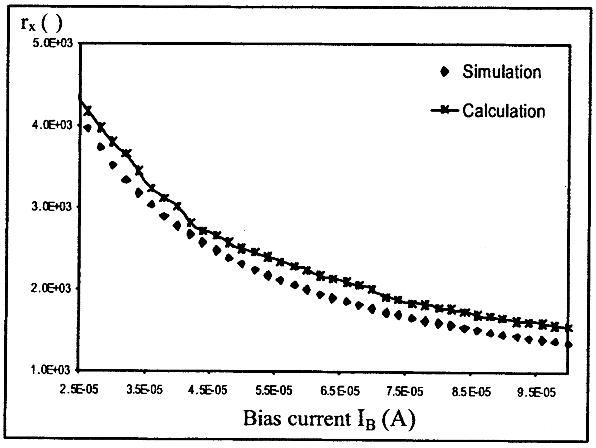


Figure3

Resistance r_x as function of the bias current I_B

III. Proposed Circuits

Simplicity and potential performance of the above circuit make it very attractive to be used as a core circuit in the proposed applications as will be shown in the following subsections.

1. ariable gain CCCII

Variable gain current conveyor can be implemented using two active devices (OPAMPs or CCIIs) and resistors [12], [13]. In this paper a variable current gain current controlled conveyor based on the simple CCCII is presented. The circuit diagram of the proposed variable gain CCCII is shown in Fig. 4. The operation performed by this circuit is described by:

$$\begin{matrix} i_y \\ v_x \\ i_1 \end{matrix} \quad \begin{matrix} 0 & 1 & 0 \\ 1 & r_x & 0 \\ 0 & -1 & 0 \end{matrix} \cdot \begin{matrix} v_y \\ i_x \\ v \end{matrix} \qquad (5)$$

and

$$i_3 = -i_2 = i_x \qquad (6)$$

where

$$k = [(g_{m3}^{-1} \quad g_{m4}^{-1})/(g_{m13}^{-1} \quad g_{m14}^{-1})] \qquad (7)$$

From equation (7), and assuming M3, M4, M13, and M14 are matched transistors the current gain is equal to $\sqrt{I_B/I_A}$. One advantage of this circuit, it realizes both positive and negative variable current gain CCCII simultaneously. Fig. 5 shows plots of the currents i and i versus the current i_x at different values of the bias current I_A. It is clear from the plots that, the current gain, k, can be controlled by varying the bias currents ratio, $\sqrt{I_B/I_A}$.

. CCCII ith negative intrinsic resistance

Negative resistance has very useful role in different applications. For example it can be used to realize oscillator circuits and to enhance quality factor of filters. Among other active devices that can be used to realize negative resistors is the CCCII. Recently a bipolar based second generation current controlled conveyor CCCII with negative intrinsic resistance was proposed in [14]. In this paper a CMOS based CCCII with negative intrinsic resistance r_x is presented. Figure 6 shows the circuit diagram of the proposed application. The resistance r_x is given by:

$$r_x = -(g_{m1}^{-1} \quad g_{m2}^{-1} \quad g_{m3}^{-1} \quad g_{m4}^{-1}) \qquad (8)$$

where g_{mi} denotes the transconductance of the transistor number i. Fig. 7 shows plots of calculated and simulated values of r_x over a wide range of I_B and I_A which depict a good agreement between them.

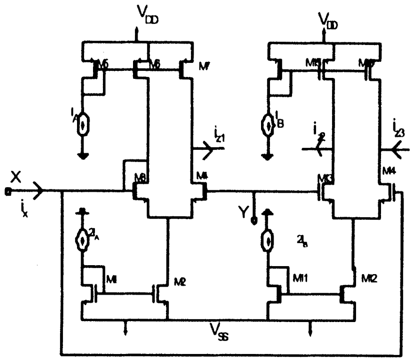
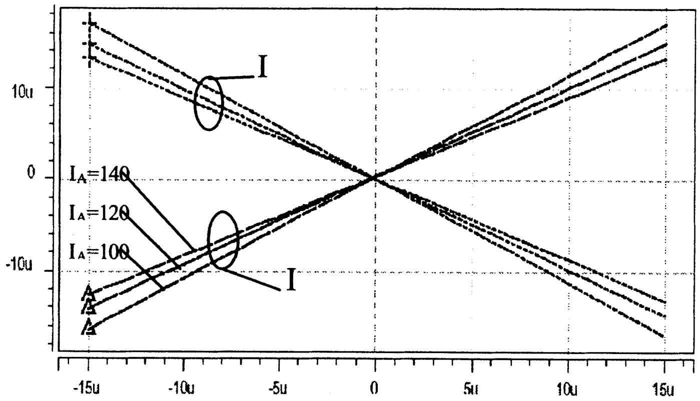


Figure 4
Circuit configuration of the proposed variable current gain CCCII



Ix (A)

Figure 5
Current Iz2 and Iz3 as a function of the current I_X at I_B =120 A

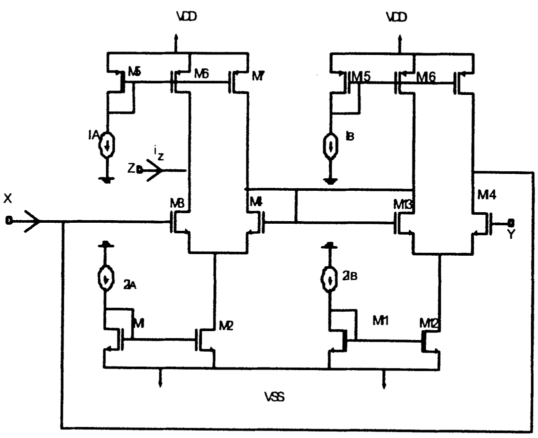
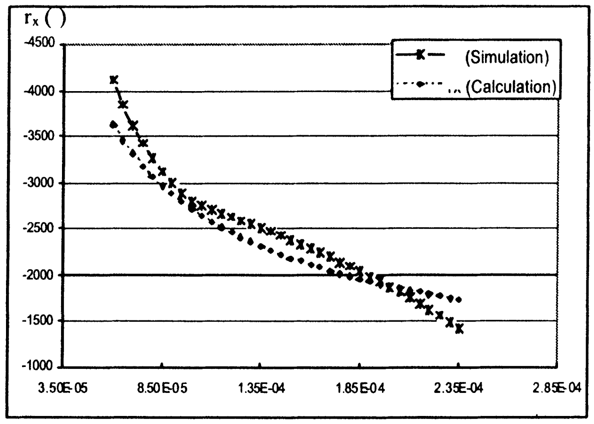


Figure 6
Circuit configuration of the proposed CCCII with negative r_x



Bias current I_B=I_A (A)

Figure 7
Resistance r_x as a function of the bias current I_B and I_A

IV. Conclusion

Variable current gain CCCII, CCCII with negative resistance have been presented. Both circuits were realized using a simple CMOS CCCII configuration. Current gain and intrinsic resistance of the proposed circuits can be easily control by the bias current HSPICE simulation shows that the proposed circuits have good performance. The simulation results are generally in excellent agreement with the proposed theory. It worth mentioning that all of the proposed circuits don't utilize signal mirroring and this will reduce the harmonic distortion [15].

Ac no ledgment The authors would like to thank Dr. M. T. Abuelma'atti for his valuable comments. Acknowledgment is also due to King Fahd University of Petroleum and Minerals for supporting the work.

V.References

1 Fabre, A., Saaid, O., Wiest, F., and Boucheron, C.: "Current controlled bandpass filter based on translinear conveyors", *Electronics etters*, vol. 31, no 20 , pp. 1727-1728, 1995.
2 Fabre, A., Saaid, O., Wiest, F., and Boucheron, C.: "High frequency applications based on a new current controlled conveyor", *IEEE trans. Circuit Syst*, vol. 43, no 2 , pp. 82 -91, 1996.
3 Seguin, F., Fabre, A.: "2 GHz controlled current conveyor in standard 0.8 /spl mu/m BiCMOS technology", *Electronics etters*, vol. 37, no 6 , pp. 329 -330, 2001.
4 Minaei, S., Kaymak, D., Ibrahim, M., and Kuntman, H.: "New CMOS Configuration for

Current Controlled Conveyor (CCCIIs)", *IEEE International Conference Circuits and Systems for Communications, ICCSC* 2002, pp. 62-65.

5 El Ghitani, H.: "A 2.2-V BiCMOS controlled current conveyor and high- current-mode band-pass filter application", *Radio Science Conference, 1 th NRSC 000*, pp. C15/1 -C15/7, 2000.

6 Abuelma'atti, M., and Tasadduq, N.: "New current-mode current-controlled filters using the controlled conveyor", *Int. . Electronics*, vol. 85, No.4, pp. 483-488, 1998.

7 Anuntahirunrat, K., Tangsrirat, W., Riewruja, V., and Surakampontron, W.: "Sinusoidal frequency doubler and full-wave rectifier using translinear current controlled conveyors", *he 000 IEEE Asia-Pacific Conference Circuits and Systems, IEEE APCCAS 000*, pp. 166 -169, 2000.

8 Toker, A., Gune, E.O., Ozoguz, S.: "New high-band-pass filter configuration using current controlled current conveyor based all-pass filters", *he th IEEE International Conference on Electronics, Circuits and Systems, ICECS 001.*, vol. 1 , pp. 165 -168, 2001

9 Minaei, S., Cicekoglu, O., Kuntman, H., and Turkoz, S.: "New current-mode lowpass, bandpass and highpass filters employing CCCIIs", *th IEEE Mid est Circuits and Systems Symposium, M SCAS 001*, vol. 1, pp. 106 -109, 2001.

10 Barthelemy, H., Meillere, S., and Kussener, E.: "CMOS sinusoidal oscillator based on current-controlled current conveyors", *Electronics etters*, vol. 38, No. 21, pp. 1254 -1256, 2002.

11 Ferri, Giuseppe.: "Current conveyors II", *Electronics orld ournal*, pp. 300-302, April 2001.

12 Carlosena, A., and Moschytz, G.S.: "Design of variable-gain current conveyors" *IEEE ransactions on Circuits and Systems I*, vol. 41, no. 1, pp. 79 -81, 1994.

13 Abuelma'atti, M. T., and Shabra, A.: " Composite Second-Generation-Current Conveyor with Variable Current and Voltage Gains" *International ournal of Analog Integrated Circuits and Signal Processing*, vol.9, pp. 265-270, 1996.

14 Barthelemy, H., and Faber, A.: "A Second Generation Current-Controlled Conveyor With Negative Intrinsic Resistance", *IEEE trans. Circuit Syst.*, vol.49, No. 1, pp. 63-65, Jan. 2002.

15 Awad, I. A., and Soliman, A. M.: "New CMOS Realization of the CCII-", *IEEE trans. Circuit Syst.*, vol. 46, no 4 , pp. 460 -463, 1999.