# A Beam-Forming Transmit ASIC for Driving Ultrasonic Arrays

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Summary. This paper describes the design of a programmable 8-channel integrated circuit for driving ultrasonic array transducers. The IC is capable of generating variable delay lengths of up to  $65\mu$ s in steps of 1ns. Integrated on the same chip is an array of eight high voltage pulser circuits (up to 100V). The output pulse width can also be set to match the transducer operating frequency. A minimum width of 20ns is possible and the rise and fall times are typically 5 ns and 7 ns. It can also be programmed to give bursts of up to 16 repetitions to facilitate Doppler imaging.

Keywords: ASIC, ultrasonic, pulser

### Introduction

The use of arrays of ultrasonic transducers has become widespread in medical ultrasonic imaging. In general these are 1-D arrays of piezo-ceramic composite materials, although PVDF arrays have been reported [1]. By electrically exciting the array elements in a pre-determined order it is possible to electronically steer a focused beam of ultrasonic energy for imaging purposes, [2]. Recent years have seen the emergence of 2-D arrays that facilitate 3-D ultrasound imaging [3]. Although, in the main, the latter are sparse arrays, the trend is for the number of array elements that have to be driven electronically to increase. The implication is that the wire bundle that connects the transducer array to the control unit becomes ever more unwieldy. A solution to this problem is to mount as much as possible of the controlling electronics, both transmit and receive, at the array itself. This paper describes an eight channel prototype transmit beam-forming IC that can be mounted directly on the transducer head.

### Overview of the new IC

A block diagram of the complete system is shown in Figure 1. The coarse timer is a 10-bit synchronous counter. The fine timer is essentially a delay locked loop (DLL) used to sub-divide a master clock into sixty-four multiple-phase clocks. These two blocks are common to eight channels of identical timing circuits. The device is programed by writing delay values into the FIFO buffers. Each timing circuit has a comparator to compare the programmed time with the running coarse counter. When these values match, a signal one clock cycle wide is triggered at the comparator output. This provides an enabling window for the fine timer. A programmed 64:1 multiplexer then selects the appropriate output from the DLL which is passed through to the high voltage module. Hence a resultant output of variable delay lengths can be programmed. The output is shaped before triggering the high voltage pulser. It can be stretched to match the operating frequency of an ultrasonic transducer. It can also be repeated to generate a tone burst for doppler imaging.



Fig. 1: Block diagram of the complete transmit ASIC.

# **Fine timer**

The fine timer is a delay locked loop (DLL) which is used to interopolate between succesive periods of the reference clock, [1]. Figure 2 shows the basic block diagram of a DLL. A reference clock is delayed through a variable delay line until it is synchronised with the *next* period of the reference clock. A feedback loop constantly adjusts the delay so that the phase difference between the two clocks remains zero.



Fig. 2: Block diagram of delay locked loop.

The variable delay line is made up of a series of sixty-four delay elements. These are shown in Figure 3 and comprise a current starved inverter and a normal inverter. The output from the last delay element is the feedback which is compared with the reference. Each delay interval is adjusted to be 1ns apart by controlling  $V_{CP}$  and  $V_{CN}$ , hence a 15.625MHz master clock is required to make the feedback exactly one clock cycle behind the reference.



Fig. 3: Current starved inverter delay element.

# High voltage output stage

This ASIC integrates the high-voltage pulsing circuits along with the 5V CMOS digital circuits. The technology is provided by the Alcatel Mietec Intelligent Interface Technology (I<sup>2</sup>T) which permits the co-integration of CMOS, bipolars (BiCMOS) and DMOS technolgies. Before being passed to the high voltage stage the output from the timing circuitry can be programmed to change the pulse width or to provide for repetitve bursts.

The pulser, shown in Figure 4, is configured as a source-follower. Co-integrated DMOS transistors are used as they can sustain the 100V needed to drive the array elements. The output must remain at ground during idle state for safety reason. The output push-pull transistors are sized ( $R_{DSon} < 20\Omega$ ) to drive a maximum load of  $200\Omega//20pF$ . Two large protection diodes are added at the output to withstand any high voltage surge



Fig. 4: DMOS pulser circuit.

Two complementary signals, at Vx and Vy, are required to drive the pulser. Vx is normally high while Vy is normally low. A transition of Vy to VDD (5V) causes the gate of HV3 to surge towards ground. The amount of voltage displacement is determined by the ratio of transistor HV1 to transistor HV2. Hence they can be sized to give maximum gate-source voltage allowed by the process design rule, that is, Vgs less than 12 volts. The effect is that transistor HV3 switches on and raises its output towards HV\_VDD. Transistor HV5 is a source-follower so that the output, Vout, follows suit. At the same moment, Vx is low, turning off both transistors HV4 and HV6.

When Vx and Vy switches back to high and low respectively, the output falls to ground. The weak diode WD1 has the benefit of pulling the gate of transistor HV3 to HV\_VDD, thus turning it completely off to minimise idle power consumption.

#### References

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