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Munir A. Al-Absi [a]
[a] Department of Electrical Engineering, King Fahd University of Petroleum and Minerals, Saudi Arabia

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A novel highly accurate current mirror

Munir A. Al-Absi*

Department of Electrical Engineering, King Fahd University of Petroleum and Minerals, P.O. Box 1139, Dhahran 31261, Saudi Arabia

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A novel complementary metal-oxide semiconductor (CMOS) current mirror that can work in weak and strong inversion is proposed. The mirror is capable of accurately copying current in the nano-ampere range. The proposed scheme eliminates the DC matching error caused by the difference between drain-to-source voltages of both the input and output transistors. The proposed circuit was verified using ORCAD simulator in 0.8 μm CMOS process technology. Simulation results confirm the functionality and accuracy of the circuit.

Keywords: current mirror; CMOS circuits

1. Introduction

Current mirrors (CMs) are the core structure for almost all analogue and mixed mode circuits, and the performance of analogue structures largely depends on their characteristics. CMs are used to perform identity operations, current amplification, biasing and loading elements. Analogue-to-digital and digital-to-analogue converters are additional circuits that use CMs (Wang 1990; Rajput 2004). In many applications, the performance of the simple CM is inadequate because of a systematic gain error and low output resistance. It is well known that CMs suffer from transistor mismatch and DC matching errors. In the past two decades, a series of high performance CMs in metal oxide semiconductor (MOS) technology has been reported (Wang 1990; Mulder and Van Der Woerd 1996; Rajput 2004). The CMs available in the literature are based on one or combination of the following design techniques (Rajput 2004).

- Triode region CMs.
- Sub-threshold region CMs.
- Bulk-driven metal-oxide-semiconductor field-effect transistor (MOSFET)-based CMs.
- Level shifter-based CMs.
- Self-cascode MOSFET-based CMs.
- Floating gate MOSFET-based CMs.

Low-power CMs using low supply voltages are attractive for all designers. Two widely used CMs with both low systematic gain errors and high output resistance are

*Email: mkulaib@kfupm.edu.sa

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the stacked cascode mirror (Ramirez-Angulo 1993) and the improved Wilson CM (Hart and Barker 1976; Gray, Hurts, Lewis and Meyer 2001). DC matching error is always present in these designs but its percentage varies from one approach to another. Its presence causes deterioration in the performance of the A/D converters (Gregorian and Temes 1986; Nairn and Salama 1988, 1989). The cascode CM reported by Behzad Razavi (2001) is a good solution but consumes voltage headroom substantially. A novel CM for portable applications was presented by Rajput and Janaur (2001). The drawback of this mirror is the limited range of the input current from 1 to 500 μA. In this article, a new design for a novel CM that can copy current in the nano-ampere range and eliminate the DC matching error is presented. The proposed CM can be used for all modes of complementary metal-oxide semiconductor (CMOS) operations; sub-threshold, triode and saturation.

2. Proposed structure

CMs can be designed with MOSFETs operating either in sub-threshold region, triode region or in saturation region. However, it may be noted that most of the CMs have been designed with MOSFETs operating in saturation region only. This is because designing of the CMs based on saturated MOSFETs is simpler and the resultant structure is suitable for high-frequency applications. Based on the region of MOSFET operation, the requirements for the CMs are:

- For CMs built using MOSFETs operating in triode region, it is mandatory to ensure that $V_{DS1} = V_{DS2}$ in addition to $V_{GS1} = V_{GS2}$.
- CMs built using saturated MOSFETs require $V_{GS1} = V_{GS2}$. However, if V_{DS1} equals V_{DS2} then the short channel effect can be eliminated.
- The requirements of the CMs operating in sub-threshold regions are the same as the CMs with saturated MOSFETs implying $V_{GS1} = V_{GS2}$; however, sub-threshold MOSFETs require large W/L and low input current.

Figure 1 shows the proposed CM. It consists of two transistors M_1 and M_2 that represent the mirror cell and a second generation current-controlled current conveyor to keep $V_{DS2} = V_{DS1}$.

The CCCII characteristic can be modelled as:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & r_x & 0 \\ 0 & -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{1}$$

From Equation (1), $v_y = v_x + i_x r_x$. With reference to Figure 1, the conveyer's Z terminal is connected to the gates of M_1 and M_2. This will ensure that $i_z = 0$. As a consequence $i_x = 0$ and hence $v_y = v_x$ which means the drain-to-source voltages of M_1 and M_2 are equal. Moreover, the voltage V_z is used to control the biasing mode of M_1 and M_2. The current conveyor is implemented using the basic structures presented by Behzad Razavi (2001) and is shown in Figure 2.

Figure 3 illustrates the complete circuit diagram of the proposed scheme. Here M_1 and M_2 form mirror transistors, M_3–M_9 are the conveyor transistors. If the input current is in nano-ampere range, load resistance R_L can be as large as 200k.

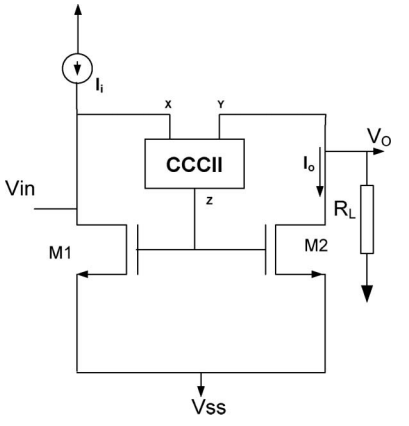

Figure 1. Proposed new CM circuit.

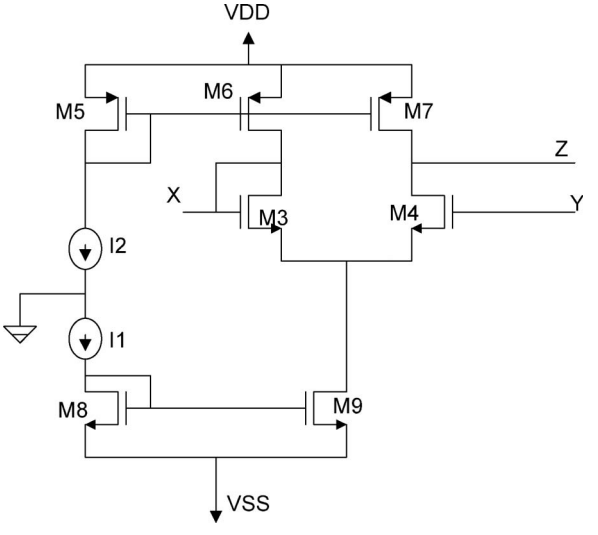

Figure 2. Complete current conveyor circuit diagram.

The mode of operation of M_1 and M_2 will be controlled by V_z which is controlled by the voltage across the load resistance.

Simulation result and discussion

The proposed CM was simulated using the ORCAD simulator in 0.8 μm CMOS process. The input current was varied from 0 to 100 nA. The plot of the output current versus the input current is shown in Figure 4. It is clear from the plot that the error is very small with a maximum value of 2%. If the current is increased, the load resistance R_L must be decreased to keep transistor M_4 in operation. Simulation of the mirror for the microampere current range is shown in Figure 5. In this range, the error decreases to around 0.1%. It is evident from Figures 4 and 5 that the output current is the exact replica of the input current.

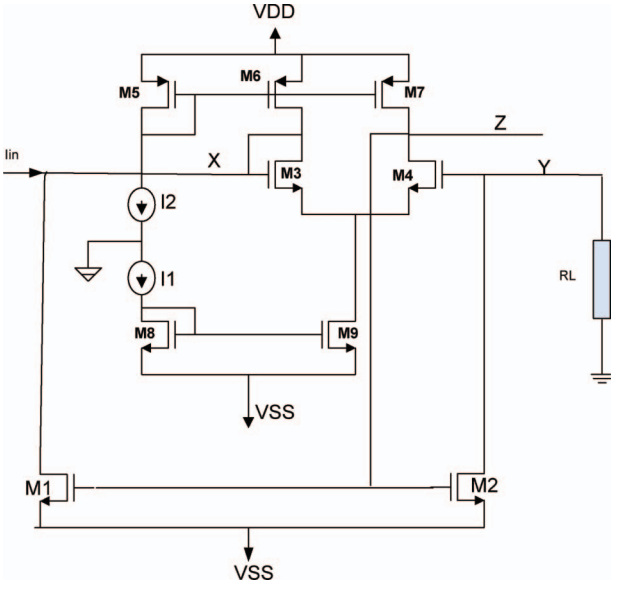

Figure 3. Proposed CM.

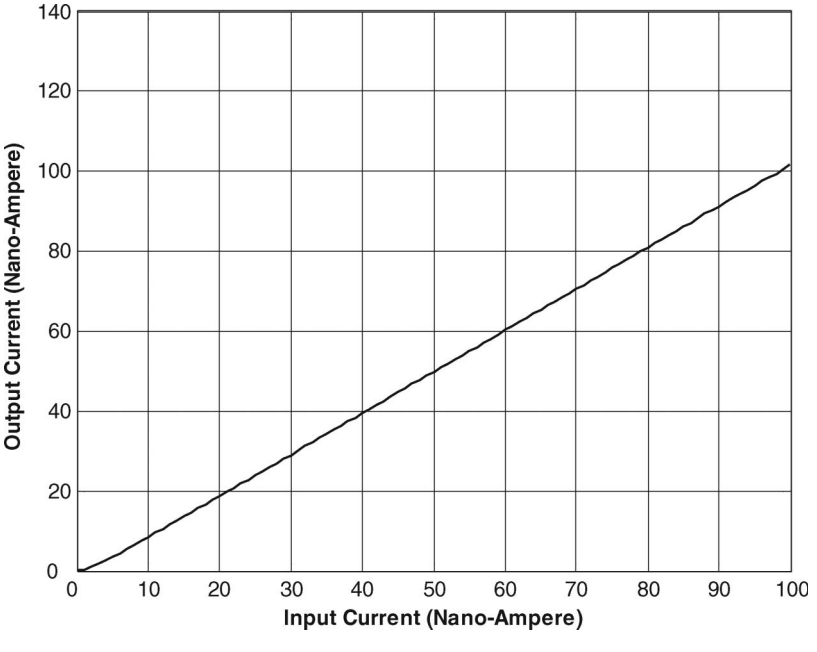

Figure 4. Variation of the output current with the input current in the nano-ampere range.

Frequency response of the proposed circuit was carried out for the nano-ampere range. Plot of the frequency response is shown in Figure 6. It is evident from the plot that the 3 dB frequency is about 60 Khz, which is expected for nano-ampere input current range.

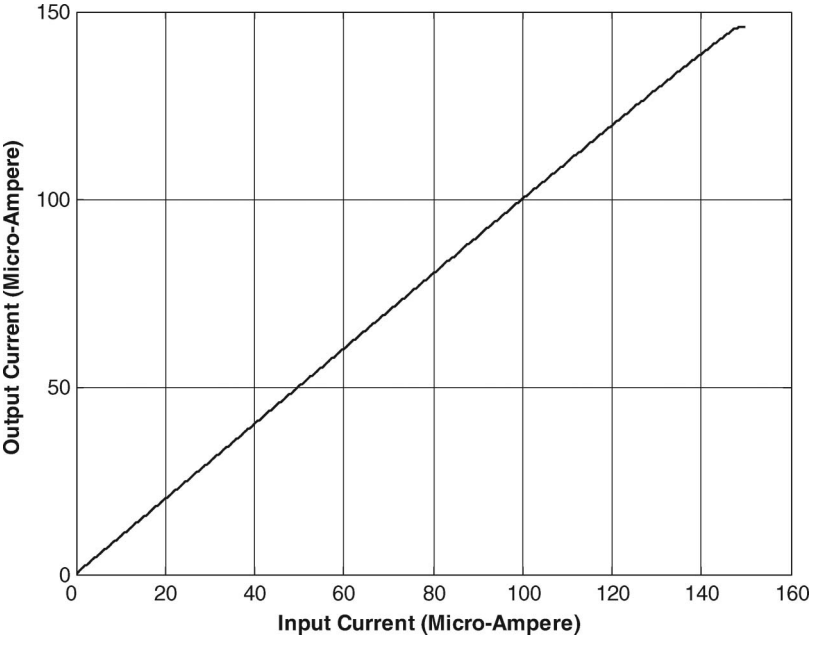

Figure 5. Variation of the output current with the input current in the microampere range.

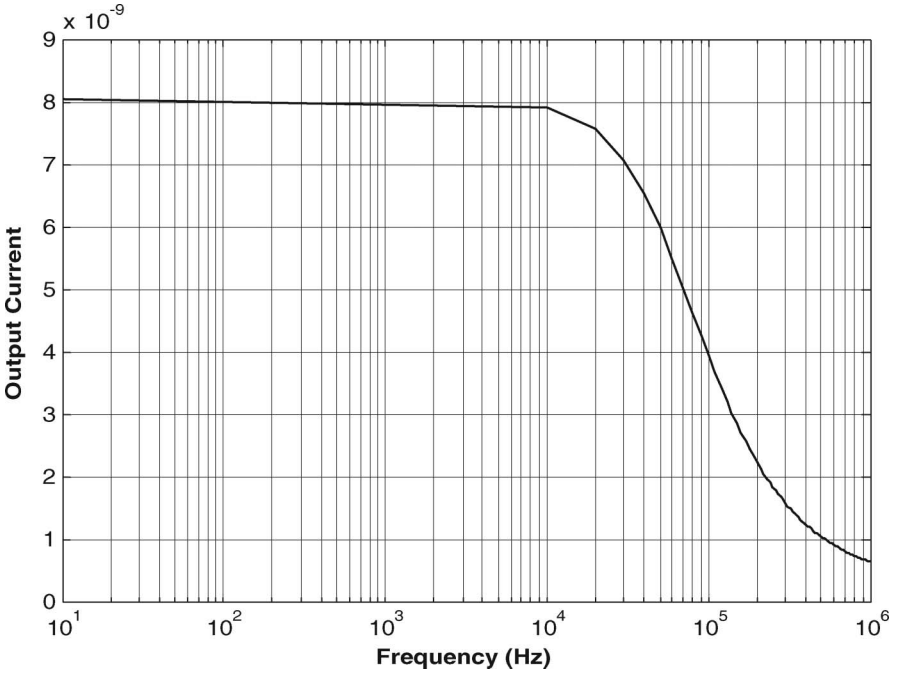

Figure 6. Frequency response of the CM operating in the nano-ampere range.

3. Conclusion

Using two MOS transistors and one second-generation current-conveyer, a CM with negligible DC-matching error has been developed. The proposed mirror covers all modes of operation and can copy current in the range of nano-ampere with high accuracy. The proposed configuration was verified by simulation using industry standard parameters in ORCAD simulator.

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