Effects of Electrode Spacing on the Response of Optically Controlled MESFETs

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In microwave GaAs MESFETs, carrier transport is a strong function of carrier energy. When illuminated, the carrier energy and carrier distribution inside the device are substantially affected by the incident optical energy. To account for these effects an accurate model based on the energy formulation of the transport equation coupled with optical energy conversion equations is used [1-2]. This model is used to investigate the optimum design of optically controlled MESFET structures considering the trade-off between the degradation in electric characteristics and the improvement in photoelectric conversion efficiency. Time domain simulations show the significant effect of electrode spacing, specifically, the drain-gate separation (Fig. 1). Interesting observations are made when the drain-gate separation was varied from 0.3 to 1.4 μm. Devices with different drain-gate spacing respond differently to a fixed-waist Gaussian light pulse in terms of peak output photocurrent, waveform rise time and waveform fall time. The peak value of the output photocurrent increases sharply, as more device area is exposed to light, but starts to level up after a certain value of drain-gate spacing where no appreciable gain is observed (Fig. 2a). This behavior is due to the increasingly active recombination process that takes place over large spacing. On the other hand, charging and discharging times remain strong functions of drain-gate spacing (Fig. 2b, and 2c), as the optically generated electron-hole pairs require more time to be flushed out. To quantify the trade-off between conversion efficiency and device switching characteristics, a figure of merit is defined as

$$FoM = \frac{Peak\ Current\ Value}{Discharge\ Time}$$

For the particular case considered here the best performance of the device is with drain-gate separation of around 0.8 μm (Fig. 2d).

[1] M. Alsunaidi et al, Int. J. Numer. Model., vol. 10, pp. 107-119, 1997.
[2] M. A. Alsunaidi et al, IEICE Trans. Electronics, vol. 7, pp. 869-874, July 2001.

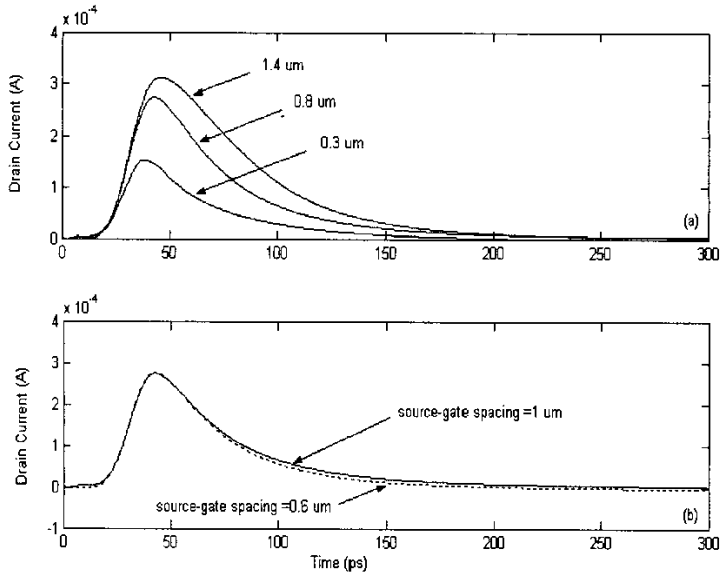

Fig. 1: Drain current pulsed response.

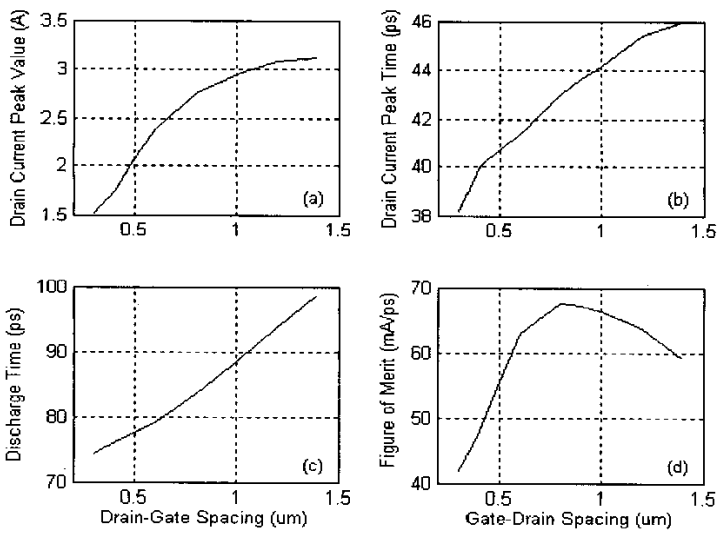

Fig. 2: The effect of Drain-gate spacing on (a) drain current peak value, (b) drain current peak time, (c) discharging time and (d) figure of merit.

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