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A New Biasing Technique for the MOS Transistor

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Abstract: - This paper describes a new biasing technique for the MOS transistor. The MOS is biased by a Gate-to-Bulk voltage V_{GB}. The value of V_{GB} can be chosen according to the level of inversion required, strong or weak. The input signal, current or voltage can be fed from either the drain or the source terminal. The technique can be sued in the implementation of logarithmic and antilogarithmic functions with microampere current range. This in turn will enhance the speed of the device in this mode of operation compared to the traditional weak inversion biasing. The new approach was verified by simulation using HSPICE level 47 in 0.8um CMOS process.

Key-Words: - Biasing Weak inversion Strong inversion Logarithmic Antilogarithmic

1 Introduction

It is well known MOS transistor are usually biased using fixed gate-to-source voltage V_{GS}. The MOS is a four terminal device and in many applications the bulk terminal is connected to the least potential for nMOS and to the highest potential for the pMOS. Some powerful circuits were designed using bulk-to-source voltage V_{BS} [1]. In this paper, a new biasing technique for the MOS transistor in which gate-to-bulk voltage, V_{GB} is used to bias the MOS transistor is presented. In section 2, background of MOS fundamentals is presented. The new MOS biasing technique is presented in section 3. Simulation verification of the technique is presented in section 4. Section 5 will be devoted to conclusion and future work.

2 Background

In the MOS transistor, using the traditional biasing technique, with all potential referenced to the substrate, the drain-source current, I_{DS}, in weak inversion is given by an expression of the form [2]:

$$I_{DS} = I_{SO}.e^{\left(\frac{V_p - V_S}{v_t}\right)} - I_{SO}.e^{\left(\frac{V_p - VD}{v_t}\right)} \qquad (1)$$

Where V_p is the pinch-off voltage given by:

$$V_P = \frac{V_{GB} - V_{TO}}{n} \qquad (2)$$

Where I_{SO} is the transistor specific current given by:

$$I_{SO} = 2.n.\beta..v_t^{\,2} \qquad (3)$$

n is the slope factor given by:

$$\frac{1}{n} = 1 - \frac{\gamma}{2\sqrt{V_G - V_{TO} + \left(\frac{\gamma}{2} + \sqrt{\Psi_O}\right)^2}} \qquad (4)$$

It has been shown that V_{GB} and the surface potential at inversion, Ψ_S, can be related by the following equation [3]:

$$V_{GB} = V_{FB} + \Psi_S + \gamma\sqrt{\Psi_S + kT/q.\exp^{\left(\frac{\Psi_S - 2\phi_F - V_{CB}}{2kT/q}\right)}} \qquad (5)$$

In weak inversion, $\Psi_S = 2\phi_F + V_P$, , [4,5] where ϕ_F is the Fermi potential, V_{FB} the flat-band voltage and V_P is the MOS "pinch-off" voltage which in weak inversion is less than or equal to the channel to substrate voltage V_{CB}. Therefore, in weak inversion with KT/q, much less than Ψ_S : the exponential term under the root sign becomes negligible and:

$$\Psi_{S(V_{GB})} \approx \left(-\frac{\gamma}{2} + \sqrt{V_{GB} - V_{FB} + \frac{\gamma^2}{4}}\right)^2 \qquad (6)$$

Thus, when V_{GB} is fixed, the surface potential is fixed in weak inversion and will vary with V_{CB} in strong inversion. This fact, lead us to the possibility of using a gate to substrate biasing technique. The value of V_{GB} can be chosen according to the level of inversion required using the above equations.

3 New biasing technique

Our approach is different from the traditional approach used and is depicted in Fig1.

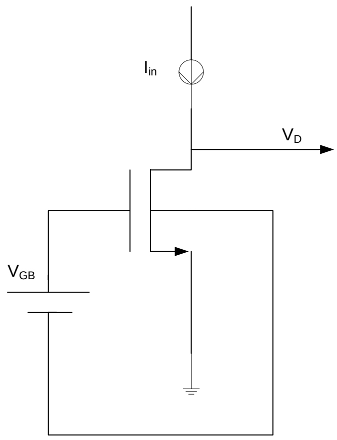

Fig1. New biasing technique

In our discussion, we will consider the weak inversion as an illustration for the new biasing approach. It is well documented that, the transistor channel is weekly inverted if the surface potential, Ψ_S is such that $\phi_F < \Psi_S < 2\phi_F$, it follows that to force the transistor to work in the middle of weak inversion, it is required to set the surface potential to be ($\Psi_S = 1.5\phi_F$) [2,3,4]. The value of V_{GB} that will ensure this situation is calculated from the equations above 3. Since the channel is weakly inverted, the drain current must be caused by diffusion only [3, 4, 5, 6, 7] . On the other hand, to operate the transistor in strong inversion then the surface potential should be set to $\Psi_S > 2\phi_F$. In terms of CMOS fabrication it is obvious that only transistors in wells can be fabricated by this approach and the technique is, therefore, better suited to Intelligent Interface technology (I2t) process. This is the rationale behind the present application.

4 Simulation results

4.1 Weak inversion

As stated before, to force the MOS transistor to work in the middle of weak inversion it is necessary to set the surface potential Ψ_S such that:

$\Psi_S = 1.5\phi_F$

Given the MOS parameters (n-MOS) in 0.8μM CMOS process,

$\phi_F = 0.4$

$\Psi_S = 0.6$

The value of V_{GB} that will ensure this value of the surface potential is calculated from equation (5). One can set V_{GB} to 0.7 volt, this value will ensure weak inversion mode of operation.

Simulation test for different device dimension was carried out and results were tabulated. >From these results, a relation between V_{DS} and the input current is extracted and is given by:

$$V_{DS} = -2V_P e^{\left(\frac{I_{in} - I_P}{(n^2+n)I_{SO}}\right)} \qquad (7)$$

Where V_p is the pinch off voltage given by equation 2 and I_p is the pinch off current.

A possible realization for the antilogarithmic function is shown in Fig 2.

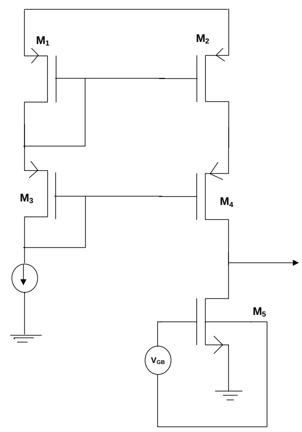

Fig2. Antilogarithmic circuit

Here transistor M_1, M_2, M_3, and M_4 forms the current mirror, which will provide the required input current at the drain of transistor M_5. Transistor M_5 is responsible for producing the antilogarithmic relation. Since transistor M_5 is biased in weak inversion by a fixed voltage V_{GB}, the drain to source voltage V_{DS} and the drain to substrate voltage V_{DB} will be proportional to the exponent of the drain current. With the transistor M_5 has a channel width to channel length ration W/L = 3;

$$V_P = \frac{V_{GB} - V_{TO}}{n} = \frac{0.7 - .8386}{1.42} \approx -0.1$$

Simulation of the circuit in Fig 3 was carried out. The input current I_{in} is varied from 0 to 6μA. Plots of V_{DS} and V_{DB} are shown in Fig 3.

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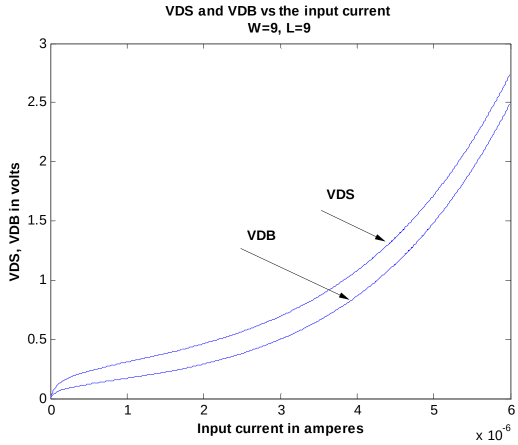

Fig3. Plots of V_{DS} and V_{DB}

From fig 3, when $V_{DB} > |V_P|$ it is evident that V_{DS} and V_{DB} are exponentially related to the input current. At the same time V_{BS} is almost in linear relation with the input current and it can be approximated to constant value. To ensure the exponential relation of V_{DS} and V_{DB} with the input current, plot of

$\ln\left(\frac{V_{DB}}{V_P}\right)$ and $\ln\left(\frac{V_{DS}}{2V_P}\right)$ are shown in Fig 4.

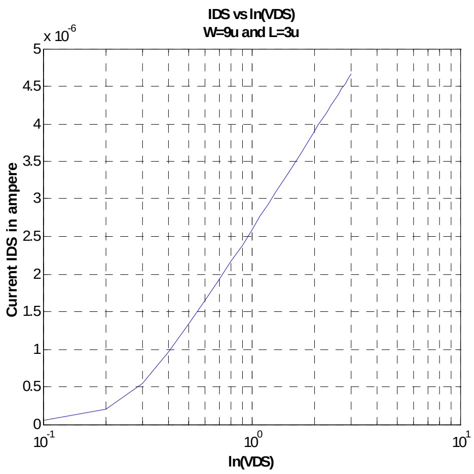

Fig4. Plot of $\ln\left(\frac{V_{DS}}{2V_P}\right)$

It is evident from the plot $\ln\left(\frac{V_{DS}}{2V_P}\right)$ is in linear relation with the input current I_{in}. The range of the input current can be set by device dimension W/L. If the ratio of W/L is increased, the range of the input current will increase while the exponential relation is still valid.

4.2 Strong Inversion

The new biasing technique can be used in strong inversion. In order to operate the MOS in strong inversion, then the surface potential Ψ_S must be set such that; $\Psi_S \geq 2\phi_F$. The value of V_{GB} that will ensure this mode of operation can be set to 1.2. In strong inversion the channel is formed, when the current signal is applied to the drain of the MOS, the voltage V_{DS} will be in linear relation with the input current. The value of which depends on the device dimension and $V_{GB.}$ Varying V_{GB} will produce a variable linear resistance, which can be used in voltage controlled amplifier. Simulation of the circuit of Fig 2 in strong inversion is carried out and the plot of V_{DS} as a function of the input current is shown in Fig 5

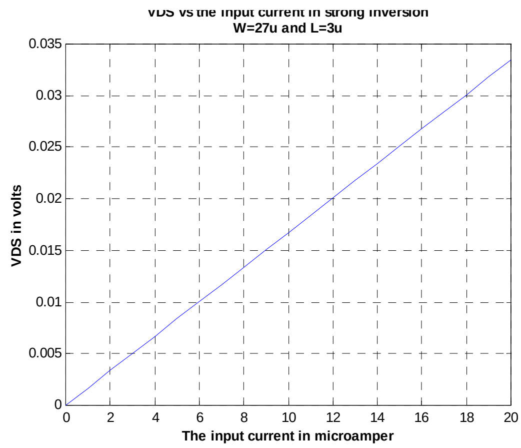

Fig5. Plot of V_{DS} in strong inversion

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5 Conclusion

A new biasing technique for the MOS transistor was presented. We believe that the new technique can open the door for implementing new circuits using the gate-to-substrate biasing. As an example antilogarithmic and logarithmic functions are easily implemented using this technique with better current range and hence better speed which is not possible in traditional biasing. More has to be done in future work like experimental verification and the design of the biasing voltage V_{GB}.

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