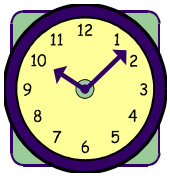
King Fahd University of Petroleum and Minerals

Electrical Engineering Department

EE200: Digital Logic Circuit Design

Second Semester 2002-2003 (022)



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Office hours: *Sat. Mon. Wed. from 12-13:30 or by prior appointment*

Tentative Course Outline and Schedule

Week	Date	Topics	Sections	Labs/Prob. Sessions
1	Feb. 22-26	Binary Numbers, Number Base Conversions,	1.1-1.3	No Lab.
2	Mar. 1-5	Octal & Hexadecimal Numbers, Complements, Signed Binary Numbers, Binary Codes	1.4-1.7	Introduction to Lab. Equipment
3	Mar. 8-12	Binary Logic, Boolean Algebra: Axioms, Theorems & Properties. Boolean functions, Digital Logic Gates	1.9, 2.1-2.4 2.7-2.8	Exp#1: Binary & Decimal Numbers
4	*Mar. 15-19*	Canonical & Standard Forms, More Logical Operations, Simplification of Boolean functions Using K-Maps, Product of Sums Simplification.	2.5-2.6 3.1-3.4	Exp#2: Digital Logic Gates
5	Mar. 22-26	Don't-care Conditions, NAND, NOR, and Other Two Level Implementations, Exclusive-OR Function, Introduction to HDL.	3.5-3.8	Exp#3: Introduction to LogicWorks
6	*Mar.29-Apr. 2*	Combinational Logic: Analysis and Design Procedures, Code Conversion, Adder circuits. ***Exam I Sun., Mar. 30***	3.9, 4.1-4.4	Exp#4: Boolean Algebra **Exam # 1 14-108 at 5:30**
7	Apr. 5-9	Subtractors, Decimal Adder, binary multiplier, Magnitude Comparator, Decoders.	4.5-4.8	Exp#5: Simplification
April 9 Last Day for dropping courses with grade 'W'				
8	Apr. 12 - 16	Encoders and Multiplexers, Example of HDL for combinational circuit (gate-level modeling).	4.9-4.11	No Lab
9	April 19 - 23	Programmable Logic, PLD'S, ROM, Programmable Logic Array, Programmable Array Logic.	7.5-7.7	Exp#6: Code Conversion
10	Apr. 26 - 30	Sequential Circuits, Latches, Flip-flops, Characteristic Tables	5.1-5.3	Exp#7: Adders/Subtractors
April 30 Last Day for withdrawal from all courses with grade 'W'				
11	May 3 - 7	Analysis of Clocked Sequential Circuits, Example of HDL for Sequential Circuits (behavioral modeling), State Reduction and Assignment.	5.4 -5.6	Exp#8: Multiplexers
12	May 10 - 14	Flip-flop Excitation Tables, Design Procedure, Synthesis using different flip flops. ***Exam II Sun., May 18***	5.7	Exp#9: Design with ROM's **Exam II 14-108 at 5:30**
13	May 17 - 21	Registers and Shift Registers	6.1, 6.2	Exp#10: Flip-flops
14	May 24 - 28	Ripple Counters, Synchronous Counters and other counters.	6.3-6.5	Exp#11: Counters & Sequential Logic
15 16	May 31– Jun 7	Revision		**Lab Final**

Homework Problem Set:

Chapter 1: 5,7,9,18,20,29,34 Chapter 2: 2,5, 9, 12,15,17 Chapter 3: 2,7,12,15,19,24,31,36
Chapter 4: 5,11,13,20,25,29,31,35,37 Chapter 7: 15,18,20,21,24
Chapter5: 2,6,9,12,19, 24,26 Chapter 6: 5,7,8,12,21