King Fahd University of Petroleum and Minerals

Electrical Engineering Department

EE200: Digital Logic Circuit Design
*Course Coordinator: Dr. **Mahmoud M. Dawoud***
First Semester 2003-2004 (031)

A. Course Information

Text Book:	**Digital Design (3rd Edition) by M. M. Mano**			
Course	Name	Office	Phone	Sections
Instructors:	Dr. Mahmoud M. Dawoud **, Coordinator** ***mmdawoud@kfupm.edu.sa***	14/277	2299	3
	Dr. Essam Hassan ***ehassan @kfupm.edu.sa***	14/273	2370	5, 6
	Dr. Abdel-Malek Zidouri, ***malek@kfupm.edu.sa***	14/209-1	3677	1, 2
	Dr. Muhammad Al-Gahtani,	14/216-1	3695	4

Lab	Name	Office	Phone	Sections
Instructors:				
	Mr. A.A. Hussain			52
	Dr. I. Al-Saihati			56, 59
	Mr. S. Al-Ubaidi			51
	Mr. Z. Khan			53, 62
	Mr. B. Ganiyu			54, 58
	Mr. M. Baig			55
Grading:	Assignments and Quizzes	Lab. & Design Proj.	Two Majors	Final
	15%	20%	30%	35%

	First Major	Second Major	Lab Final	Final
Exams Dates:	**Sat. Oct. 18, 2003**	**Mon. Dec. 17, 2003**	**January 3-7, 2004** Your Lab time In your Lab	Per the schedule from the registrar's office
Exams Times:	8:00-9:30 pm	6:00-7:30 pm		
Exams Places:	**14-108**	**14-108**		

Important Dates:	Last day to drop the course without a permanent record	Last day to drop the course with "W" grade	Last day to drop all courses with "W" Thru Registrar's office.
	September 24, 2003	**October 28, 2003**	**December 2, 2003**

Note #1: Final Exam is comprehensive (i.e. covers chapter 1-7 as described in the syllabus and class notes). Lab Final will be given by the Lab instructor in the Lab during the normal Lab session.

Note #2: According to the rules and regulations of KFUPM, attendance is **MANDATORY**. More than **8** unexcused absences will be reported to the registrar office and result in a **GRADE of DN** regardless of the student's grade.

Note #3: It is your responsibility to solve the homework as soon as the material is covered in the class. Homework solution will be published on the University Web. Quizzes will be given regularly based on the homework problems.

Note #4: You can access the homework solutions on the computer network as arranged by your instructor:

The course information and home work solution will be available under Black Board EE200. This can be reached by typing http://bb.kfupm.edu.sa/ in your Internet Explorer Address line. Login using your student number as your user ID and password. Then change your password.

Note #5: **A** design project will be assigned around week 12 and will be due at the end of week 14**.**

B. Tentative Course Outline and Schedule

Week	Date	Topics	Sections	Labs/Prob. Sessions
1	September 13-17	Binary Numbers, Number Base Conversions,	1.1-1.3	No Lab.
2	September 20-25*	Octal & Hexadecimal Numbers, Complements, Signed Binary Numbers, Binary Codes	1.4-1.7	Introduction to Lab. Equipment
3	Sept. 27 – Oct. 1	Binary Logic, Boolean Algebra: Axioms, Theorems & Properties. Boolean functions, Digital Logic Gates	1.9, 2.1-2.4 2.7-2.8	Exp#1: Binary & Decimal Numbers
4	October 4-8	Canonical & Standard Forms, More Logical Operations, Simplification of Boolean functions Using K-Maps, Product of Sums Simplification.	2.5-2.6 3.1-3.4	Exp#2: Digital Logic Gates
5	October 11-15	Don't-care Conditions, NAND, NOR, and Other Two Level Implementations, Exclusive-OR Function, Introduction to HDL.	3.5-3.8	Exp#3: Introduction to LogicWorks
6	October 18-22	Combinational Logic: Analysis and Design Procedures, Code Conversion, Adder circuits.	3.9, 4.1-4.4	Exp#4: Boolean Algebra **Exam # 1**
7	October 25-29	Subtractors, Decimal Adder, binary multiplier, Magnitude Comparator, Decoders.	4.5-4.8	Exp#5: Simplification
8	November 1-5	Encoders and Multiplexers, Example of HDL for combinational circuit (gate-level modeling).	4.9-4.11	No Lab
9	November 8-12	Programmable Logic, PLD'S, ROM, Programmable Logic Array, Programmable Array Logic.	7.5-7.7	Exp#6: Code Conversion
10	November 30-Dec. 3	Sequential Circuits, Latches, Flip-flops, Characteristic Tables	5.1-5.3	Exp#7: Adders/Subtractors
11	December 6-10	Analysis of Clocked Sequential Circuits, Example of HDL for Sequential Circuits (behavioral modeling), State Reduction and Assignment.	5.4 -5.6	Exp#8: Multiplexers
12	December 13-17	Flip-flop Excitation Tables, Design Procedure, Synthesis using different flip flops.	5.7	Exp#9: Design with ROM's **Exam # 2**
13	December 20-24	Registers and Shift Registers	6.1, 6.2	Exp#10: Flip-flops
14	December 27-31	Ripple Counters, Synchronous Counters and other counters.	6.3-6.5	Exp#11: Counters & Sequential Logic
15	January 3-7	Revision		**Lab Final**

*** Thursday 25 September is a normal Saturday class.**

C. Homework Problem Set

Chapter 1: 5,7,9,18,20,29,34
Chapter 2: 2,5, 9, 12,15,17
Chapter 3: 2,7,12,15,19,24,31,36
Chapter 4: 5,11,13,20,25,29,31,35,37
Chapter 7: 15,18,20,21,24
Chapter 5: 2,6,9,12,19, 24,26
Chapter 6: 5,7,8,12,21