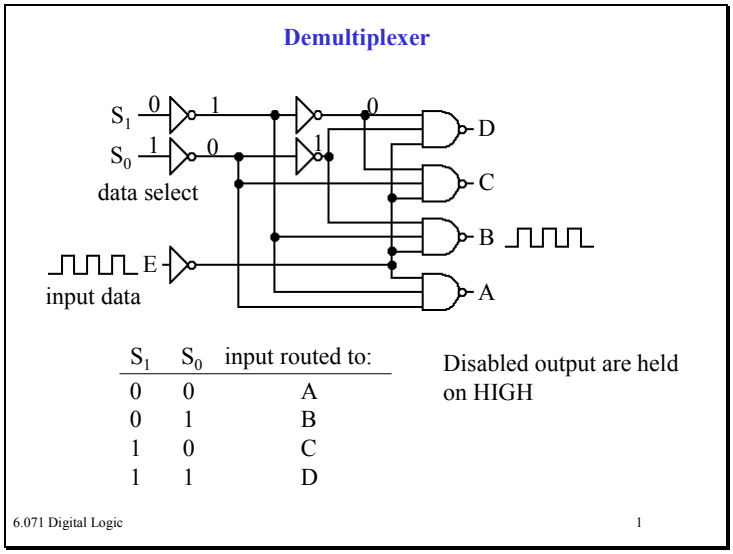
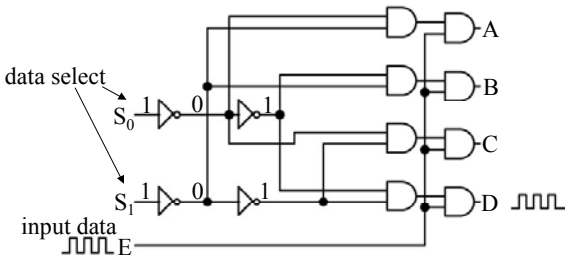
Slide 1



Of course the opposite action can also be implemented. A demultiplexer sends one signal to one of many lines.

Slide 2

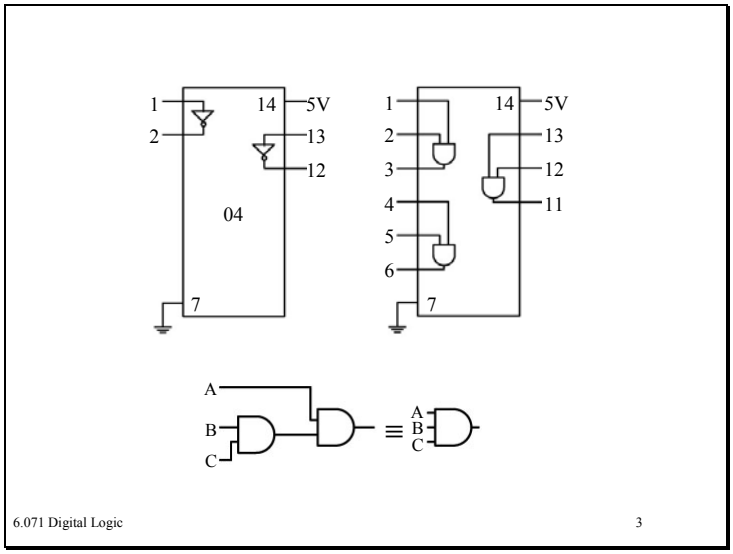
Demultiplexer (2-input AND gates)



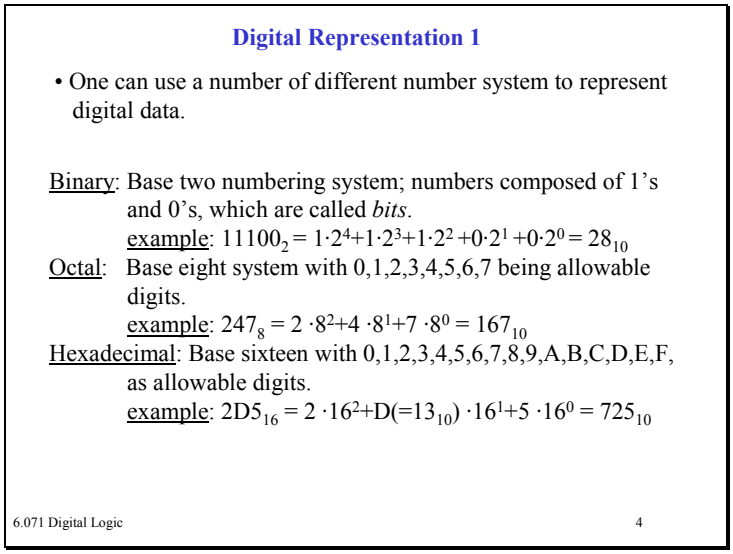
S_1	S_0	input routed to:
0	0	A
0	1	B
1	0	C
1	1	D

Disabled output are held on LOW

Slide 3



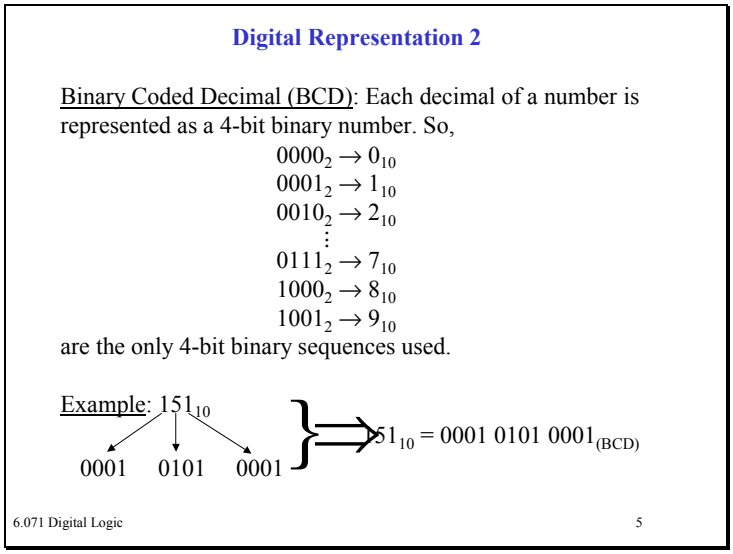
Slide 4



In digital circuits information is stored in binary form, consisting of an ordered array of two state devices.

Often for convenience three binary bits are combined to form an octal code, so although we discuss the information as though it was base eight, it is still stored and manipulated in binary form. The same is true for hexadecimal where data is represented in base 16 and stored in 4 bit binary.

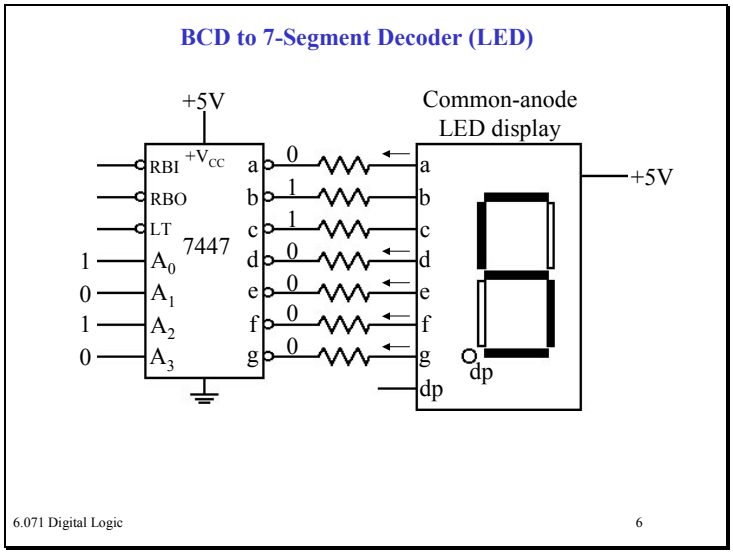
Slide 5



Since in out normal manipulations base 10 has special importance it is sometimes convenient to store and process information in binary coded decimal. Here 4 bits are used to represent the numbers 0 through 9. Of course 4 bits could store numbers 0 through 15, so there is some unused space.

BCD is most often encountered when we wish to output a decimal result. Using BCD greatly simplifies the task since each decimal bit is uniquely coded by 4 binary digits. There are encoders to switch from binary to BCD and back.

Slide 6



Another complex chip, in this case designed to control an LED numeric display.

Slide 7

7447 Data Sheet

March 1998

FAIRCHILD SEMICONDUCTOR

DM7446A, DM7447A
BCD to 7-Segment Decoders/Drivers

DM7446A, DM7447A BCD to 7-Segment Decoders/Drivers

General Description

The 46A and 47A feature active-low outputs designed for driving common-anode LEDs or incandescent indicators directly. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown on a following page. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

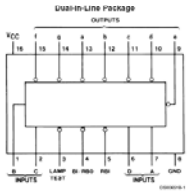
All of the circuits incorporate automatic leading and/or trailing-edge, zero-blanking control (RBI and RBO). Lamp test (LT) of these devices may be performed at any time when the BI/RBO node is at a high logic level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity (by pulsing) or to inhibit the outputs.

Features

- All circuit types feature lamp intensity modulation capability
- Open-collector outputs drive indicators directly
- Lamp-test provision
- Leading/trailing zero suppression

Connection Diagram

Dual-In-Line Package



Order Number DM5447AJ, DM7446AN or DM7447AN
See Package Number J16A or N16E

Slide 8

7447 Data Sheet 2

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V	DM54	−55°C to +125°C
Input Voltage	5.5V	DM74	0°C to +70°C
Operating Free Air Temperature Range		Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM5447A			DM7447A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			15			15	V
I_{OH}	High Level Output Current (BI/RBO)			−0.2			−0.2	μA
I_{OL}	Low Level Output Current (a thru g)			40			40	mA
I_{OL}	Low Level Output Current (BI/RBO)			8			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Slide 9

7447 Data Sheet 3

'47A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage (BI/RBO)	V_{CC} = Min I_{OH} = Max		2.4	3.7		V
I_{CEX}	High Level Output Current (a thru g)	V_{CC} = Max, V_O = 15V V_{IL} = Max, V_{IH} = Min				250	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.3	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max	BI/RBO			−4	mA
		V_I = 0.4V	Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (BI/RBO)				−4	mA
I_{CC}	Supply Current	V_{CC} = Max	DM54		60	85	mA
		(Note 5)	DM74		60	103	

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

'47A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 120Ω		100	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			100	ns

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7447 Data Sheet 4

Function Table

46A, 47A

Decimal or Function	Inputs						BI/RBO	Outputs							Note
	LT	RBI	D	C	B	A	(Note 6)	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	(Note 7)
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 8)
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 9)
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 10)

H = High level, L = Low level, X = Don't Care

Note 6: BI/RBO is a wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

Note 7: The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

Note 8: When a low logic level is applied directly to the blanking input (BI), all segment outputs are high regardless of the level of any other input.

Note 9: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go H and the ripple-blanking output (RBO) goes to a low level (response condition).

Note 10: When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are L.

X's means that the state does not matter; therefore, they are just a wa to save space in the table.

L's in the BI/RBO column suppresses all outputs; used to block leading and following zeros.

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Digital Representation 3

2's Compliment: Binary numbering scheme used to represent both positive and negative integers. Positive integers are represented the same was as in the original binary scheme; but negative integers are represented as the binary number that when added to the binary representation of its absolute value, equals zero.
Example: $41_{10} = 0010\ 1001_{2\text{'s comp}}$; $-41_{10} = 1101\ 0111_{2\text{'s comp}}$
One can verify adding both binary number equals zero.

To obtain a 2's compliment representation from a negative integer, take the true binary representation of the absolute value of that integer, reverse the bits, and add 1.

The addition of two binary numbers is quite simple, but the subtraction is a drag due to the borrowing needed. By storing information in 2's complement and then adding the result we achieve the same effect as if we had subtracted the numbers.

Slide 12

Binary Arithmetic

Adding: Adding binary numbers is just like adding decimal numbers; whenever the result of adding one column of numbers is greater than one digit, a 1 is carried over to the next column to be added.

Example:

			1		1			
20_{10} =	0	0	0	1	0	1	0	0
87_{10} =	0	1	0	1	0	1	1	1
	0	1	1	0	1	0	1	1

Subtraction: This operation is similar to decimal subtraction. The only potential point of confusion is that when "borrowing" from one column a 10_2 ($=2_{10}$) is carried over (not just a 1) to the next column. A trick to subtracting binary numbers is to add the 2's compliment of the subtracting number to the true binary representation of the number from which it is subtracting.

Example:

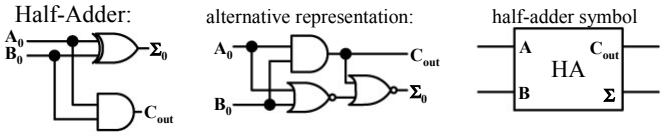
$+19_{10}$ =	0	0	0	1	0	0	1	1
-7_{10} =	1	1	1	1	1	0	0	1
Sum =	0	0	0	0	1	1	0	0

Subtraction is easy for us but a drag in binary

Slide 13

Binary Adders

Earlier, it was said that adding binary numbers is analogous to adding decimal numbers (i.e. one has to consider carry bits in multiple-bit additions). Binary addition can be implement through the use of logic gates. First consider the half-adder circuits below.



These circuits add two one-bit numbers and produce one two-bit number. Notice that both of the logic gate representations are equivalent.

6.071 Digital Logic 13

Adders are very useful devices and are simple to explore in binary representations. The half adder is used for the least significant bit. This bit of course has no possibility of a carry from an even lower bit and so just the two binary numbers themselves are important. Of course the two can generate a carry bit. So the half adder has two inputs and two outputs (the binary sum and a carry).
The half adder is most simply represented with an exclusive OR, but we rarely use such devices and so it is re-written in terms of AND and NORs. Since the half adder is widely used it is also given a special symbol.

Truth Table:

A	B	Συμ	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

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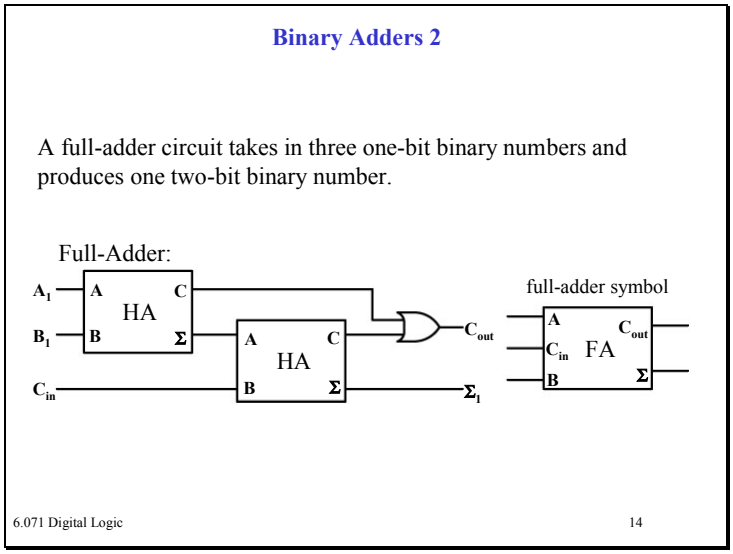

The full adder is used for all but the least significant bit. Here there are three inputs (the two binary numbers, and the carry from the next lower significant bit. Still there are only two outputs the sum and a carry. Of course if you can add two digits with a half adder, then two half adders can add three numbers. Notice the logic for the carry.

Truth Table:

A	B	Cin	Sum	Cout
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

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Binary Adders 3

A	B	Σ_{out}^{1}	C_{out}^{1}	C_{in}	$\Sigma_{\Sigma_{out}^{1}+C_{in}^{1}}$	C_{out}^{2}	$C_{out}^{1}+C_{out}^{2}$
0	0	0	0	0	0	0	0
0	1	1	0	0	1	0	0
1	0	1	0	0	1	0	0
1	1	0	1	0	0	0	1
0	0	0	0	1	1	0	0
0	1	1	0	1	0	1	1
1	0	1	0	1	0	1	1
1	1	0	1	1	1	0	1

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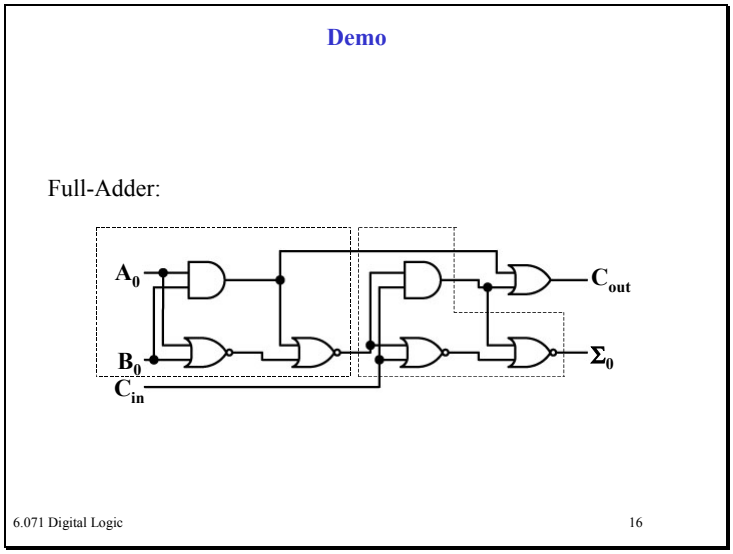

Our version of a 2 bit full adder. In the class one of the NOR gates is replaced with an OR and a NOT.

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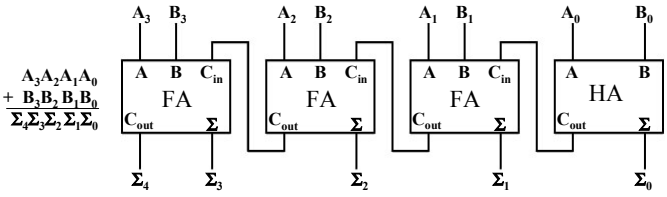
Binary Adders 4

Now, with the half-adders and full-adders, a multi-bit adder can be constructed:

4-bit Adder:

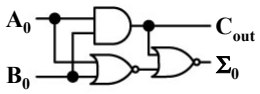


A 4 bit full adder. The least significant is a half adder and the others are full adders. Also notice that when adding 2x 4 bit digits and answer spans 5 bits.

Slide 18

Demo

Half-Adder:



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Problem (Extra Credit for Quiz #5):

Using as many of the following list of components as possible construct a circuit that performs some interesting function. Describe the function and state the output of the circuit. The circuit need not be most efficient, but should not be trivially reducible.

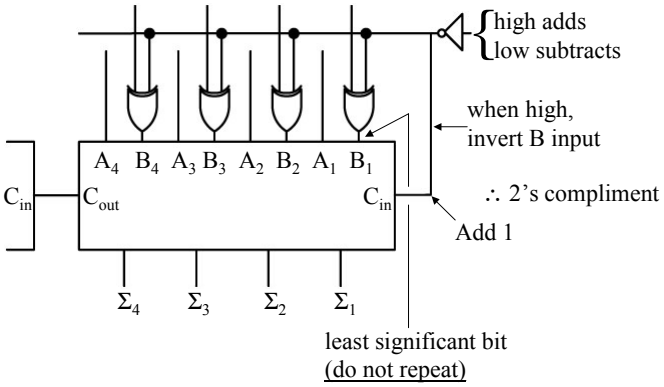
Component List:

4x switch	3x three-input AND
1x clock	3x three-input NOR
4x JK flip-flops	3x three-input NAND
4x OR	4x NOT
4x AND	
4x NOR	
4x NAND	

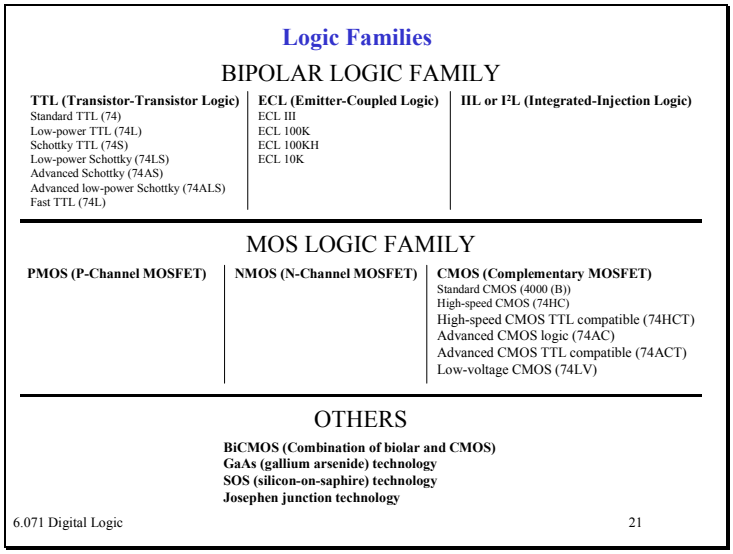
Bring this to the quiz and hand in at the start.

Slide 20

Binary Adder/Subtracter

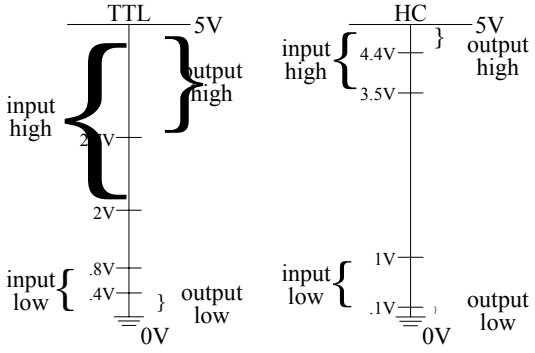


Slide 21



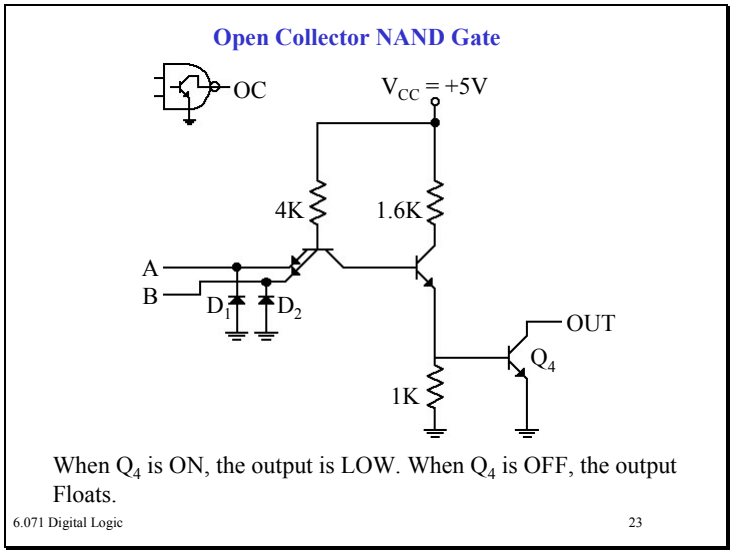
There are many versions of chips and they are not all compatible. Some of the older versions are hard to find and easily replaced with modern chips for example the HCT class. You do need to be careful about mixing types.

Slide 22



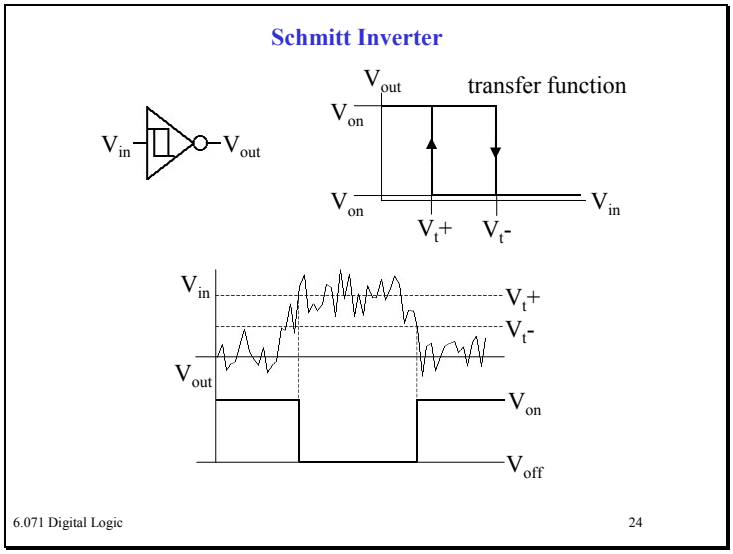
Output of HC can drive TTL. Output of TTL does not drive HC.

Slide 23



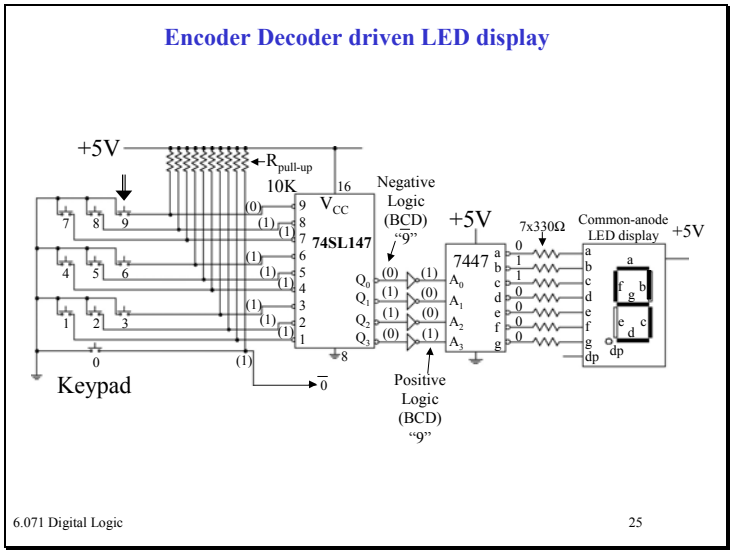
When both A and B are high the two BJT's in parallel are off (the emitter diodes do not have .6 V across them) so that the base of Q3 is high and Q3 is on and so the base of Q4 is high and the output is pulled low. However in the off state the output floats. If you use this in a digital circuit you will have to pull up the output with a resistor to 5 V. The nice feature about open collector devices is that they can sink a reasonable amount of power. So you could use this to switch 15 V at 100 mA, something you could not do with a normal TTL output.

Slide 24



We saw hystorisis with op amps, it is also often used with digital circuits especially where one expects noise (as in the bounce of a switch).

Slide 25



An example of the use of a 10 line decimal to 4 line BCD coder to drive an LED display of a numeric keypad. The 147 has 9 inputs and when any one is pulled low it outputs an inverted BCD representation of the digit. The inverters convert this to BCD which is then used to drive the 47 which is a BCD to 7 segment LED driver. The 0 state does not need to be coded and will be displayed correctly when all four BCD bits are low. Note the default output state of the 147 (all inputs high) is for all outputs to be high.
One of the issues when using the 147 is that there are many other input states that due not seem to be coded for, For example what happens when two inputs are pulled down? For this you need to check the data sheets.

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74LS147 Data Sheet

SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

SDLS053A – OCTOBER 1976 – REVISED FEBRUARY 2001

'147, 'LS147

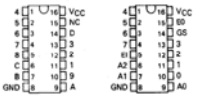
- Encodes 10-Line Decimal to 4-Line BCD
- Applications Include:
  - Keyboard Encoding
  - Range Selection

'148, 'LS148

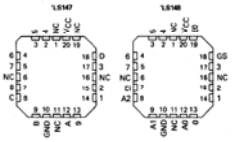
- Encodes 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:
  - N-Bit Encoding
  - Code Converters and Generators

TYPE	TYPICAL DATA DELAY	TYPICAL POWER DISSIPATION
'147	10 ns	225 mW
'148	10 ns	190 mW
'LS147	15 ns	60 mW
'LS148	15 ns	60 mW

SN54147, SN54LS147, SN54148, SN54LS148 . . . J OR W PACKAGE
SN74147, SN74148 . . . N PACKAGE
SN74LS147, SN74LS148 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS147, SN54LS148 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The '147 and 'LS147 encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. The '148 and 'LS148 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level. All inputs are buffered to represent one normalized Series 54/74 or 54LS/74LS load, respectively.

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74LS147 Data Sheet 2

'147, 'LS147
FUNCTION TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = high logic level, L = low logic level, X = irrelevant

'148, 'LS148
FUNCTION TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

TEXAS INSTRUMENTS

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1

Notice that the highest decimal number that is pulled down is coded. The X in the table indicates that the state of that input does not matter.

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74LS147 Data Sheet 3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '147, '148 . . . . . 5.5 V
'LS147, 'LS148 . . . . . 7 V
Interemitter voltage: 148 only (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54', SN54LS Circuits . . . . . −55°C to 125°C
SN74', SN74LS Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For '148 circuits, this rating applies between any two of the eight data lines, 0 through 7.

recommended operating conditions

	SN54'			SN74'			SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800			−400			−400	μA
Low-level output current, I_{OL}			16			16			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	−55		125	0		70	°C

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74LS147 Data Sheet 4

SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

SDLS053A – OCTOBER 1976 – REVISED FEBRUARY 2001

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'147 MIN	'147 TYP‡	'147 MAX	'148 MIN	'148 TYP‡	'148 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.3		2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	0 input	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		Any input except 0					40			80	
I_{IL}	Low-level input current	0 input	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		Any input except 0					−1.6			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−35		−85	−35		−85	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	Condition 1		50	70		40	60	mA
				Condition 2		42	62		35	55	mA

NOTE 3: For '147, I_{CC} (condition 1) is measured with input 7 grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open. For '148, I_{CC} (condition 1) is measured with inputs 7 and 8 grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

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74LS147 Data Sheet 5

SN54147, SN74147 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Any	In-phase output	C_L = 15 pF, R_L = 400 Ω, See Note 4		9	14	ns
t_{PHL}						7	11	
t_{PLH}	Any	Any	Out-of-phase output			13	19	ns
t_{PHL}						12	19	

SN54148, SN74148 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	1 thru 7	A0, A1, or A2	In-phase output	C_L = 15 pF, R_L = 400 Ω, See Note 4		10	15	ns
t_{PHL}						9	14	
t_{PLH}	1 thru 7	A0, A1, or A2	Out-of-phase output			13	19	ns
t_{PHL}						12	19	
t_{PLH}	0 thru 7	EO	Out-of-phase output			6	10	ns
t_{PHL}						14	25	
t_{PLH}	0 thru 7	GS	In-phase output			18	30	ns
t_{PHL}						14	25	
t_{PLH}	EI	A0, A1, or A2	In-phase output			10	15	ns
t_{PHL}						10	15	
t_{PLH}	EI	GS	In-phase output			8	12	ns
t_{PHL}						10	15	
t_{PLH}	EI	EO	In-phase output			10	15	ns
t_{PHL}						17	30	

[1] t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

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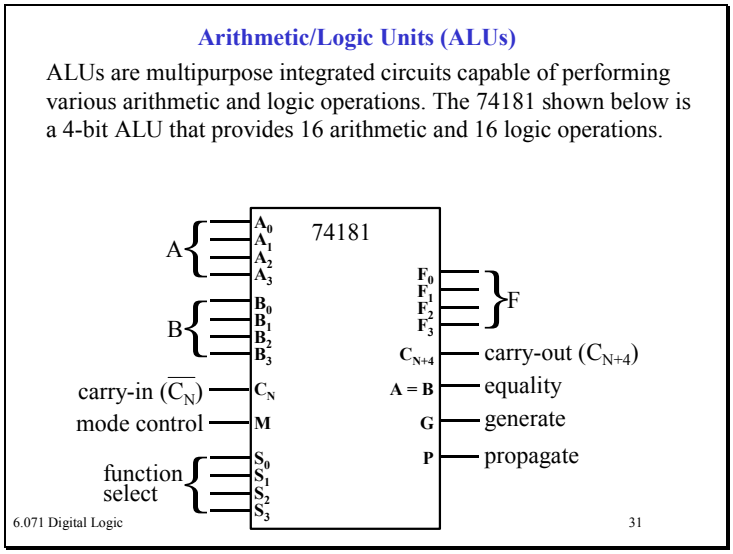

This one chip can perform any logic operation and many arithmetic operations on 2 4 bit words, and it does so via a programmable function selector. It is actually a rather old fashioned device by todays standards but it shows some nice capabilities of more complex chips. Today you would be more likely to use a microprocessor than an ALU.

For arithmetic operations the chip is provided with a carry (from an array of lower significance ALUs) and a carry out (to an array of higher significance ALUs. The chip works on two's complement and can add, subtract, double etc.

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74181 Data Sheet

MOTOROLA

SN54/74LS181

4-BIT ARITHMETIC LOGIC UNIT

The SN54/74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic, operations on two variables and a variety of arithmetic operations.

- Provides 16 Arithmetic Operations Add, Subtract, Compare, Double, Plus Twelve Other Arithmetic Operations
- Provides all 16 Logic Operations of Two Variables Exclusive — OR, Compare, AND, NAND, OR, NOR, Plus Ten other Logic Operations
- Full Lookahead for High Speed Arithmetic Operation on Long Words
- Input Clamp Diodes

4-BIT ARITHMETIC LOGIC UNIT

LOW POWER SCHOTTKY

CONNECTION DIAGRAM DIP (TOP VIEW)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

J SUFFIX
CERAMIC
CASE 623-05

N SUFFIX
PLASTIC
CASE 649-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic

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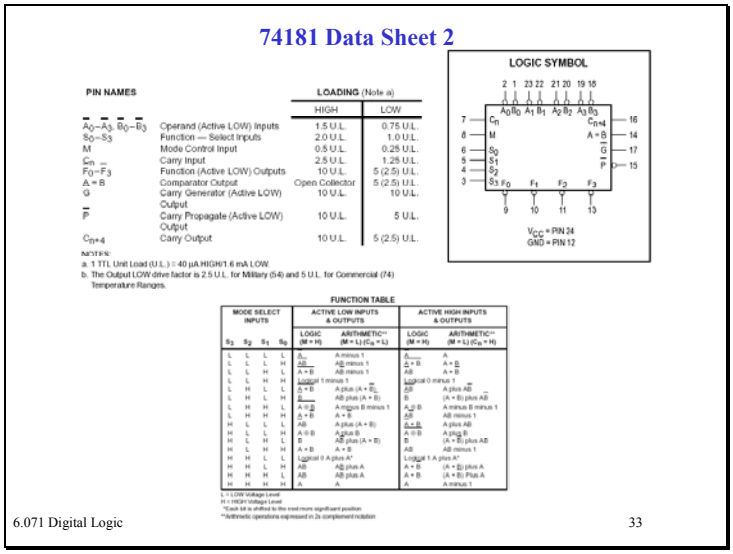

74181 Data Sheet 2

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{A_0}-\overline{A_3}$, $\overline{B_0}-\overline{B_3}$	Operand (Active LOW) Inputs	1.5 U.L.	0.75 U.L.
S_0-S_3	Function — Select Inputs	2.0 U.L.	1.0 U.L.
M	Mode Control Input	0.5 U.L.	0.25 U.L.
C_n	Carry Input	2.5 U.L.	1.25 U.L.
$\overline{F_0}-\overline{F_3}$	Function (Active LOW) Outputs	10 U.L.	5 (2.5) U.L.
A = B	Comparator Output	Open Collector	5 (2.5) U.L.
G	Carry Generator (Active LOW) Output	10 U.L.	10 U.L.
$\overline{P}$	Carry Propagate (Active LOW) Output	10 U.L.	5 U.L.
C_{n+4}	Carry Output	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL

FUNCTION TABLE

MODE SELECT INPUTS S_3	S_2	S_1	S_0	ACTIVE LOW INPUTS & OUTPUTS LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	ACTIVE HIGH INPUTS & OUTPUTS LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A}+B$	A + $\overline{B}$
L	L	H	L	$\overline{A+B}$	AB minus 1	AB	A + B
L	L	H	H	Logical 1 minus 1		Logical 0 minus 1	
L	H	L	L	$\overline{A}+B$	A plus (A + $\overline{B}$)	$\overline{AB}$	A plus AB, $\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A + B)	B	(A + B) plus AB
L	H	H	L	$A+\overline{B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$\overline{A}+B$	A + B	$\overline{AB}$	AB minus 1
H	L	L	L	AB	A plus (A + B)	$\overline{A+B}$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$A \oplus B$	A plus B
H	L	H	L	B	AB plus (A + B)	B	(A + B) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logical 0 A plus A*		Logical 1 A plus A*	
H	H	L	H	AB	AB plus A	A + B	(A + B) plus A
H	H	H	L	AB	AB plus A	A + B	(A + B) Plus A
H	H	H	H	A	A	A	A minus 1

L = LOW Voltage Level
H = HIGH Voltage Level
*Each bit is shifted to the next more significant position
**Arithmetic operations expressed in 2s complement notation

Note even in the arithmetic side, the + symbol stands for OR and AB means A and B. The word plus means addition.

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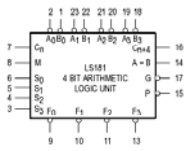
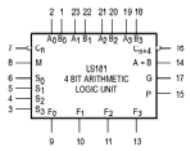
74181 Data Sheet 3

ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA
V_{OH}	Output Voltage — High (A = B only)	54, 74			5.5	V

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74181 Data Sheet 4

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage Except G and P	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA
		74		0.35	0.5	V	I_{OL} = 8.0 mA
	Output $\overline{G}$	54, 74			0.7	V	I_{OL} = 16 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
	Output $\overline{P}$	54			0.6	V	I_{OL} = 8.0 mA
		74			0.5		
I_{OH}	Output HIGH Current	54, 74			100	μA	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current Mode Input				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Any A or B Input				60		
	Any S Input				80		
	C_n Input				100		
	Mode Input				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
	Any A or B Input				0.3		
	Any S Input				0.4		
	C_n Input				0.5		
I_{IL}	Input LOW Current Mode Input				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	Any A or B Input				−1.2		
	Any S Input				−1.6		
	C_n Input				−2.0		
I_{OS}	Short Circuit Current (Note 2)		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current See Note 1A	54			32	mA	V_{CC} = MAX
		74			34		
	See Note 1B	54			35		
		74			37		

Note 1:
With outputs open, I_{CC} is measured for the following conditions:
A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded.
B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.
Note 2: Not more than one output should be shorted at a time, nor for more than 1 second.

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74181 Data Sheet 5

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, Pin 12 = GND, C_L = 15 pF)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, (C_n to C_{n+4})		18 13	27 20	ns	M = 0 V, (Sum or Diff Mode) See Fig. 4 and Tables I and II
t_{PLH} t_{PHL}	(C_n to $\overline{F}$ Outputs)		17 13	26 20	ns	M = 0 V, (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{G}$ Output)		19 15	29 23	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{G}$ Output)		21 21	32 32	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{P}$ Output)		20 20	30 30	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{P}$ Output)		20 22	30 33	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}_X$ or $\overline{B}_X$ Inputs to $\overline{F}_X$ Output)		21 13	32 20	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}_X$ or $\overline{B}_X$ Inputs to $\overline{F}_X$ Output)		21 21	32 32	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	(A_X or B_X Inputs to F_{XH} Outputs)			38 26	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	(A_X or B_X Inputs to F_{XH} Outputs)			38 38	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to $\overline{F}$ Outputs)		22 26	33 38	ns	M = 4.5 V (Logic Mode) See Fig. 4 and Table III
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to C_{n+4} Output)		25 25	38 38	ns	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (Sum Mode) See Fig. 6 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to C_{n+4} Output)		27 27	41 41	ns	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode)
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ Inputs to A = B Output)		33 41	50 62	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V R_L = 2.0 kΩ (Diff Mode) See Fig. 5 and Table II