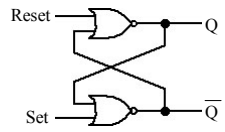
Slide 1

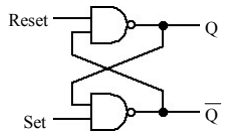
Flip-Flops

Cross-NOR SR flip-flop



S	R	Q	$\overline{Q}$	
0	0	Q	$\overline{Q}$	hold
0	1	0	1	reset
1	0	1	0	set
1	1	0	0	not used

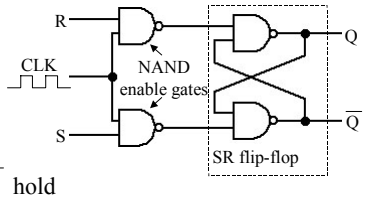
Cross-NAND SR flip-flop



S	R	Q	$\overline{Q}$	
0	0	1	1	not used
0	1	0	1	reset
1	0	1	0	set
1	1	Q	$\overline{Q}$	hold

Slide 2

Clocked Level-Triggered NAND SR Flip-Flop

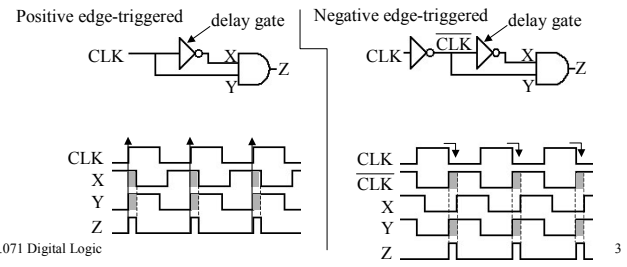


CLK	S	R	Q	$\overline{Q}$		
0	0	0	Q	$\overline{Q}$	hold	
0	0	1	Q	$\overline{Q}$	hold	SR inputs
0	1	0	Q	$\overline{Q}$	hold	disabled
0	1	1	Q	$\overline{Q}$	hold	
1	0	0	0	0	hold	
1	0	1	0	1	reset	SR inputs
1	1	0	1	0	set	enabled
1	1	1	Q	$\overline{Q}$	indeterminate	

Slide 3

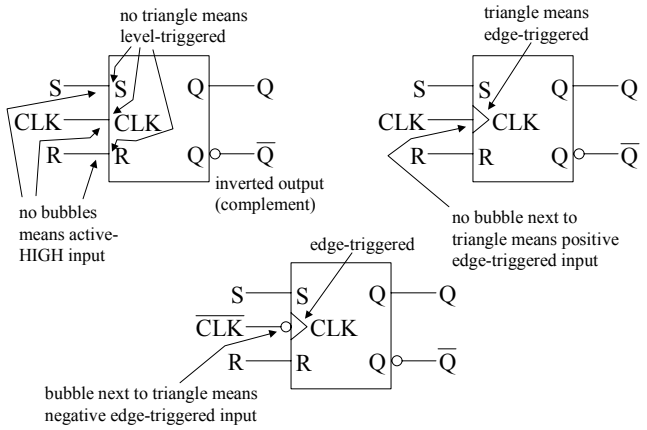
Edge-Triggered SR Flip-Flops

We can make the level triggered flip-flop more flexible (in terms of timing control) by turning it into an edge-triggered flip-flop. An edge-triggered flip-flop only samples the inputs during either a positive or negative clock edge. This conversion can be done by taking the clock signal and running it through a level-triggered, pulse generator network and taking the corresponding output as the clock signal.



Slide 4

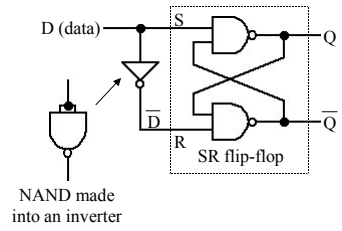
Level and Edge Triggered Flip-Flop Symbols



Slide 5

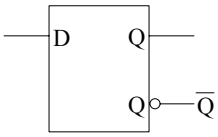
D-Type Flip-Flops

Basic D-type flip-flop or latch



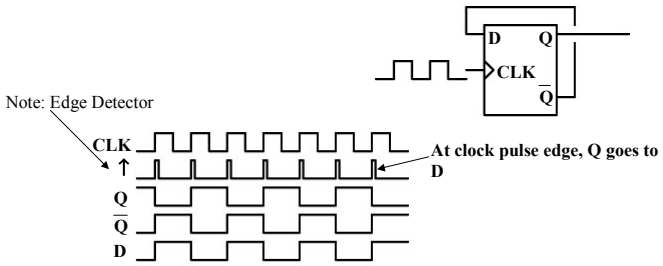
D	Q	$\overline{Q}$	
0	0	1	Reset
1	1	0	Set

logic symbol



Slide 6

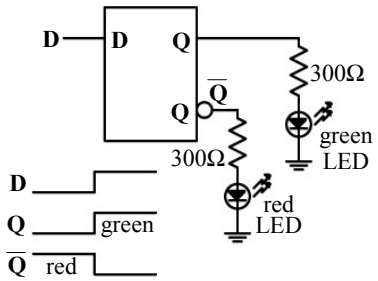
Divide by Two Circuit



So every time there is a clock pulse, Q is set to the old value of D. Therefore, $\overline{Q}$ changes (as does D) but by the time D changes, the edge is past.

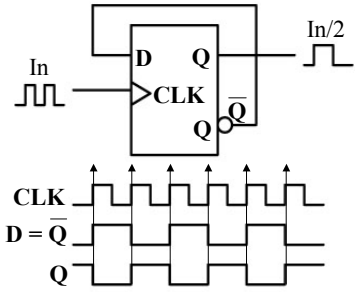
Slide 7

Stop-Go Indicator



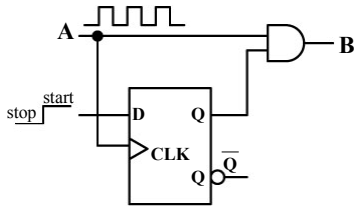
Slide 8

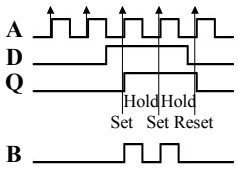
Divide-by-Two Counter



Slide 9

Synchronizer

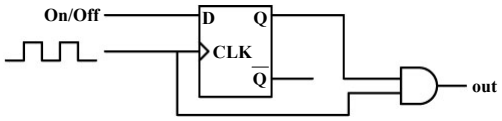


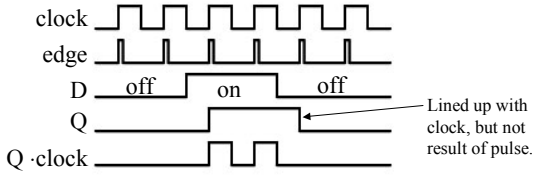


Slide 10

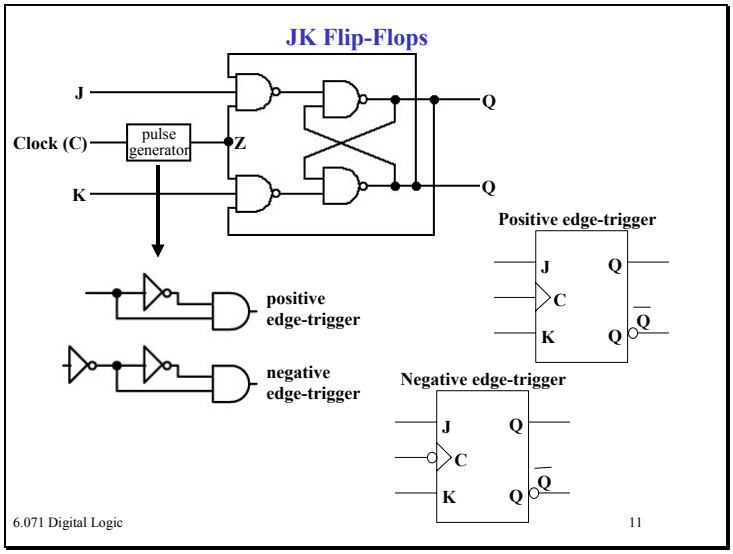
Synchronizer 2

We see timing is important, so we want to synchronize signals.



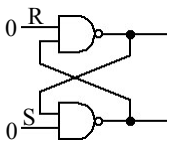


Slide 11


JK Flip-Flops
J
Clock (C)
pulse generator
Z
K
Q
Q
positive edge-trigger
negative edge-trigger
Positive edge-trigger
J
C
K
Q
Q
Negative edge-trigger
J
C
K
Q
Q
6.071 Digital Logic
11

Slide 12

JK Flip-Flops 2



R_{in} is (0,X) ∴ output is high; S_{in} is (0,1) ∴ output is high.

∴ all outputs are high.

The problem is that you can not "hold" this condition. The input 1,1 can only hold outputs of (0,1) or (1,0).

Slide 13

JK Flip-Flops 3

Positive edge-trigger

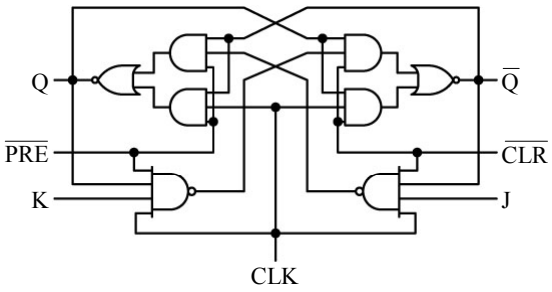
C	J	K	Q	$\overline{Q}$	
0	X	X	Q	$\overline{Q}$	hold
1	X	X	Q	$\overline{Q}$	hold
↓	X	X	Q	$\overline{Q}$	hold
↑	0	0	Q	$\overline{Q}$	hold
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	$\overline{Q}$	Q	Toggle

Negative edge-trigger

C	J	K	Q	$\overline{Q}$	
0	X	X	Q	$\overline{Q}$	hold
1	X	X	Q	$\overline{Q}$	hold
↑	X	X	Q	$\overline{Q}$	hold
↓	0	0	Q	$\overline{Q}$	hold
↓	0	1	0	1	Reset
↓	1	0	1	0	Set
↓	1	1	$\overline{Q}$	Q	Toggle

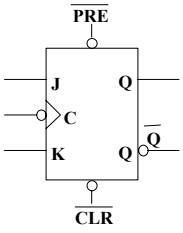
Slide 14

JK Flip-Flop with Preset and Clear



Slide 15

JK Flip-Flop with Preset and Clear (Negative Edge-Triggered)

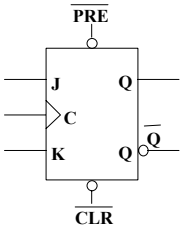


PRE	CLR	CLK	J	K	Q	$\overline{Q}$	
0	1	X	X	X	1	0	Preset
1	0	X	X	X	0	1	Clear
0	0	X	X	X	1	1	not used
1	1	↓	0	0	Q_0	$\overline{Q}_0$	hold
1	1	↓	0	1	0	0	Reset
1	1	↓	1	0	0	0	Set
1	1	↓	1	1	$\overline{Q}_0$	Q_0	Toggle
1	1	↑ 0,1	1	1	Q_0	$\overline{Q}_0$	hold

Q_0 = state of Q before HIGH-to-LOW edge of clock.

Slide 16

JK Flip-Flop with Preset and Clear (Positive Edge-Triggered)

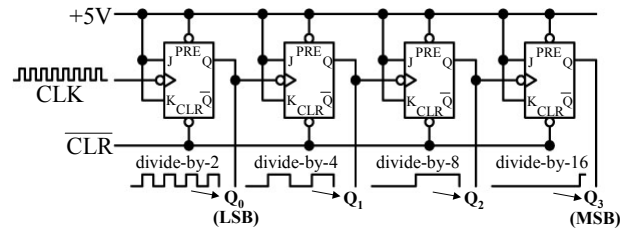


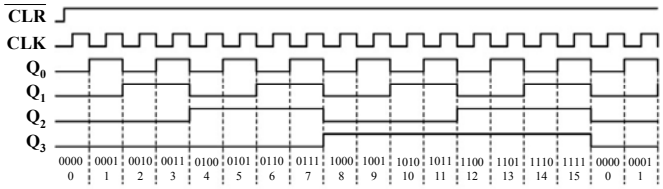
PRE	CLR	CLK	J	K	Q	$\overline{Q}$	
0	1	X	X	X	1	0	Preset
1	0	X	X	X	0	1	Clear
0	0	X	X	X	1	1	not used
1	1	↑	0	0	Q_0	$\overline{Q}_0$	hold
1	1	↑	0	1	0	0	Reset
1	1	↑	1	0	0	0	Set
1	1	↑	1	1	$\overline{Q}_0$	Q_0	Toggle
1	1	↓ 0,1	1	1	Q_0	$\overline{Q}_0$	hold

Q_0 = state of Q before LOW-to-HIGH edge of clock.

Slide 17

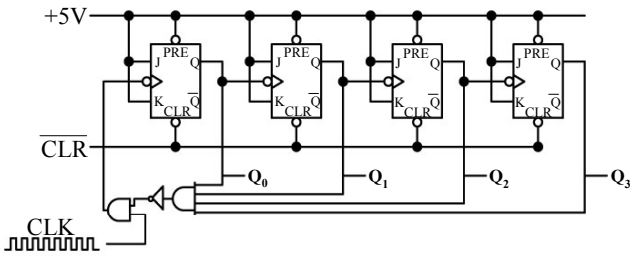
MOD-16 Ripple Counter/divide-by-2,4,8,16 Counter





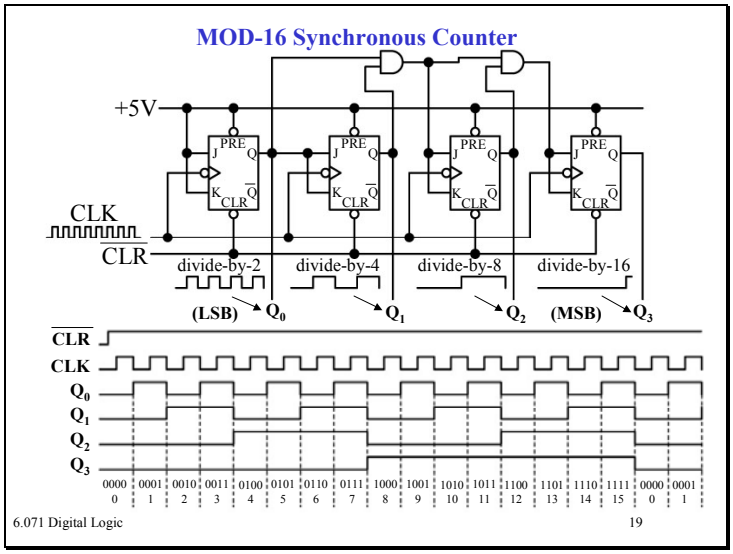
Slide 18

MOD-16 Ripple Counter 2



This circuit will count to up to 15 and then will disable (all bits = 0). Note: If one uses the $\overline{Q}$'s as the counting bits instead of the Q's, the Counter will count down from 15 and disable when 0 is reached.

Slide 19


MOD-16 Synchronous Counter
+5V
CLK
CLR
PRE
J
Q
K
CLR
Q
divide-by-2
divide-by-4
divide-by-8
divide-by-16
(LSB)
Q0
Q1
Q2
(MSB)
Q3
CLR
CLK
Q0
Q1
Q2
Q3
0000 0
0001 1
0010 2
0011 3
0100 4
0101 5
0110 6
0111 7
1000 8
1001 9
1010 10
1011 11
1100 12
1101 13
1110 14
1111 15
0000 0
0001 1
6.071 Digital Logic
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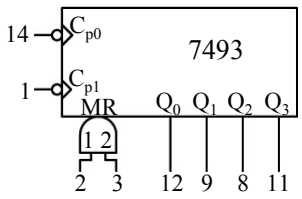
Slide 20

4-Bit Counter IC

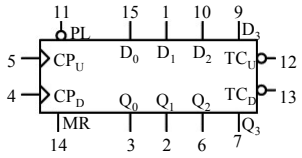
The 7493's internal structure consists of four JK flip-flops connected to provide separate MOD-2 and MOD-8 sections. Both of these are clocked by separate clock inputs. The MOD-2 uses C_{p0} as its clock input while MOD-8 uses C_{p1}.



MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H		count		
H	L		count		
L	L		count		

Slide 21

74193 Presettable 4-bit Binary Up/Down Counter



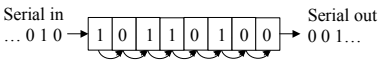
	Inputs								Outputs					
	MR_1	$\overline{PL}$	C_{pU}	C_{pD}	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	L	X	H	H	H	H	L	L	L	L	H	H
	L	L	H	X	H	H	H	H	H	H	H	H	L	H
	H	L	H	H	L	L	L	L	H	H	H	H	H	H
count up	H	H	↑	H	X	X	X	X	Count up				H	H
count down	L	H	H	↑	X	X	X	X	Count down				H	H

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH voltage transition

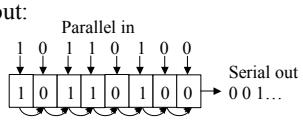
Slide 22

Block Diagrams of Various Shift Registers

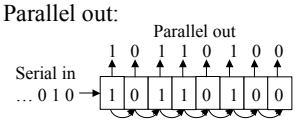
Serial in / Serial out:



Parallel in / Serial out:

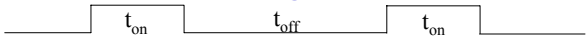


Serial in / Parallel out:



Slide 23

Creating Devices



Some device creating power -

There are two modes for destruction

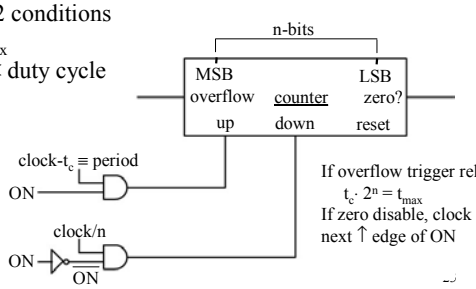
1.) Short term t_{on} is too long. Instantaneous heat load too high. Assume no heat dissipation during t_{on}.

2.) long term - duty cycle t_{on}/t_{off} too high.

$\therefore$ Test for 2 conditions

$t_{on} < t_{max}$

$t_{on}/t_{off} <$ duty cycle



If overflow trigger relay

$t_c \cdot 2^n = t_{max}$

If zero disable, clock until next ↑ edge of ON

Slide 24

Problem

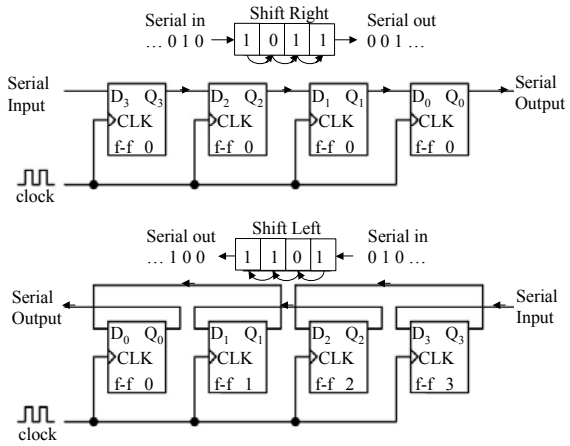
Explain why mon-stable is not so useful.

Solve problem using:

1x 555 - clock
flip/flops, simple logic …
1x up/down counter
borrow
carry
clear

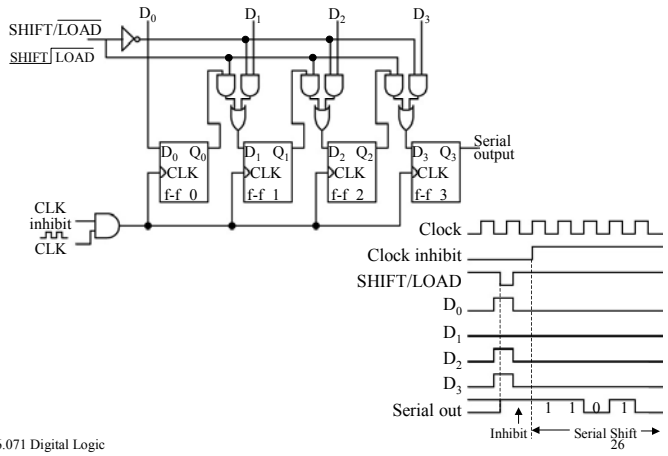
Slide 25

4-bit Serial in/Serial out Shift Registers



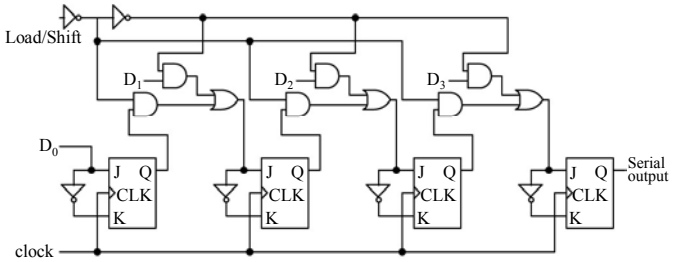
Slide 26

Parallel-to-Serial Shift Register

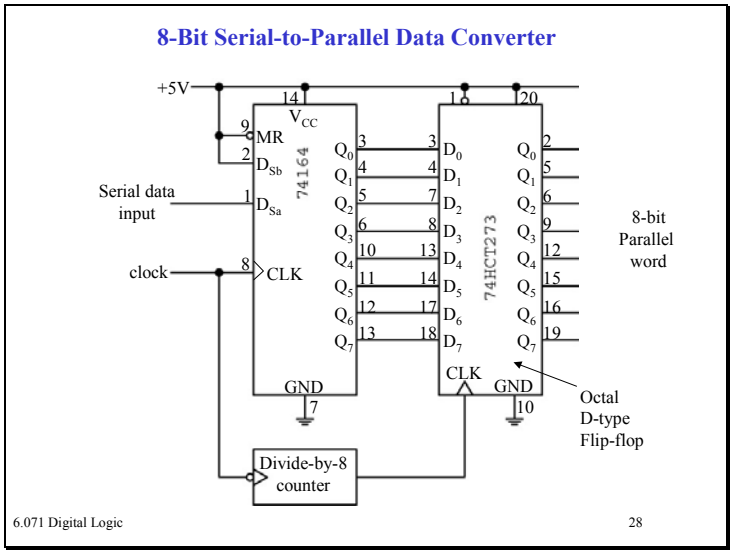


Slide 27

JK Parallel-to-Serial Shift Register



Slide 28


8-Bit Serial-to-Parallel Data Converter
+5V
14
V_{CC}
9
MR
2
D_{Sb}
Serial data input
1
D_{Sa}
clock
8
CLK
74164
Q_0 3
Q_1 4
Q_2 5
Q_3 6
Q_4 10
Q_5 11
Q_6 12
Q_7 13
GND
7
Divide-by-8 counter
1
20
D_0 3
D_1 4
D_2 7
D_3 8
D_4 13
D_5 14
D_6 17
D_7 18
CLK
GND
10
74HCT273
Q_0 2
Q_1 5
Q_2 6
Q_3 9
Q_4 12
Q_5 15
Q_6 16
Q_7 19
8-bit Parallel word
Octal D-type Flip-flop
6.071 Digital Logic
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Slide 29

8-Bit Parallel-to-Serial Interface