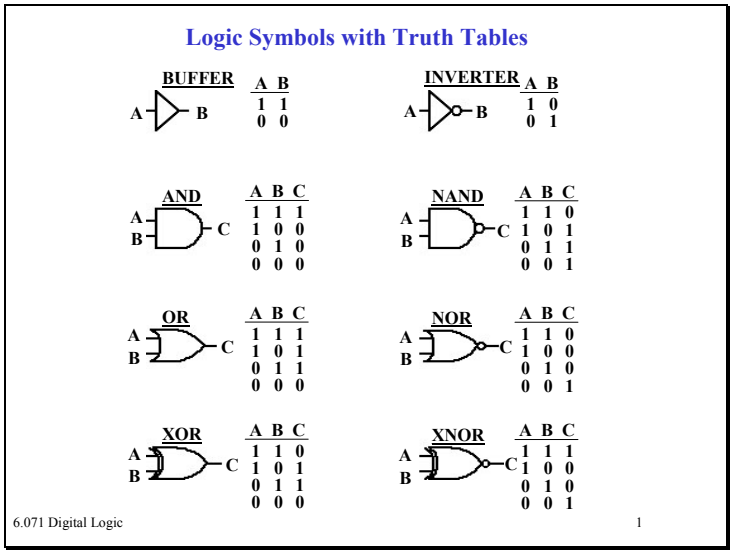
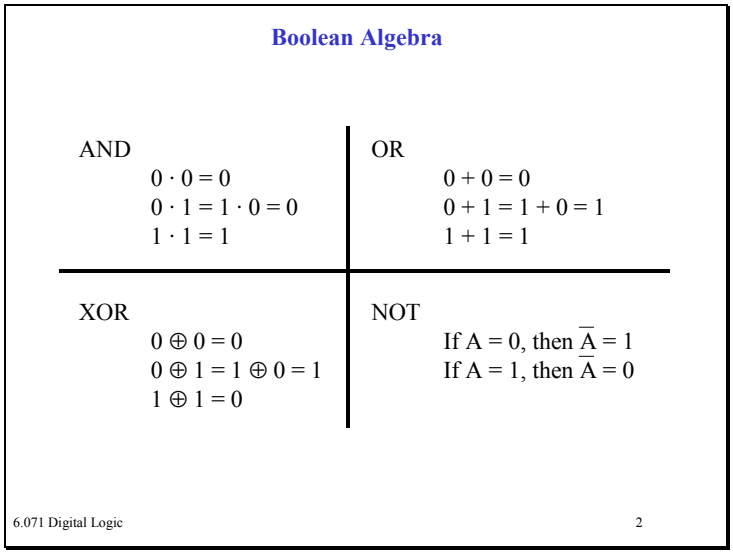
Slide 1



Digital logic can be described in terms of standard logic symbols and their corresponding truth tables. The electronics companies have made transistor based chips that carry out the function of each of these. The horizontal lines represent inputs or outputs (in the examples above read from left to right). The small circles at the outputs on the right correspond to an inverter (performs a logical NOT operation to the output).

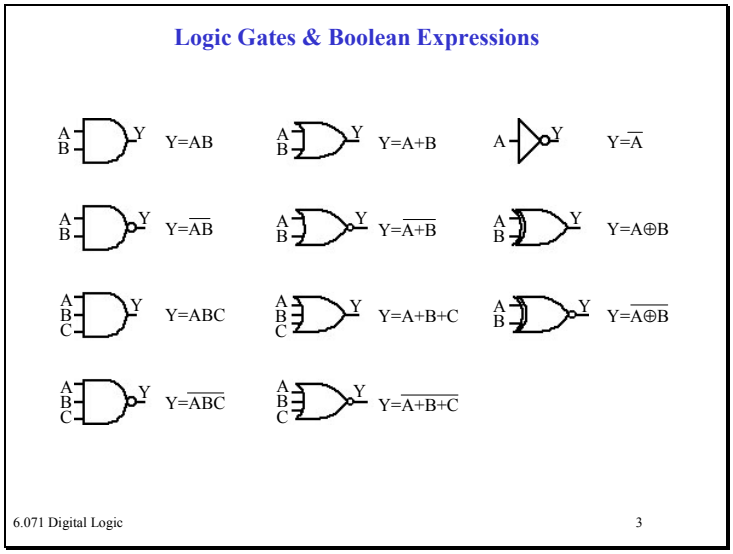
Slide 2



The action of logic circuits can be understood in terms of Boolean logic. We will typically use three elements of this. First you should recall that in our short hand notation 0 is FALSE and 1 is TRUE. The AND operation is indicated by a dot (which is often left out), and the logical table above looks familiar. The OR operation is indicated by a + sign, and the set of outcomes is mostly familiar, but notice that TRUE or TRUE is TRUE. The NOT operation is simply and inversion and is indicated by a bar over the state.

We will also have occasional need for the EXCLUSIVE OR gate which is similar to the OR but is indicated by a + with a circle around it and TRUE EXCLUSIVE OR TRUE is FALSE.

Slide 3



We can rewrite the logic gate in terms of Boolean algebra. Notice that the AND and OR gates can be extended to beyond two inputs, in fact they can have any number.

Slide 4

Table of Logic Identities

1) $A+B = B+A$
2) $AB = BA$
3) $A+(B+C) = (A+B)+C$
4) $A(BC) = (AB)C$
5) $A(B+C) = AB+AC$
6) $(A+B)(C+D) = AC+AD+BC+BD$
7) $\overline{1} = 0$
8) $\overline{0} = 1$
9) $A \cdot 0 = 0$
10) $A \cdot 1 = A$
11) $A+0 = A$
12) $A+1 = 1$
13) $A+A = A$
14) $A\overline{A} = A$
15) $\overline{\overline{A}} = A$
16) $A+\overline{A} = 1$
17) $A\overline{A} = 0$
18) $\overline{A+B} = \overline{A}\,\overline{B}$
19) $\overline{AB} = \overline{A}+\overline{B}$
20) $A+\overline{A}B = A+B$
21) $\overline{A}+AB = \overline{A}+B$
22) $A \oplus B = \overline{A}B+A\overline{B} = (A+B)\overline{AB}$
23) $\overline{A \oplus B} = AB+\overline{A}\,\overline{B}$

6.071 Digital Logic 4

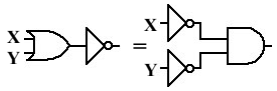
Boolean algebra is simple once you are used to it but takes some getting to know. The above sets of identities are straightforward to show. The first column you probably know (if you say them out in terms of TRUE and FALSE) and second column entries can be figured out and do not need to be memorized.

Slide 5

DeMorgan's Theorem

$\overline{(X+Y)} = \overline{X} \cdot \overline{Y}$

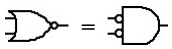
Not of the quantity, X OR Y is equal to
NOT X AND NOT Y



X	Y	X+Y	$\overline{X+Y}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

X	Y	$\overline{X}$	$\overline{Y}$	$\overline{X} \cdot \overline{Y}$
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	0

Compress to



6.071 Digital Logic 5

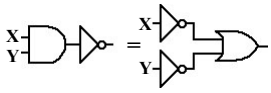
DeMorgan's theorem is probably the most important of the identities that are not immediately known. Here we show that it is true.
Notice that DeMorgan's theorem make concrete the concept that there are many ways of achieving the same truth table. In fact we will demonstrate latter that all logic can be created with NAND gates alone (though this is usually not the most convenient method). Also note that the bubble inverting the input or output of a device can take the place of an inverter.

Slide 6

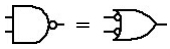
DeMorgan's Theorem 2

A second version is

$$\overline{X \cdot Y} = \overline{X} + \overline{Y}$$



or

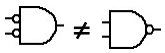


Another versions of DeMorgan's theorem, this time taking a AND type circuit to an OR. Since all logic could be created with NANDs and NANDs can be mapped into NORs then all logic could also be constructed solely out of NORs.

Slide 7

Problem:

Convince yourself that



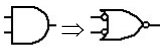
6.071 Digital Logic 7

Write out the truth table of this and convince yourself that you can not simply invert all inputs and outputs and have the same action.

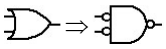
Slide 8

Bubble Pushing

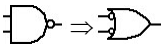
DeMorgan's Theorm says



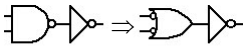
or



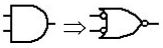
Note: as we quoted DeMorgan's Theorm, it said $\overline{A \cdot B} = \overline{A} + \overline{B}$



Now we add a NOT to each output:



or



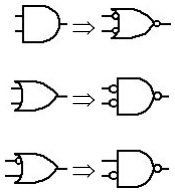
6.071 Digital Logic 8

Now we look at a much more general statement of De Morgan's theorem.

Slide 9

Bubble Pushing 2

1.) change AND to OR
or OR to AND.
2.) invert all inputs and outputs.



This does not sound as elegant or mathematical as DeMorgan's theorem, but it covers a much broader set of examples.

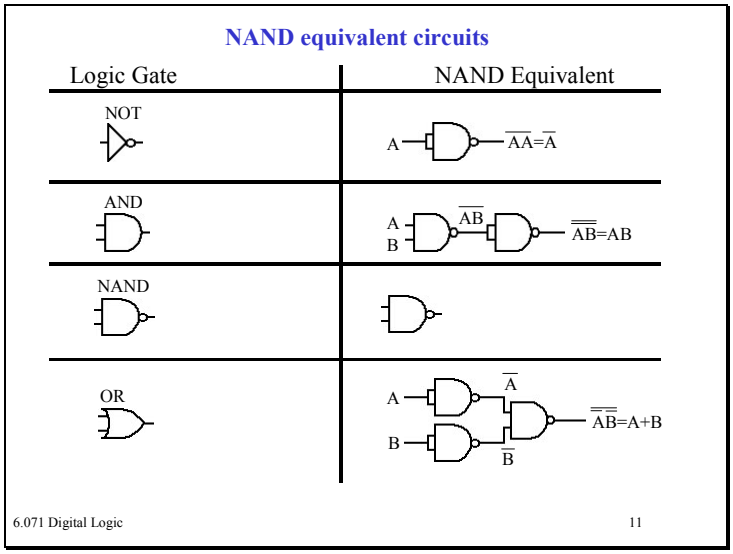
Slide 10

Generalized DeMorgan's Theorem

$$\overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$$
$$\overline{A + B + C} = \overline{A} \cdot \overline{B} \cdot \overline{C}$$

The entire thing can be generalized to any number of inputs and always keeps the same structure.

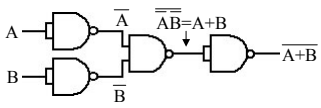
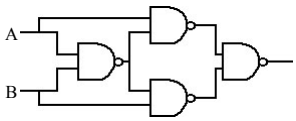
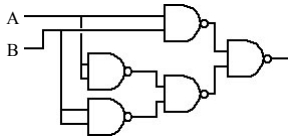
Slide 11



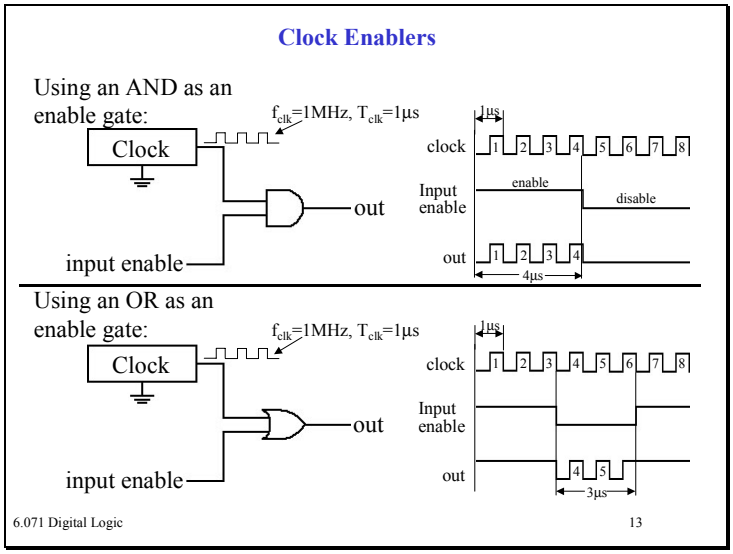
As we said, all logic can be written in terms of NANDs and here are some examples. Notice that in some cases the two inputs of the NAND are tied together to make an inverter.

Slide 12

NAND equivalent circuits 2

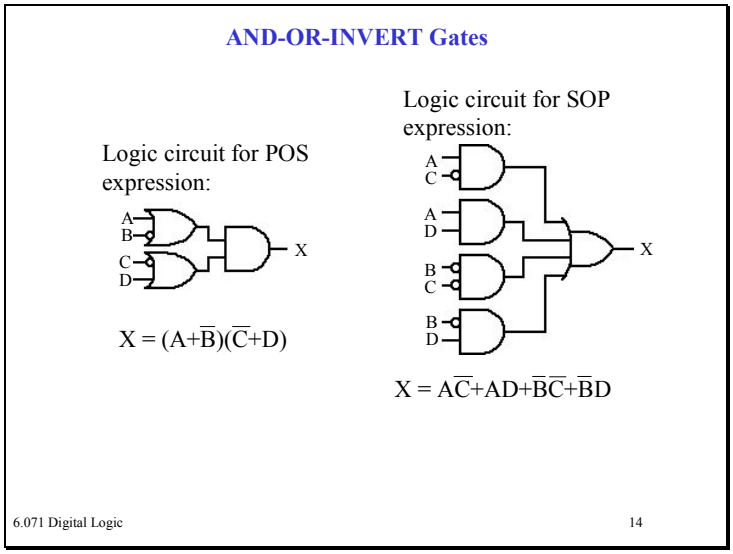
Logic Gate	NAND Equivalent
NOR	
XOR	
XNOR	

Slide 13



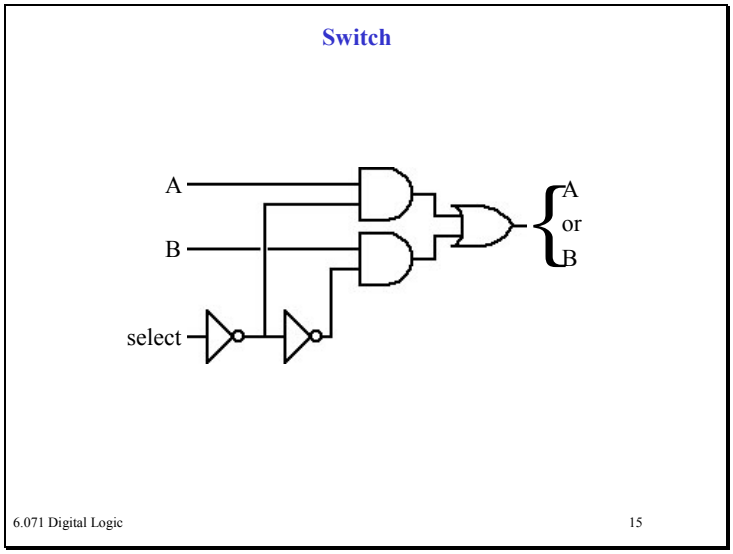
One of the many uses of digital logic is to enable a signal to be transmitted. In this case the clock is the signal and the AND or OR acts to control if it is transmitted. Notice the different actions and the output states when the device is disabled.

Slide 14



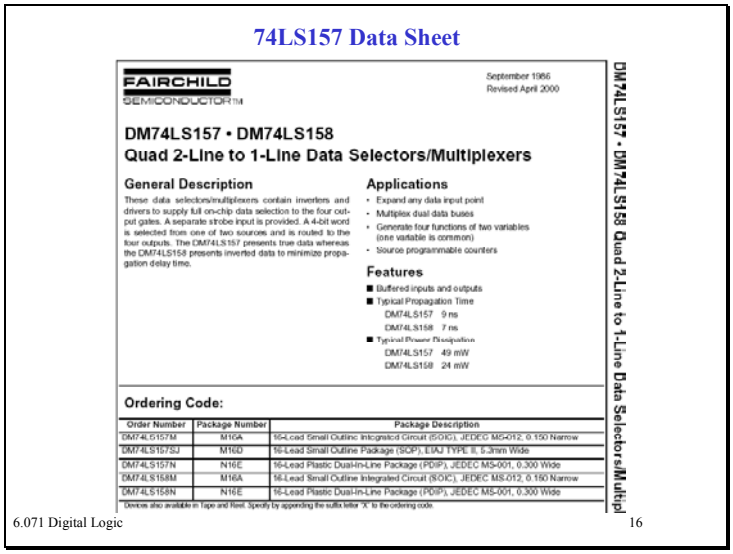
You can directly build digital circuits from Boolean logic. Two two circuits are the same, the left written as a product of sums and the right as a sum of products. There are also approaches to simplifying a network (including software packages).

Slide 15



This shows the simple action of a multiplexer, it takes two inputs and switches the output between them.

Slide 16

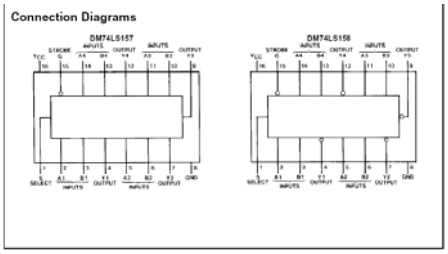


There are higher level devices that are designed for specific applications. Here is a already implemented multiplexer.

Slide 17

74LS157 Data Sheet 2

Connection Diagrams



lexers

DM74LS157 • DM74LS158

Function Table

Inputs				Output Y	
Strobe	Select	A	B	DM74LS157	DM74LS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = HIGH Level
L = LOW Level
X = Don't Care

Slide 18

74LS157 Data Sheet 3

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DM74LS157 Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

DM74LS157 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	S or G			0.2	mA
			A or B			0.1	
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V	S or G			40	µA
			A or B			20	
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V	S or G			−0.8	mA
			A or B			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			9.7	16	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with 4.5V applied to all inputs and all outputs OPEN.

Slide 19

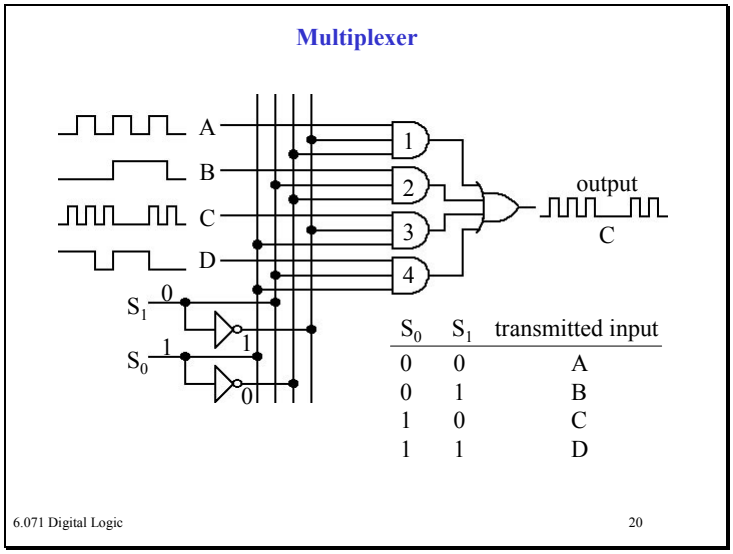
74LS157 Data Sheet 4

DM74LS157 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

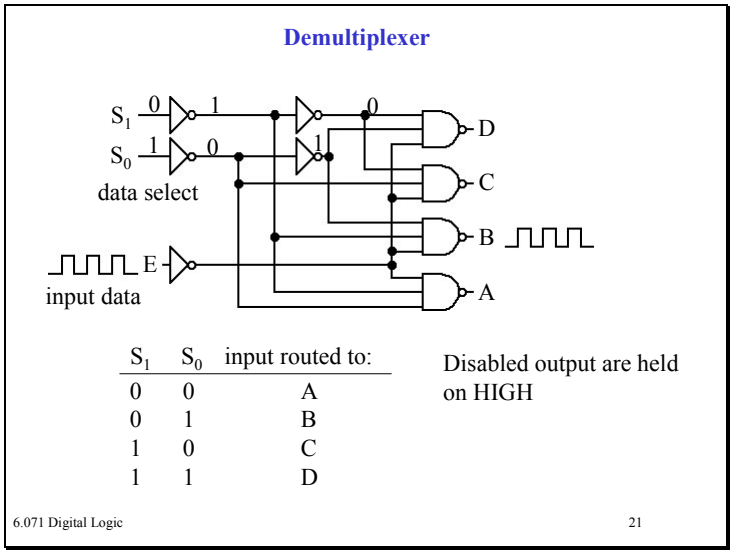
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Data to Y		14		18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Data to Y		14		23	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Strobe to Y		20		24	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Strobe to Y		21		30	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Y		23		28	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Y		27		32	ns

Slide 20



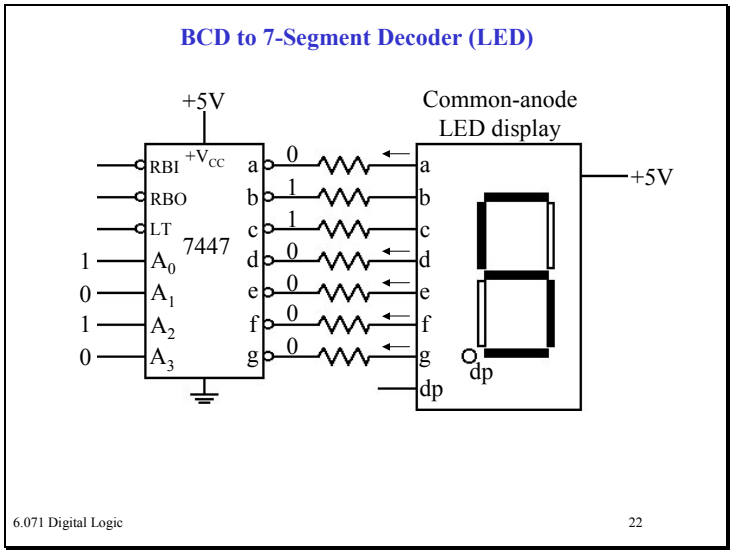
The multiplexer can be expanded to many more lines. Notice that in this case each AND gate has been expanded to three inputs so that the full coding can appear at each. We would need to add one more input to each AND for every power of two increase in the number of inputs. How do you build the same circuit using the ANDs only as enables?

Slide 21



Of course the opposite action can also be implemented. A demultiplexer sends one signal to one of many lines.

Slide 22



Another complex chip, in this case designed to control an LED numeric display.

Slide 23

7447 Data Sheet

March 1998

FAIRCHILD SEMICONDUCTOR

DM7446A, DM7447A
BCD to 7-Segment Decoders/Drivers

DM7446A, DM7447A BCD to 7-Segment Decoders/Drivers

General Description

The 46A and 47A feature active-low outputs designed for driving common-anode LEDs or incandescent indicators directly. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown on a following page. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

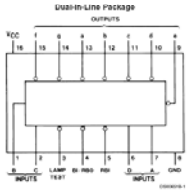
All of the circuits incorporate automatic leading and/or trailing-edge, zero-blanking control (RBI and RBO). Lamp test (LT) of these devices may be performed at any time when the BI/RBO node is at a high logic level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity (by pulsing) or to inhibit the outputs.

Features

- All circuit types feature lamp intensity modulation capability
- Open-collector outputs drive indicators directly
- Lamp-test provision
- Leading/trailing zero suppression

Connection Diagram

Dual-In-Line Package



Order Number DM5447AJ, DM7446AN or DM7447AN
See Package Number J16A or N16E

Slide 24

7447 Data Sheet 2

Absolute Maximum Ratings (Note 1)

Supply Voltage 7V
Input Voltage 5.5V
Operating Free Air Temperature Range
DM54 −55°C to +125°C
DM74 0°C to +70°C
Storage Temperature Range −65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM5447A			DM7447A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			15			15	V
I_{OH}	High Level Output Current (BI/RBO)			−0.2			−0.2	μA
I_{OL}	Low Level Output Current (a thru g)			40			40	mA
I_{OL}	Low Level Output Current (BI/RBO)			8			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Slide 25

7447 Data Sheet 3

'47A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage (BI/RBO)	V_{CC} = Min I_{OH} = Max		2.4	3.7		V
I_{CEX}	High Level Output Current (a thru g)	V_{CC} = Max, V_O = 15V V_{IL} = Max, V_{IH} = Min				250	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.3	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	BI/RBO Others			−4 −1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (BI/RBO)				−4	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 5)	DM54 DM74		60 60	85 103	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

'47A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 120Ω		100	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			100	ns

Slide 26

7447 Data Sheet 4

Function Table

46A, 47A

Decimal or Function	Inputs						BI/RBO	Outputs							Note
	LT	RBI	D	C	B	A	(Note 6)	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	(Note 7)
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 8)
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 9)
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 10)

H = High level, L = Low level, X = Don't Care

Note 6: BI/RBO is a wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

Note 7: The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

Note 8: When a low logic level is applied directly to the blanking input (BI), all segment outputs are high regardless of the level of any other input.

Note 9: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go H and the ripple-blanking output (RBO) goes to a low level (response condition).

Note 10: When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are L.