



**AIN SHAMS UNIVERSITY  
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Electronics and Communications Engineering Department

**Modeling and Characterization of  
VLSI MOSFET for CAD**

**A Thesis**

Submitted in Partial Fulfillment for the Requirements  
of the Degree of Master of Science in Electrical Engineering  
(**Electronics and Communications Engineering**)

Submitted By

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## نمذجة و توصيف الترانزيستور من نوع معدن أكسيد شبة موصل للدوائر المتكاملة واسعة النطاق لبرامج محاكاة الدوائر الالكترونية

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### مستخلص

علاء الدين الراعى محمد. نمذجة و توصيف الترانزيستور من نوع معدن أكسيد شبه موصل للدوائر المتكاملة واسعة

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تم القيام بتنفيذ نموذج إستاتيكي للترانزستور من نوع معدن - أكسيد - شبه موصل بغرض تطبيقه في برامج محاكاة الدوائر. وقد تم الإهتمام في هذه الدراسة بنمذجة عمل الترانزستور في حالة وجود تطعيم غير منتظم للقناة. كما تم الإهتمام بتصميم النموذج ليشمل تطبيقات الدوائر التناظرية و العددية، مما وضع متطلبات عالية من الدقة في النموذج المقترح. وقد تم بناء النموذج على وصف توصيل التيار في القناة بدلالة جهد السطح عند كل من المنبع والمصب. ومن خصائص النموذج الذى تم بناؤه أنه قابل للتطبيق على النبائط المصغرة كما إنه متصل من منطقة تحت جهد العتبة حتى منطقة الانقلاب الشديد. وقد تم البرهنة على دقة النموذج في حالات متعددة من جهود الإنحياز وأبعاد النبائط. وجدير بالذكر أن خصائص النموذج من حيث الدقة والإتصال والإستقرار ترجع الى الأساس الفيزيائى لهذا النموذج من حيث توصيف الظواهر والمؤثرات الداخلة في عمل النبطية. وقد تم تنفيذ هذا النموذج في برنامج محاكاة الدوائر ELDO عن طريق لغة HDL-A و بذلك يمكن إستخدام النموذج في محاكاة الدوائر المكونه من نبائط معدن - أكسيد - شبه موصل. كما تم أيضا عمل برنامج قياس آلى بأستخدام برنامج LabVIEW للقيام بتوصيف الترانزيستور من نوع MOS. هذا بالإضافة الى برنامج آلى لاستخراج بارمترات النموذج من نتائج القياس العملية.

الكلمات المفتاحية: الدوائر المتكاملة شديدة الاتساع- النمذجة - محاكاة الدوائر الالكترونية

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﴿قَالُوا سُبْحَانَكَ لَا عِلْمَ لَنَا إِلَّا مَا عَلَّمْتَنَا إِنَّكَ أَنْتَ الْعَلِيمُ الْحَكِيمُ﴾

(البقرة ٣٢)

## ملخص الرسالة

إن المتطلبات التي يجب توافرها في النموذج المعد لخدمة برامج محاكاة الدوائر الإلكترونية جد متشعبة و متداخلة. فيجب أن يكون النموذج طبيعي المنشأ، وأن يمثل بدقة الآلية الإلكترونية الداخلية للنبائط، متضمنا الوصف الهيكلي للنبائط، كما يجب أن يتصل برباط محكم بتكنولوجيا التصنيع ونسق التصميم بالإضافة إلى الخواص الكهربائية. ويجب أن يمثل النموذج بدقة خواص النبائط الكهربائية خلال مدى التشغيل اللازم و تحت كافة الظروف.

كما أن استحداث النماذج التحليلية الملائمة لبرامج محاكاة الدوائر قد تدفعنا إلى استخدام معادلات شبة طبيعية تحتوى بدورها على بارامترات لا تنتمي إلى مجموعة قيم وحيدة، لذلك فلتحقيق ماأرئنا في الحصول على نموذج جيد لبرامج محاكاة الدوائر، يجب استحداث برامج قياس آلية بالإضافة إلى خوارزم مناسب لاستخلاص أفضل قيم لهذه البارامترات حتى يكون النموذج ممثلا دقيقا للنتائج العملية.

في هذه الرسالة تم استكمال عملية إعداد نموذج للترانزيستورات من نوع معدن أكسيد شبة موصل صالح للتطبيقات التماثلية و الرقمية (يتم إعداد هذا النموذج بمعمل الدوائر المتكاملة)، عن طريق إدخال الظواهر المصاحبة لعدم انتظام تطعيم القناة. كما تم استحداث برامج آلية علي الحاسب الشخصي للقيام بعملية القياس اللازمة لتوصيف الترانزيستورات، وتم استحداث برنامج لاستخلاص قيم دقيقة لبارامترات النموذج استنادا على خوارزم ليفنبرج-ماركودت، ويتميز هذا البرنامج بأنه لا يعتمد على النموذج ويمكن استخدامه في أي تطبيق آخر يتطلب استخراج البارامترات بطريقة أقل خطأ في المربعات لمعادلات غير خطية.

وقد تم تقسيم الرسالة إلى أربعة فصول:

الفصل الأول: يعطي ملخص لتوصيف الترانزيستور من نوع معدن أكسيد شبه موصل، كما يناقش مفهوم نمذجة الترانزيستورات لبرامج محاكاة الدوائر والقواعد التي يجب تحقيقها للقيام بعمل النموذج للدوائر التناظرية.

الفصل الثاني: يتناول إظهار النموذج المقترح مع توضيح ظواهر القناة الضيقة والقصيرة وكيفية توصيفها بالنموذج، كما تم شرح كيفية استكمال النموذج ليشمل القنوات الغير منتظمة التطعيم وتم التحقق من دقة هذا الاستكمال بالمقارنة مع النتائج العملية.

الفصل الثالث: تم استعراض طريقة القياس الآلية المستحدثة والنبائط المطلوبة، كما تم توضيح بارمترات النموذج وكيفية استخراجها بطريقة جماعية لتلائم مجموعة من النبائط ذات تكنولوجيا تصنيع واحدة.

الفصل الرابع: تم استعراض المبادئ الرياضية المستخدمة في خوارزميات أقل خطأ للمربعات للدوال الغير خطية، وتم التركيز على الخوارزم المستخدم وهو ليفنبرج-ماركودت. وقد لوحظ التطابق القوي بين النتائج التي تم الحصول عليها من القياسات العملية ونتائج النموذج المبنية علي قيم البارمترات المستخلصة من البرنامج المستحدث في هذه الرسالة.

# ABSTRACT

**Alaa El-Din El-Raey Mohamed. Modeling and Characterization of VLSI MOSFET for CAD. Unpublished Master of Science dissertation, University of Ain Shams, 1996.**

The main objective of this dissertation is to develop a *circuit-level* dc current model for the MOS transistor. Special care is taken to the modeling of the transistors of non uniform doping. The model is to be used for *analog* and digital circuit design. This puts heavy demands on the accuracy provided by the model. The model is based on the representation of current transport in a sheet channel in terms of the surface potential conditions at the source and drain boundaries. The model is scaleable and results in continuous device characteristics under all operating conditions, from deep subthreshold to strong inversion. Accuracy of the model is demonstrated over a wide range of device geometries and terminal voltages. The features of scalability, continuity, and accuracy are attributed to the physical representation of all important effects occurring in the MOS transistor. The model is implemented under the circuit simulator *ELDO* using HDL-A language and can be used to simulate dc MOSFET circuits.

Also we develop an automated measurements program works under LabVIEW software to characterize the MOS transistors, as well as an automated program to extract the model parameters from the measured characteristics.

## Key Words

VLSI - MOSFET- CAD - Modeling - Simulation

# SUMMARY

The requirements to be satisfied by a CAD device model for use in circuit simulation are demanding and essentially in conflict. The model should be physically based, representing faithfully the internal electronic mechanisms and the implications of device structure, and should provide a coherent link between fabrication technology, design layout and electrical performance. It should give accurate and continuous representation of device electrical characteristics over the full range of operating modes and conditions.

The required analytical model to be suitable for CAD applications, may force us to the development of some quasi-physical equations and the required parameters in this case do not normally relate to any single identifiable physical set of parameters, so to achieve our purpose to obtain good model for CAD applications, an automated measurement setup must be provided beside an optimization algorithm to best fit the obtained experimental data.

In this work we continue the development of a MOSFET model for analog and digital applications, which is carried out in the ICL lab, by introducing the non-uniform doping effects. Also automated programs for MOSFET characterization, as well as an optimization program based on the Levenberg-Marquadt algorithm have been developed. The developed optimization program is model independent and can be used for any nonlinear least square parameter extraction problem. The thesis is divided into four chapters:

The first chapter, gives a quick review to the MOSFET characteristics since it is our target for modeling and characterization. The concept of

MOSFET modeling for circuit CAD and the required criteria to be satisfied in the model development has been discussed.

In the second chapter, the proposed model is presented, the short channel effects which are included in the model are outlined with their governing equations. Also the extension to the non-uniform doping are presented and is verified by comparison with experimental results.

The third chapter, presents the suggested measurement procedure and the required devices, also it provides the model parameters and an extraction strategy called the group strategy, which is best fit a group of devices based on the same technology, but may have not strong fit for each device alone.

The mathematical foundation required for non linear least square algorithms are presented in chapter four with focusing on the used algorithm called Levenberg-Marqudet algorithm. A good agreement has been observed between the proposed model results and the experimental results obtained using the suggested measurement procedure.

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Alaa El-Raey  
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# CONTENTS

<b>List of Figures .....</b>	<b>viii</b>
<b>List of Tables .....</b>	<b>xi</b>
<b>List of Symbols .....</b>	<b>xii</b>
<b>Abbreviations.....</b>	<b>xvii</b>

## CHAPTER 1

<b>MOSFET Modeling for CAD.....</b>	<b>1-22</b>
1.1 Introduction.....	1
1.2 Basic MOSFET electrostatics.....	1
1.2.1 Surface and Fermi Potentials.....	2
1.2.2 MOS Charges.....	3
1.2.2.1 The Semiconductor Charge.....	4
1.2.2.2 Oxide Charges .....	6
1.2.2.3 Interface Trap Charge.....	6
1.2.3 The Flat Band Voltage.....	10
1.3 The MOSFET Mobility .....	11
1.4 MOSFET Modeling .....	12
1.4.1 Numerical MOSFET Modeling.....	13
1.4.2 Analytical MOSFET Modeling .....	15
1.5 MOSFET Modeling for Analog Circuit CAD.....	15
1.5.1 The Special Nature of Analog Modeling Needs .....	17
1.6 CAD requirements .....	18
1.6.1 Nonconvergence .....	19
1.6.2 The smoothing function.....	21
1.7 Overview of various simulators.....	22

## CHAPTER 2

<b>Model Description .....</b>	<b>23-58</b>
2.1 Introduction.....	23

2.2 Gradual Channel approximation (GCA) .....	24
2.3 The long channel current model.....	25
2.3.1 The classical long-channel Pao and Sah model .....	27
2.3.2 The charge-sheet based models.....	28
2.3.3 Bulk Charge Model .....	29
2.3.4 Square law model .....	29
2.3.5 Approximate models .....	30
2.3.6 Modified charge sheet model.....	31
2.4 The Short Channel Model .....	33
2.4.1 Channel Length Modulation .....	35
2.4.2 Velocity Saturation.....	37
2.4.3 Drain induced barrier lowering.....	40
2.4.4 Series Resistance .....	46
2.5.5 Impact Ionization and the Substrate Current .....	48
2.5 Narrow Channel Effect.....	50
2.6 Non uniform doping [40].....	51
2.6.1 Non uniform doping profile .....	51
2.6.2 Model implementation .....	53
2.6.3 Effect on threshold voltage .....	54
2.7 Temperature effects .....	57

## CHAPTER 3

### **Measurements and Parameter Extraction ..... 59-78**

3.1 Introduction .....	59
3.2 Model Parameters .....	59
3.3 Measurement Procedure .....	62
3.3.1 Required equipment and samples.....	62
3.3.2 Measurement procedure .....	64
3.3.3 Results .....	65
3.4 Parameter extraction .....	67
3.4.1 Extraction Strategy .....	67
3.4.2 Parameters extraction procedure.....	68
3.4.2.1 Theory.....	68
3.4.2.2 Extraction Results .....	74

## CHAPTER 4

### **Optimization Algorithm and Results ..... 79-94**

4.1 Introduction .....	79
4.2 Nonlinear Least Squares Optimization .....	80
4.2.1 Algorithm Description.....	81
4.2.2 Calculation of the Jacobian Matrix .....	84

4.2.3 Parameters Constraints .....	84
4.2.4 Termination Criteria .....	85
4.3 Results.....	85
4.3.1 Obtained parameters .....	86
4.4 Comparison with simulation results .....	86
4.5 Other Models .....	93
4.6 Conclusion .....	93
<b>References .....</b>	<b>95-98</b>
<b>Appendix A</b>	
<b>Measurement program in G language .....</b>	<b>99-104</b>
<b>Appendix B</b>	
<b>Model Formulation in HDL-A Language .....</b>	<b>105-122</b>

## List Of Figures

<b>Figure 1.1</b> MOSFET structure .....	2
<b>Figure 1.2</b> Comparison of the energy band diagram of an inverted n-channel MOS for: (a) the equilibrium case and (b) the nonequilibrium case (applied drain bias).....	3
<b>Figure 1.3</b> The MOS charges and associated electric field and potential.....	4
<b>Figure 1.4</b> Semiconductor charges versus $\psi_s$ for two values of the quasi Fermi potential $\phi_c$ . .....	5
<b>Figure 1.5</b> Band-bending diagram showing how interface traps change occupancy with gate bias. The sample is p-type. (a) No gate bias; (b) negative gate bias; (c) positive gate bias.....	7
<b>Figure 1.6</b> Interface trap charge versus the surface potential.....	10
<b>Figure 1.7</b> (a) $I_D$ - $V_{DS}$ characteristics as resulting from measurement (solid line) and simulation (dashed line). (b) The output conductance resulting from taking the slopes in (a). .....	16
<b>Figure 1.8</b> Iterations around a model discontinuity.....	20
<b>Figure 1.9</b> The smoothing function .....	21
<b>Figure 2.1</b> The MOSFET structure.....	24
<b>Figure 2.2</b> Drain current components: The drift current, $I_{d1}$ , and the diffusion current, $I_{d2}$ . The device has $W/L=50\mu/6\mu$ , $N_{sub}=5E16\text{ cm}^{-3}$ , and $T_{ox}=40\text{ nm}$ . [30].....	32
<b>Figure 2.3</b> Drain current for different interface trapped charge densities. Positive $D_{it}$ are donor like traps, while negative $D_{it}$ are acceptor like. The device has $W/L=50\mu/6\mu$ , $N_{sub}=5E16\text{ cm}^{-3}$ , and $T_{ox}=40\text{ nm}$ [30].....	32
<b>Figure 2.4</b> Schematic representation of a MOSFET in saturation, where the channel is divided into a non-saturated region and a saturated region.....	36
<b>Figure 2.5</b> Diagram showing (a) the Gaussian box used in the quasi-two-dimensional analysis, (b) the boundary conditions for solving eq. (2.4.14).....	40
<b>Figure 2.6</b> Calculated surface potential along the channel for different channel lengths. The dashed lines show the data for $V_{DS}=0.05\text{V}$ and the solid lines show the data for $V_{DS}=1.5\text{V}$ . .....	43
<b>Figure 2.7</b> Calculated $V_{th}$ shifts versus channel length at $V_{DS} = 0.05\text{ V}$ . The continuous line denotes numerical calculations, while the dashed one is obtained by eq. 2.4.23.....	44

<b>Figure 2.8</b> Calculated $V_{th}$ shifts versus the drain voltage $V_{DS}$ at a channel length of $0.3\mu m$ . The continuous line denotes numerical calculations, while the dashed one is obtained by eq. 2.4.23.[35] .....	45
<b>Figure 2.9</b> MOSFET with parasitic source and drain resistance.....	47
<b>Figure 2.10</b> Depletion charge along the width of the transistor.....	50
<b>Figure 2.11</b> Comparison between Gaussian profile and suggested profile using equation (2.6.1) for $n=0.2$ and $n=10$ .....	52
<b>Figure 2.12</b> Obtained results for sample devices in Table 2.2 .....	55
<b>Figure 2.13</b> Percentage error in the threshold voltage calculations for sample devices in Table 2.2.....	56
<b>Figure 2.14</b> Drain current dependence on the substrate bias at subthreshold region . .....	56
<b>Figure 2.15</b> Variation of the body factor ( $\gamma$ ) parameter for sample device MOS3.....	57
<b>Figure 3.1</b> Automated measurement using HP4142 .....	63
<b>Figure 3.2</b> Automated measurement connections.....	63
<b>Figure 3.3</b> Distribution of device's sizes used for parameter extraction.....	64
<b>Figure 3.4</b> User interface for the measurement program.....	65
<b>Figure 3.5</b> Drain Current versus Gate voltage for low drain voltage ( $10mV$ ) [ $W/L=50\mu/1.2\mu$ ].....	65
<b>Figure 3.6</b> Drain Current versus Gate voltage for high drain voltage ( $5V$ ) [ $W/L=50\mu/1.2\mu$ ].....	66
<b>Figure 3.7</b> Drain Current versus Drain voltage for $V_{bs}=0$ [ $W/L=50\mu/1.2\mu$ ].....	66
<b>Figure 3.8</b> The variation of $I_D/g_m^{1/2}$ as a function of gate voltage for different channel lengths. ....	70
<b>Figure 3.9</b> The variation of $1/m_1^2$ as a function of channel length.....	70
<b>Figure 3.10</b> The variation of $R_0$ as a function of the mask channel length $L71$	
<b>Figure 3.11</b> $\Delta V_{th}$ as a function of the effective channel length.....	73
<b>Figure 3.12</b> Determination of Impact ionization parameters.....	74
<b>Figure 3.13</b> Drain current versus gate voltage for long device ( $6\mu m$ ) .....	75
<b>Figure 3.14</b> Transconductance versus gate voltage for long device ( $6\mu m$ )	75
<b>Figure 3.15</b> Drain current versus drain voltage for long device ( $6\mu m$ ) .....	76
<b>Figure 3.16</b> Drain current versus gate voltage for short device ( $1\mu m$ ) .....	76
<b>Figure 3.17</b> Transconductance versus gate voltage for short device ( $1\mu m$ )	77
<b>Figure 3.18</b> Drain current versus drain voltage for short device ( $1\mu m$ ).....	77
<b>Figure 4.1.a</b> Drain current versus gate voltage for drain voltage= $10mV$ [Linear Scale].....	88
<b>Figure 4.1.b</b> Drain current versus gate voltage for drain voltage= $10mV$ [Log Scale].....	88
<b>Figure 4.2</b> Transconductance versus gate voltage for drain voltage= $10mV$	89

**Figure 4.3.a** Drain current versus gate voltage for drain voltage=5V ..... 89

**Figure 4.3.b** Drain current versus gate voltage for drain voltage=5V ..... 90

**Figure 4.4** Transconductance versus gate voltage for drain voltage=5V ... 90

**Figure 4.5** Drain current versus gate voltage for different drain voltages.. 91

**Figure 4.6** Drain current versus drain voltage for different gate voltages.. 91

**Figure 4.7** Output conductance versus drain voltage for different gate  
voltage..... 92

**Figure 4.8**  $g_m/I_d$  versus Drain current ..... 92

**Figure A.1** Measurement program control panel ..... 99

**Figure A.2** Measurement program block diagram..... 100-103

# List of Tables

<b>Table 1.1</b> <i>Overview of various simulators</i> .....	22
<b>Table 2.1</b> <i>Comparison of Long-Channel and Short-Channel MOSFETs</i> <i>C/Cs</i> .....	34
<b>Table 2.2</b> <i>Sample devices parameters</i> .....	55
<b>Table 3.1</b> <i>Model parameters</i> .....	60
<b>Table 3.2</b> <i>Obtained parameters</i> .....	74
<b>Table 4.1</b> <i>Obtained parameters</i> .....	86
<b>Table 4.2.</b> <i>Comparison between SPICE Level (2) model, BSIM model,</i> <i>aMOS model, and this work</i> .....	94

# LIST OF SYMBOLS

$AI$	Impact ionization pre-exponential constant (1/V)
$BI$	Impact ionization exponent constant (V/cm)
$C_d$	Depletion capacitance per unit area (F/cm <sup>2</sup> )
$C_G$	Total gate capacitance per unit area (F/cm <sup>2</sup> )
$C_{it}$	Interface trap charge capacitance per unit area (F/cm <sup>2</sup> )
$C_{ox}$	Gate oxide capacitance per unit area (F/cm <sup>2</sup> )
$C_s$	Total surface capacitance per unit area (F/cm <sup>2</sup> )
$d_{inv}$	Thickness of the inversion layer (50 - 100 Å)
$D_{it}$	Total interface trapped charge density per unit area, and per unit energy (cm <sup>-2</sup> .eV <sup>-1</sup> )
$D_{ita}$	Acceptor like interface trapped charge density per unit area, and per unit energy (cm <sup>-2</sup> .eV <sup>-1</sup> )
$D_{itd}$	Donor like interface trapped charge density per unit area, and per unit energy (cm <sup>-2</sup> .eV <sup>-1</sup> )
$E_c$	The lowest energy level of the conduction band (eV)
$E_f$	Fermi level (eV)
$E_{fn}$	Electrons quasi-Fermi level (eV)
$E_{fp}$	Holes quasi-Fermi level (eV)
$E_g$	Energy band gap (eV)
$E_i$	Intrinsic level (eV)
$E_t$	Interface trap level (eV)
$E_v$	The upper energy level of the valence band (eV)
$F_{max}$	The critical electric field in the channel at which carriers move with their limiting velocity $v_{max}$ (V/cm)
$F_x$	The electric field component parallel to the Si-SiO <sub>2</sub> interface (V/cm)
$F_y$	The electric field component perpendicular to the Si-SiO <sub>2</sub> interface (V/cm)

$F_{yb}$	The electric field component perpendicular to the Si-SiO <sub>2</sub> interface just below the inversion layer (V/cm)
$F_{ys}$	The electric field component perpendicular to the Si-SiO <sub>2</sub> interface at the surface (V/cm)
$f(E)$	Fermi-Dirac distribution function
$g_m$	Transconductance (A/V)
$g_{mb}$	Bulk transconductance (A/V)
$g_d$	Drain conductance (A/V)
$I_D$	Drain current (A)
$I_{D1}$	Drift current component (A)
$I_{D2}$	Diffusion current component (A).
$I_{Dsat}$	Drain current at saturation (A)
$I_{st}$	Substrate current due to impact ionization (A)
$k$	Boltzmann constant (=1.380662E-23) (J/K)
$L$	Mask Channel length (cm)
$L_{eff}$	Effective channel length (cm)
$L_s$	The width of the source depletion region (cm)
$L_d$	The width of the drain depletion region (cm)
$\Delta L$	Channel shortening in the saturation region (cm)
$l_d$	Drain induced barrier lowering characteristic length (cm)
$N_A$	Acceptor impurity density per unit volume (cm <sup>-3</sup> )
$N_D$	Donor impurity density per unit volume (cm <sup>-3</sup> )
$N_{sub}$	Substrate impurity doping density per unit volume (cm <sup>-3</sup> )
$n$	Electron density per unit volume (cm <sup>-3</sup> )
$n_i$	Intrinsic carrier density per unit volume (cm <sup>-3</sup> )
$p$	Hole density per unit volume (cm <sup>-3</sup> )
$Q_B$	Depletion (bulk impurity) charge density per unit area (C/cm <sup>2</sup> )
$Q_{ox}$	Effective oxide charge per unit area at the Si-SiO <sub>2</sub> interface (C/cm <sup>2</sup> )
$Q_i$	Inversion charge density per unit area (C/cm <sup>2</sup> )
$Q_{it}$	Interface trapped charge density per unit area (C/cm <sup>2</sup> )
$Q_{it}'$	= $Q_{it}(\psi_s, \phi_c) - Q_{it}(0, 0)$ (C/cm <sup>2</sup> )

$Q_{ita}$	Acceptor like interface trap charge density per unit area (C/cm <sup>2</sup> )
$Q_{itd}$	Donor like interface trapped charge density per unit area (C/cm <sup>2</sup> )
$Q_{sc}$	Semiconductor charge density per unit area (C/cm <sup>2</sup> )
$q$	Magnitude of the electronic charge (=1.60219E-19) (C)
$R_d$	Drain parasitic series resistance ( $\Omega$ )
$R_s$	Source parasitic series resistance ( $\Omega$ )
$R_t$	Total parasitic series resistance ( $\Omega$ )
$SF$	The smoothing function
$T$	Temperature ( $^{\circ}$ K)
$T_{ox}$	Gate oxide thickness (cm)
$V_{bi}$	Built-in voltage of the drain and source junctions (V)
$V_D$	Drain voltage referenced to the bulk potential (V)
$V_{DS}$	Drain to Source voltage (V)
$V_{DSI}$	Drain to Source voltage taking into account velocity saturation effects (V)
$V_{DSsat}$	Drain to Source voltage at the saturation point (V)
$V_{FB}$	Real flat band voltage (V)
$V_{FBD}$	Effective Flat band voltage including the effect of the interface trap charge (V)
$V_{FB}'$	Effective Flat band voltage (V)
$V_G$	Gate voltage referenced to the bulk potential (V)
$V_{GS}$	Gate to Source voltage (V)
$V_{GF}$	= $V_G - V_{FB}$ (V)
$V_{GT}$	= $V_G - V_T$ (V)
$V_S$	Source voltage referenced to the bulk potential (V)
$V_T$	Gate to bulk voltage at threshold (V)
$V_{th}$	Gate to source voltage at threshold (V)
$v_{max}$	Maximum velocity of the carriers in the channel (cm/s.)
$W$	Channel width (cm)
$w$	Depletion region width (cm)
$X_{dep}$	Depletion region width at threshold (cm)

$y_j$	Source/drain junctions depth (cm)
$\beta$	$1/\phi_t$ ( $V^{-1}$ )
$\beta_{eff}$	Transconductance parameter using $\mu_{eff}$ ( $A/V^2$ )
$\beta_{eff}'$	Transconductance parameter using $\mu_{eff}'$ ( $A/V^2$ )
$\beta_g$	Transconductance parameter using $\mu_g$ ( $A/V^2$ )
$\beta_o$	Transconductance parameter using $\mu_o$ ( $A/V^2$ )
$\gamma$	Body factor ( $V^{1/2}$ )
$\epsilon_{ox}$	Permittivity of $SiO_2$ (F/cm)
$\epsilon_s$	Permittivity of Si (F/cm)
$\theta$	Normal mobility coefficient ( $1/V$ )
$\mu_{eff}$	Effective electron mobility in the channel, taking into consideration the effect of both normal, and lateral field scattering ( $cm^2/V.s$ )
$\mu_{eff}'$	Effective electron mobility in the channel, taking into consideration the effect of both normal, and lateral field scattering, in addition to the parasitic series resistance $R_s$ ( $cm^2/V.s$ )
$\mu_g$	Effective electron mobility in the channel, taking into consideration the effect of the normal field scattering only ( $cm^2/V.s$ )
$\mu_n$	Electron surface mobility in the channel ( $cm^2/V.s$ )
$\rho$	Space charge density in the semiconductor ( $C/cm^3$ )
$\phi_c$	The Quasi-Fermi potential (the difference between $E_{fn}$ at the surface of the semiconductor and $E_{fp}$ in the bulk of the semiconductor) (V)
$\phi_f$	The difference between $E_i$ and $E_f$ in the bulk of the semiconductor (V)
$\phi_m$	Metal work function (eV)
$\phi_{ms}$	Metal-semiconductor work function difference (eV)
$\phi_s$	Semiconductor work function (eV)
$\phi_{si}$	Surface potential referenced to the source at threshold (V)
$\phi_t$	Thermal voltage (V)

$\phi_v$	Channel potential induced by the drain-source bias (V)
$\psi_s$	Surface potential referenced to the bulk potential (V)
$\psi_{sw}$	Estimated surface potential $\psi_s$ in the weak inversion regime (V)
$\psi_{ss}$	Estimated surface potential $\psi_s$ in the strong inversion regime (V)
$\psi_{s0}$	Surface potential at the source end of the channel referenced to the bulk (V)
$\psi_{sL}$	Surface potential at the drain end of the channel referenced to the bulk (V)
$\psi_{s0}'$	Surface potential at the source end of the channel referenced to the bulk, used in the calculation of the drift current component (V)
$\psi_{sL}'$	Surface potential at the drain end of the channel referenced to the bulk, used in the calculation of the drift current component (V)

# Abbreviations

<b>CAD</b>	Computer Aided Design
<b>CPU</b>	Central Processing unit
<b>CMOS</b>	Complementary Metal Oxide Semiconductor
<b>CLM</b>	Channel Length Modulation
<b>DIBL</b>	Drain Induced Barrier Lowering
<b>GCA</b>	Gradual Channel Approximation
<b>MOSFET</b>	Metal Oxide Semiconductor Field Effect Transistor
<b>VLSI</b>	Very Large Scale Integration
<b>HDL-A</b>	Hardware Description Language - Analog part
<b>LabVIEW</b>	Laboratory Virtual Instrument Engineering Workbench
<b>HP VEE</b>	Hewlett Packard Visual Engineering Environment



# CHAPTER 1

## MOSFET Modeling for CAD

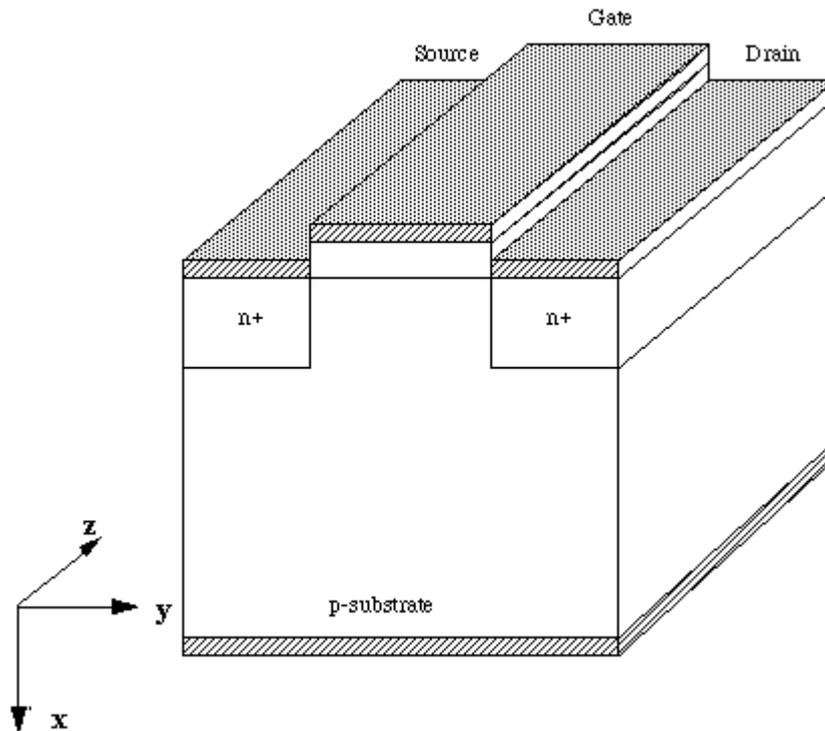
### 1.1 Introduction

The requirements to be satisfied by a CAD device model for use in circuit simulation are demanding and essentially in conflict. The model should be physically based, representing faithfully the internal electronic mechanisms and the implications of device structure, and should provide a coherent link between fabrication technology, design layout and electrical performance. It should give accurate and continuous representation of device electrical characteristics over the full range of operating modes and conditions.

In the following chapter we shall deal with the MOSFET structure and its basic governing equations, and also we shall discuss the basic requirements implied by CAD applications in order to develop a good model of the MOSFET suitable for analog CAD applications.

### 1.2 Basic MOSFET electrostatics

In the following section we shall review the basic MOSFET characteristics, and governing equations which will be used to get a suitable model for circuit CAD applications. The MOSFET structure is shown in Fig. 1.1



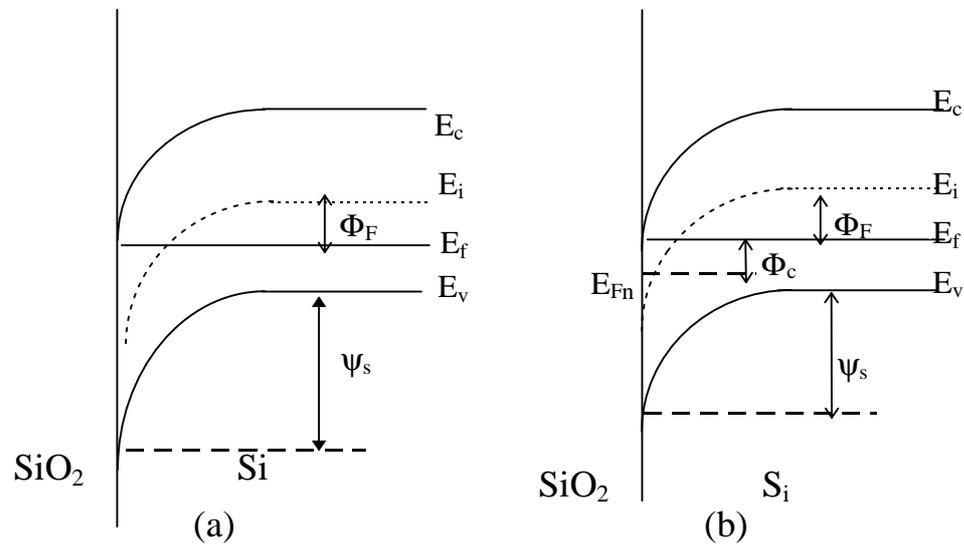
**Figure 1.1** MOSFET structure

### 1.2.1 Surface and Fermi Potentials

Fig. 1.2a shows the energy band diagram at the middle of the channel. This case corresponds to a device in equilibrium ( $V_S=V_D=0$ ) and an applied gate voltage  $V_G$  that makes the device in inversion i.e.  $\psi_s > 2\phi_f$ .

Fig. 1.2b shows the same device in the non-equilibrium case ( $V_D > 0$ ), such that we use the quasi-Fermi levels  $E_{fn}$  and  $E_{fp}$  [1], instead of the Fermi level  $E_f$ . A split in the quasi-Fermi level equal to  $\phi_c$  is noticed due to the applied drain bias. This shift is equal to  $V_D$  at the drain side of the channel. This is equivalent to assuming that the electron quasi-Fermi levels remains essentially constant over the transition region (between the channel and the drain)<sup>1</sup>.  $\phi_c$  is then the Fermi potential induced by the drain-source bias. In the general case where  $V_S \neq V_D \neq 0$ , we have  $V_S < \phi_c < V_D$ .

<sup>1</sup> A corresponding assumption is often made in *pn* junction theory [2]

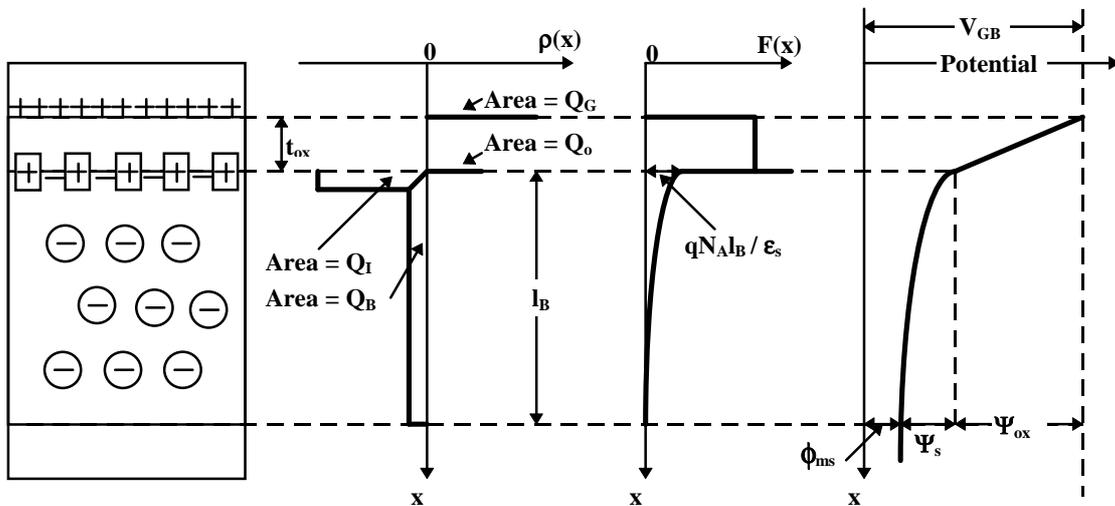


**Figure 1.2** Comparison of the energy band diagram of an inverted  $n$ -channel MOS for: (a) the equilibrium case and (b) the nonequilibrium case (applied drain bias).

A potential convention is always used;  $\psi_s$ ,  $\phi_f$ , and  $\phi_c$  are positive downward (in the normal operation of the  $n$ -channel MOS), and negative upwards (in the normal operation of the  $p$ -channel MOS).

### 1.2.2 MOS Charges

Fig. 1.3 shows different charges associated with the MOS structure, together with the associated electric field and potential in the  $y$ -direction. In this section we try to calculate those charges as a function of the surface potential  $\psi_s$ .



**Figure 1.3** The MOS charges and associated electric field and potential.

### 1.2.2.1 The Semiconductor Charge

The semiconductor charge is a major parameter to get a good quantitative description to MOSFET operation, it may be found from the integration of the one dimensional Poisson's equation in the x direction. The semiconductor charge is divided into two components the inversion charge  $Q_i$  and the bulk charge  $Q_B$ , they may be found in all operating regimes of the device, from accumulation to strong inversion, as follows.

In the semiconductor the electrons and holes density can be expressed as [2]:

$$n(x) = (n_i^2 / N_A) e^{\beta(\psi(x) - \phi_c(x))} \quad (1.2.1)$$

$$p(x) = N_A e^{-\beta\psi(x)} \quad (1.2.2)$$

where  $n_i$  is the intrinsic carrier density per unit volume,  $N_A$  is the acceptor impurity density per unit volume,  $\beta$  is the inverse of the thermal voltage ( $=1/\phi_t$ ),  $\psi_s$  is the surface potential referenced to the bulk potential, and  $\phi_c$  is the quasi Fermi potential (the difference between  $E_{fn}$  at the surface of the semiconductor and  $E_{fp}$  in the bulk of the semiconductor).

Substituting equations (1.2.1) and (1.2.2) into the one dimensional Poisson's equation, we get

$$\frac{d^2\psi}{dx^2} = -\frac{q N_A}{\epsilon_s} [e^{-\beta\psi(x)} - 1 - e^{\beta(\psi(x)-\phi_c(x)-2\phi_f)}] \quad (1.2.3)$$

with  $\phi_f$  defined as the difference between  $E_i$  and  $E_f$  in the bulk of the semiconductor,

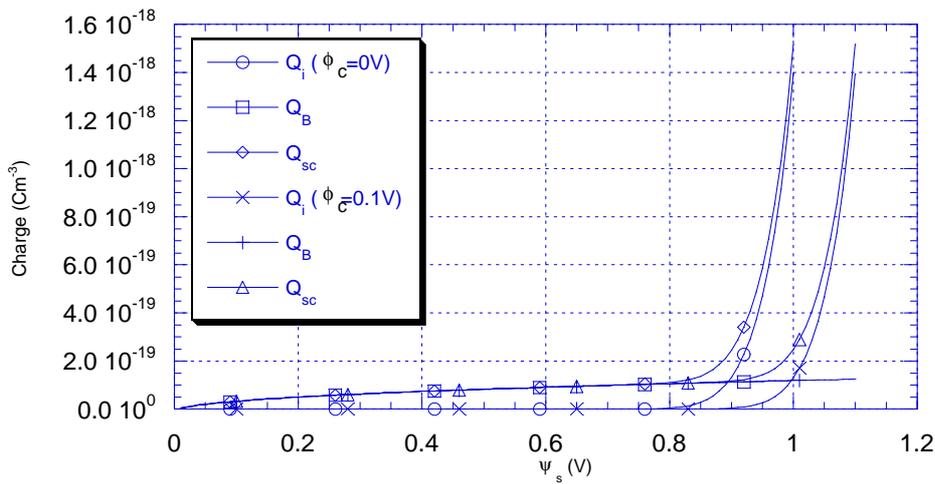
$$\phi_f = \phi_t \ln\left(\frac{N_A}{n_i}\right) \quad (1.2.4)$$

Equation (1.2.3) may be solved to yield :

$$Q_{sc}(\psi_s, \phi_c) = -\frac{\gamma C_{ox}}{\sqrt{\beta}} \sqrt{(\beta\psi_s + e^{-\beta\psi_s} - 1) + e^{-\beta(\phi_c + 2\phi_f)}(e^{\beta\psi_s} - 1)} \quad (1.2.5)$$

where

$$\gamma = \frac{\sqrt{2\epsilon_s q N_A}}{C_{ox}} \quad (1.2.6)$$



**Figure 1.4** Semiconductor charges versus  $\psi_s$  for two values of the quasi Fermi potential  $\phi_c$ .

and

$$Q_B(\psi_s) = -\frac{\gamma C_{ox}}{\sqrt{\beta}} \sqrt{\beta\psi_s + e^{-\beta\psi_s} - 1} \quad (1.2.7)$$

Finally, the *inversion* charge can then be computed using

$$Q_i(\psi_s, \phi_c) = Q_{sc}(\psi_s, \phi_c) - Q_B(\psi_s) \quad (1.2.8)$$

Fig. 1.4 shows the above semiconductor charges ( $Q_{sc}$ ,  $Q_B$  &  $Q_i$ ) versus the surface potential  $\psi_s$ , for two values of the quasi Fermi potential. The higher the quasi Fermi potential,  $\phi_c$  the lower is the *inversion* charge.

### 1.2.2.2 Oxide Charges

Generally speaking, the gate oxide of the MOSFET is not perfect. Oxide charges [2] include the oxide fixed charge, the oxide trapped charge, and the mobile ionic charge. They are represented in device analysis by an effective net oxide charge per unit area  $Q_{ox}$  at the Si-SiO<sub>2</sub> interface.  $Q_{ox}$  can be regarded as a fixed charge sheet located at the interface, and it is generally a positive charge, refer to Fig. 1.3.

### 1.2.2.3 Interface Trap Charge

An interface trap is an allowed electronic state, spatially located at a surface (or at an interface), due to the interruption of the periodic lattice structure [3]. It possesses the following properties:

- i. It can exchange charge with the silicon. Specifically, they can interact with the silicon conduction band by capturing or emitting electrons and with the valence band by capturing or emitting holes.
- ii. Its energy level is located in the forbidden gap or in either band (valence or conduction). However only the energy levels located within the forbidden gap or slightly above or below the band edges, will have the possibility to charge or discharge with bias.
- iii. It can be of either type: *donor* or *acceptor*
  - A monovalent *donor* trap possesses two states of charge: +1 and 0. Its charge is positive (in thermal equilibrium) when the trap level  $E_t$  is above the

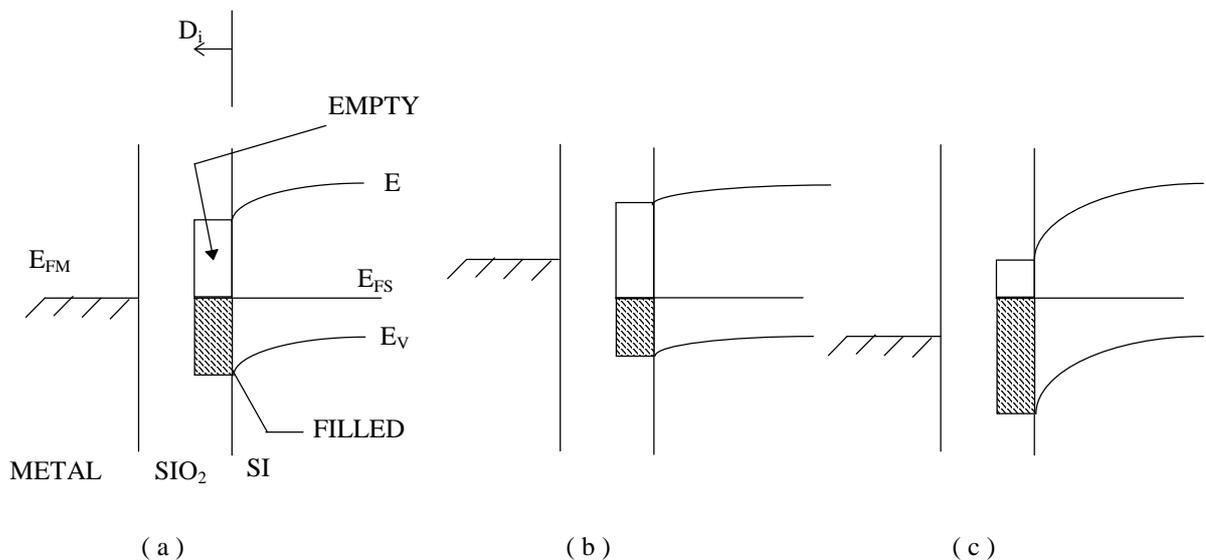
Fermi level  $E_f$ . Its charge is zero when  $E_t$  is below  $E_f$ .

- A monovalent *acceptor* trap possesses two states of charge: 0 and -1. Its charge is zero when  $E_t$  is above  $E_f$ . Its charge is negative when  $E_t$  is below  $E_f$ .

The interface trap level distribution in the bandgap is typically a rather smooth function of energy. Such a distribution is often called a *continuum* of interface trap levels. The interface trap charge is usually identified by the density of interface trap levels per unit area per electron volt  $D_{it}$ , that is the number of interface trap levels per unit area which is present between  $E_t$  and  $E_t+dE_t$  with energy in electron volts, i.e.  $D_{it}=(1/q)(dQ_{it}/dE)$ .

Changes in occupancy can be produced by changes in gate bias as illustrated in Fig. 1.5 for a *p*-type substrate.

For an acceptor trap, the interface trapped charge can be calculated using Fig. 1.5 as



**Figure 1.5** Band-bending diagram showing how interface traps change occupancy with gate bias. The sample is *p*-type. (a) No gate bias; (b) negative gate bias; (c) positive gate bias.[4]

$$Q_{ita} = -q \int_{E_v}^{E_c} D_{ita}(E_t) f(E_t) dE_t \quad (1.2.9)$$

where  $f(E_t)$  is the Fermi-Dirac distribution function given by

$$f(E_t) = \frac{1}{1 + e^{\beta(E_t - E_{fn})}} \quad (1.2.10)$$

Similarly the donor interface trapped charge can be calculated as follows

$$Q_{iid} = q \int_{E_v}^{E_c} D_{iid}(E_t) (1 - f(E_t)) dE_t \quad (1.2.11)$$

The net interface trapped charge per unit area  $Q_{it}$  is given by

$$Q_{it} = Q_{iid} + Q_{ita} \quad (1.2.12)$$

using eqs. (1.2.9), and (1.2.11)

$$Q_{it} = q \left[ \int_{E_v}^{E_c} D_{iid}(E_t) dE_t - \int_{E_v}^{E_c} D_{it}(E_t) f(E_t) dE_t \right] \quad (1.2.13)$$

where we have defined a total interface trapped density  $D_{it} = D_{iid} + D_{ita}$ .

Experimentally, it has been shown [4] that interface traps in the upper half of the silicon bandgap are donor like in device grade oxide. There are no reliable measurements to determine whether interface traps in the lower half of the silicon bandgap are donor or acceptor like. However there exist different reliable ways of measuring the total interface trap density  $D_{it}$  such as charge pumping technique [5,6]. As will be shown later, it is this total density that affects the device characteristics.

The following assumptions have been introduced to simplify the analytical determination of the interface trap charge  $Q_{it}$  [7]:

1. The interface trap density  $D_{it}$  is taken to be constant in the whole energy range of interest, referring to Fig. 1.5, that is the average density in the region of interest.

2. In nonequilibrium i.e. an applied drain-source bias, the occupancy of the interface traps is determined by the position of the quasi-Fermi level of the minority carriers.

Using the above two assumptions the trapped charge  $Q_{it}$  can be calculated using eq. (1.2.13) in the form

$$Q_{it}(\psi_s, \phi_c) = q \left\{ D_{itd} E_g - \frac{D_{it}}{\beta} \left[ \beta \left( \frac{E_g}{2} - \phi_f + \psi_s - \phi_c \right) + \ln \left( 1 + e^{-\beta \left( \frac{E_g}{2} - \phi_f + \psi_s - \phi_c \right)} \right) \right] \right\} \quad (1.2.14)$$

Practically,  $Q_{it}$  is expressed in terms of its constant term at flat band plus a variable term

$$Q_{it}(\psi_s, \phi_c) = Q_{it}(0,0) + Q_{it}'(\psi_s, \phi_c) \quad (1.2.15)$$

where

$$Q_{it}(0,0) \approx q \left[ D_{itd} E_g - D_{it} \left( \frac{E_g}{2} - \phi_f \right) \right] \quad (1.2.16)$$

and

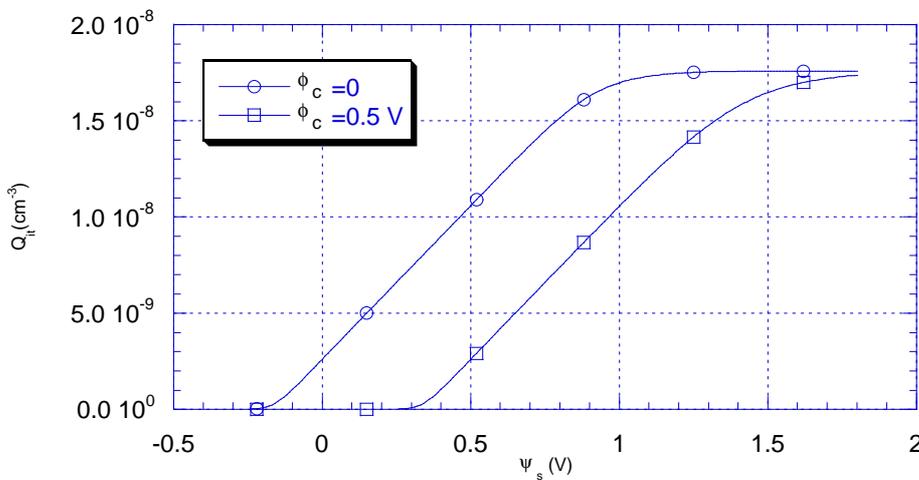
$$Q_{it}'(\psi_s, \phi_c) \approx -q \frac{D_{it}}{\beta} \left[ \beta (\psi_s - \phi_c) + \ln \left( 1 + e^{-\beta \left( \frac{E_g}{2} - \phi_f + \psi_s - \phi_c \right)} \right) \right] \quad (1.2.17)$$

As shown from the above equations, the nature of the interface traps (*acceptor-* or *donor-*like traps) affects only the constant part of the interface trapped charge  $Q_{it}(0,0)$ . This constant part can't be practically distinguished from the oxide fixed charge at flat band, and is determined through flat-band voltage measurements (sec. 1.2.3). On the other hand, the variable part of the interface trapped charge  $Q_{it}'(\psi_s, \phi_c)$ , depends only on the total interface trapped charge density  $D_{it}$ . The interface trapped charge is comparable to the total semiconductor charge in subthreshold, and affects the device characteristics in that region, while it is negligible compared to this charge in strong inversion.

Note that for a heavily doped bulk in strong inversion where  $\psi_s > 2\phi_f + 6\phi_t$  [1], the quasi Fermi level  $E_{fn}$  approaches the conduction band, Fig. 1.5 (c). The upper limit for  $Q_{it}$  is then  $q(D_{itd} - D_{it})E_g$ .

Fig. 1.6 shows the above calculated interface trapped charge, which is assumed to be composed only of acceptor-like traps (i.e.  $D_{it} = D_{ita}$  and  $D_{itd} = 0$ ),

versus the surface potential for two different values of the quasi Fermi potential  $\phi_c$ , in an  $n$ -channel MOS transistor. As  $\phi_c$  increases, more levels *emit* their electrons, and  $Q_{it}$  decreases. When  $\phi_c$  approaches the valence band edge  $E_v$ ,  $Q_{it}$  tends to zero. On the other hand as  $\psi_s$  increases, more levels *trap* electrons, and  $Q_{it}$  increases. The interface trapped charge is shown to vary only while  $\psi_s$  changes within the range of  $E_g$ .



**Figure 1.6** Interface trap charge versus the surface potential.

### 1.2.3 The Flat Band Voltage

The flat band voltage, may be defined as the gate-bulk voltage necessary to obtain a zero surface potential  $\psi_s$  [3], it expressed as

$$V_{FB} = \phi_{ms} - \frac{1}{C_{ox}} [Q_{ox} + Q_{it}(0,0)] \quad (1.2.18)$$

In the above equation,  $\phi_{ms}$  is the gate-semiconductor work function difference. This value depends on the gate material (metal,  $N$ -Poly, or  $P$ -Poly).

This voltage is usually measured practically, and it is difficult to distinguish its components from such measurements. Any variation in the flat band voltage appears directly as an equal variation in the threshold voltage value.

### 1.3 The MOSFET Mobility

The mobility of electrons in the inversion layer (called *surface mobility*) is smaller than the bulk mobility, due to *scattering mechanisms*. The effective mobility used in the long channel model must include the effect of the normal field due to the gate. The effect of the longitudinal field on the mobility is important only in short channel devices.

For a given temperature, the value of the surface mobility is found to be only a function of the average normal electric field  $F_{xav}$  in the inversion layer, defined by

$$F_{xav} = \frac{F_{xs} + F_{xb}}{2} \quad (1.3.1)$$

where  $F_{xs}$  is the value of the normal field at the surface and  $F_{xb}$  is its value just below the inversion layer. The experimental data appear to conform to the following relation:

$$\mu = \frac{\mu_o}{1 + \alpha F_{xav}} \quad (1.3.2)$$

where  $\mu_o$  is the low field mobility, and  $\alpha$  is a fitting parameter.

The effective normal electric field at the surface is related to the total charge per unit area below the surface by gauss law:

$$F_{xs} = -\frac{Q_{sc}}{\epsilon_s} \quad (1.3.3)$$

where  $Q_{sc}$  is given by (1.2.5)

Similarly the field just below the inversion layer can be determined by assuming a very thin inversion layer, so that the total charge per unit area below the inversion layer is practically all of  $Q_B$ , given by eq. (1.2.7):

$$F_{xb} = -\frac{Q_B}{\epsilon_s} \quad (1.3.4)$$

Using the above equations, we obtain

$$\mu = \frac{\mu_o}{1 - \frac{\alpha}{2\epsilon_s}(Q_{sc} + Q_B)} \quad (1.3.5)$$

The effective mobility [8] may be obtained by substituting with eq. (1.3.5) in the drain current equation and integrate from 0 to L on the assumption that  $\psi_s$  is linear with y (i.e.  $d\psi_s/dy \cong (\psi_{sL} - \psi_{s0})/L$ ), to simplify the integration, thus we obtain

$$\mu_{eff} = \frac{\mu_o}{1 + \theta f_\mu} \quad (1.3.6)$$

where

$$f_\mu = (V_G - V_{FBD}) - 0.5(\psi_{sL} + \psi_{s0}) + \frac{2}{3}\gamma \frac{((\psi_{sL} - \frac{1}{\beta})^{3/2} - (\psi_{s0} - \frac{1}{\beta})^{3/2})}{(\psi_{sL} - \psi_{s0})} \quad (1.3.7)$$

and

$$\theta = \frac{C_{ox}\alpha}{2\epsilon_s} \quad (1.3.8)$$

## 1.4 MOSFET Modeling

The reason for MOSFET modeling as any other device modeling is two fold. First, the device designer needs to understand how a device operates and hence is primarily interested in the internal device mechanisms. Second, the circuit designer looks for a quantitative description of the terminal behavior only, which should be as accurate as necessary and as simple as possible. In his part of the overall design process, the circuit designer wants to predict circuit performance by numerically simulating a proposed circuit topology. Generally, he relies on an established process for device fabrication and hence is able to improve model accuracy by introducing fitting parameters into the analytical formulas of his model. Extending this approach may lead to the point where the measured parameters constitute a table and the model acts only as an interpolation routine between neighboring table values. During this process, the

connection to device physics is gradually lost gaining computational efficiency which is the uppermost concern in simulating large circuits. However, this introduces a serious drawback for such models, that they are likely to fail in predicting ahead of time what will happen if some fabrication process parameters are changed. Developing a model is an art involving constant tradeoffs between accuracy and computational time efficiency.

On the other hand, the device designer is also somewhat interested in circuit performance at least of small-scale building blocks, since the devices he is designing are to operate in a circuit environment. He seeks to reserve the connection to device physics in order to be guided by circuit performance criteria in his design process. Ideally, the desired device performance should arise from those criteria and the device design process should result in specifications for a wafer process to be developed. In practice, however, process and device development are carried out simultaneously and device modeling should aid the iterative process of device specification and wafer processing by saving part of the otherwise necessary cycles of the iteration loop.

### ***1.4.1 Numerical MOSFET Modeling***

A device simulator calculates the electrical characteristics of devices when structure shape, and impurity profile are given.

The behavior of electronic devices is governed by a set of basic semiconductor equations, these equations are summarized as follows [9]:

#### ***1- Poisson's equation***

$$\nabla^2 \psi = -\frac{q}{\epsilon}(p - n + N_D^+ - N_A^-) \quad (1.4.1)$$

**2- The continuity equations**

$$\begin{aligned}\frac{\partial p}{\partial t} &= -\frac{1}{q} \nabla \cdot J_p - R + G \\ \frac{\partial n}{\partial t} &= \frac{1}{q} \nabla \cdot J_n - R + G\end{aligned}\tag{1.4.2}$$

**3- The current equations**

$$\begin{aligned}J_p &= -q \mu_p p \nabla \psi - q D_p \nabla p - \mu_p k p \nabla T_p \\ J_n &= -q \mu_n n \nabla \psi + q D_n \nabla n + \mu_n k n \nabla T_n\end{aligned}\tag{1.4.3}$$

**4- The energy balance equations [10]**

$$\begin{aligned}\nabla \cdot S_p - F \cdot J_p + U \omega_p + p \frac{\omega_p - \omega_p^*}{\tau_p} &= 0 \\ \nabla \cdot S_n - F \cdot J_n + U \omega_n + n \frac{\omega_n - \omega_n^*}{\tau_n} &= 0\end{aligned}\tag{1.4.4}$$

where  $R$  represents the recombination rate,  $G$  the generation rate,  $S_p$  and  $S_n$  represent the energy flux of holes and electrons respectively,  $F$  is the electric field,  $\omega_p$  and  $\omega_n$  are the carrier energies, and  $\tau_p$  and  $\tau_n$  are the energy relaxation times.

The semiconductor equations contain quantities, such as the recombination ( $R$ )/generation ( $G$ ) rates and the mobilities ( $\mu_n$  and  $\mu_p$ ), which themselves are the result of complicated physical mechanisms. Therefore, these quantities are not constant but depend on the local values of carrier densities and electric field.

The complete set of nonlinear differential device equations together with the given boundary conditions are then solved numerically using different methods yielding the device's physical characteristics.

The device simulator aims to derive from the input set of physical and technological parameters, the electrostatic potential  $\psi$  and quasi-Fermi levels for electrons  $E_{fn}$  and holes  $E_{fp}$  in space and time. These three quantities yield, in turn, the vector fields of the electric field strength and electric current density. Finally, integration of the first vector along a contour between

respective contacts and the second over respective contact areas results in the terminal characteristics of a device.

### ***1.4.2 Analytical MOSFET Modeling***

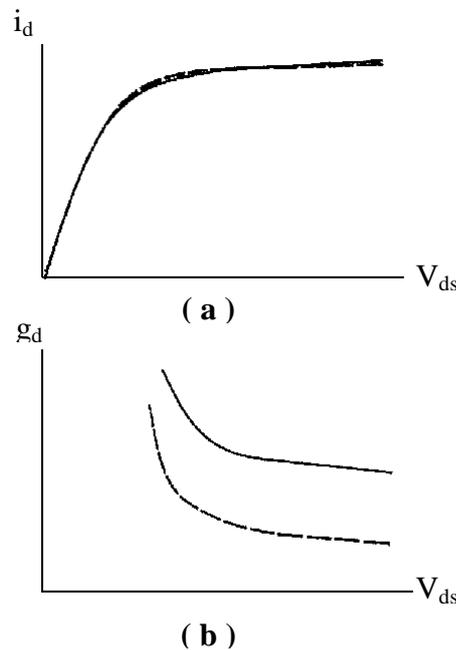
In order to be used in a circuit simulator where thousands of MOSFETs are present, numerical modeling turns to be ineffective, as it turns to be very time consuming. Analytical models must then be used. An analytical model is simply a system of algebraic equations describing the terminal  $I$ - $V$  performance of the device.

All analytical MOSFET models use the *Gradual Channel Approximation* (GCA) [11] (which will be discussed in the next chapter), which decomposes and simplifies the two-dimensional problem into two analytical one-dimensional problems. One deals with the solution of the oxide field due to the voltage applied between the gate and the Si bulk. The other deals with the current in the channel due to voltage applied between the drain and source terminals. More Details about analytical modeling are given in chapter 2.

The circuit simulator aims only to calculate the voltage and current at every circuit node by a numerical procedure that depends on the terminal  $I$ - $V$  characteristics of each circuit element. This requires that every circuit element (including the MOSFET) must provide an analytical (closed-form) relation between the terminal voltages and output currents.

## **1.5 MOSFET Modeling for Analog Circuit CAD**

The modeling of MOS transistors for computer-aided design has been driven by the needs of digital circuit designers for many years, but unfortunately these models give poor results when used in analog simulation [8].



**Figure 1.7** (a)  $I_D$ - $V_{DS}$  characteristics as resulting from measurement (solid line) and simulation (dashed line). (b) The output conductance resulting from taking the slopes in (a).[8]

As an example [8], consider Fig. 1.7(a). It would seem that the model (dashed line) is an adequate representation of the experiment (solid line). Yet, consider the drain-source small-signal conductance  $g_d$ , given by the slope of the  $I_D$ - $V_{DS}$  characteristics: for the case of Fig. 1.7(a) that slope is given in Fig. 1.7(b), and a very large discrepancy between the model and experiment becomes obvious. To argue about the seriousness of this problem, one needs only to recall that the amplifier voltage gain can be inversely proportional to sum of  $g_d$  quantities.

Recently, many laboratories have put a considerable effort into the development of new analog MOS models to comply with the new technological trend towards mixed analog-digital chips, not only for direct interfacing to the physical world, but also for aiding digital systems to increase their performance. It is predicted that in a few years, most chips will contain at least some analog circuits.

### 1.5.1 The Special Nature of Analog Modeling Needs

From the last discussed example, it becomes obvious that, if somebody claims a model to give a good drain current fit to measurements, all we can conclude is that, maybe, the model can predict satisfactorily the bias point of an analog circuit. Since the design of such a circuit involves much more than just bias point evaluation, many more requirements need to be met by the model before we could call it adequate for analog work.

A MOSFET model for analog circuit design should ideally satisfy the following criteria [12]:

1. The model should, of course, meet common requirements for digital work, such as reasonable  $I$ - $V$  characteristic accuracy, shift register speed prediction, charge conservation, etc.
2. It should give accurate values for all small-signal quantities as  $g_m$ ,  $g_{mb}$ ,  $g_d$ , and capacitances. In particular, all of these parameters should be *continuous* with respect to *any* terminal voltage.
3. It should meet the above requirements over large bias ranges, including  $V_{SB} \neq 0$ , and encompassing the weak, moderate, and strong inversion regions.
4. It should do all of the above over the temperature range of interest.
5. It should do all of the above for any combination of channel width and length values, from the minimum specified upwards. The user should only have to specify the geometrical dimensions for each device, and *one* set of model parameters valid for *all* devices of the same type and independent of dimensions.
6. The model should provide a flag at any attempt to use it outside its limits of validity. For example, if the model is quasi-static and one attempts to use it, say, around the unity gain frequency of the device, a warning should be given to the user that the result may be inaccurate.
7. The model should have as few parameters as possible (but just enough), and those parameters should be linked as strongly as possible to ones

related to the device structure and fabrication processing (e.g. oxide thickness, substrate doping, junction depth). This would allow meaningful worst-case simulations and predictions. Empirical parameters without physical meaning should be avoided as much as possible. This requirement strongly points to the direction of a *physically-based model*.

8. The model should be linked to an efficient parameter extraction method; one could even go so far as to say that parameter extraction should be constantly kept in mind during model development from the beginning. The number of required test devices and tests for parameter extraction should be as small as possible.
9. The model should ideally provide links to device simulators (refer to table 1.1).
10. For application in a circuit simulator, the model also needs to be relatively simple in its formulation to achieve low computer CPU time per model call.

## 1.6 CAD requirements

In order to develop a *working* model, one should understand the working nature of the circuit simulator which incorporates the model.

The circuit simulator starts an analysis by writing a set of *nodal* equations which describe the elements in the circuit. This set of nodal equations is often a system of transcendental equations, and a nonlinear solution technique known as Newton-Raphson algorithm is applied to the system matrix. The Newton-Raphson algorithm, a method of successive approximations, is an iterative approach to solving a set of nonlinear equations. The circuit simulator starts with an initial guess for every node voltage in the circuit and begins iterating. With each successive iteration, a new set of node voltages is predicted. The solution routine monitors the node voltage of the present iteration and the previous iteration value.

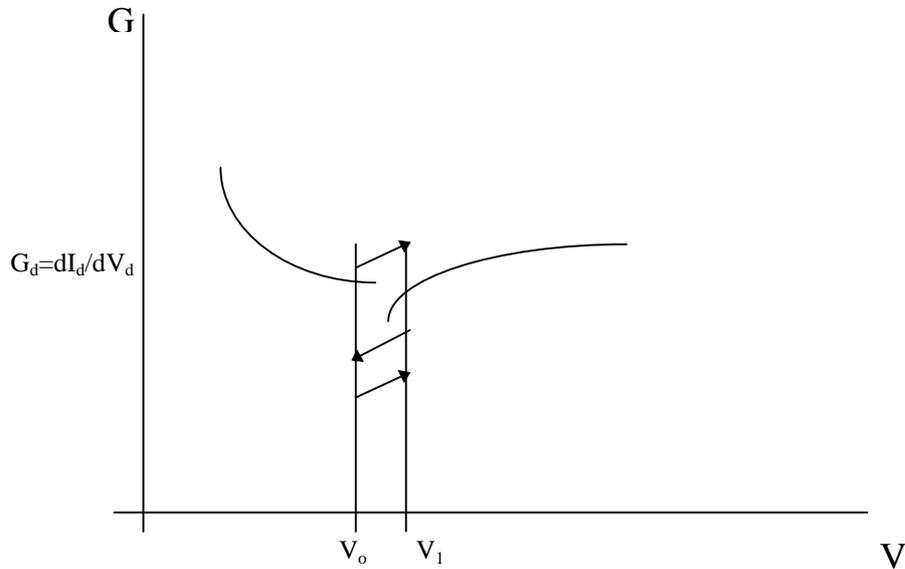
Ideally, at the exact solution, the node voltage between successive iterations should be identical, or the difference between iterative voltage

values should be zero. But because of the way digital computers represent numbers, saying when two numbers are exactly equal can be difficult (because of round-off errors). Because of this difficulty, the circuit simulator monitors the difference between iterative node voltage values and compares the difference with a predefined error tolerance. When the difference between iterative voltage values is less than the error tolerance for every node of the circuit, the circuit simulator terminates the iterative process for that solution point.

### ***1.6.1 Nonconvergence***

In addition to the error tolerance limits, the simulator limits the total number of iterations each analysis type is allowed to process. If the iterative node voltages have not satisfied the error tolerance requirements before the simulator exceeds the iteration limit, the simulator *aborts* the simulation and proclaims the infamous *nonconvergence* error message.

One of the main problems that causes nonconvergence in the calculation of the bias point is *model discontinuities*. As an example we consider Level 3 MOSFET SPICE model. Classical MOSFET theories split the transistor curves into the linear region and the saturated region of operation. The device equations in SPICE follow the same regions of operation. But, unlike the real device, SPICE uses separate equations for each region of operation. Because of the mathematical difficulty in writing an equation which describes the entire family of curves, two different sets of equations were written, one for the linear region and one for the saturation region, and joined together. Unfortunately, because of the way the equations were joined, there is a discontinuity in the conductance characteristics (the slope of the I-V curve) of the device.



**Figure 1.8** Iterations around a model discontinuity. [13]

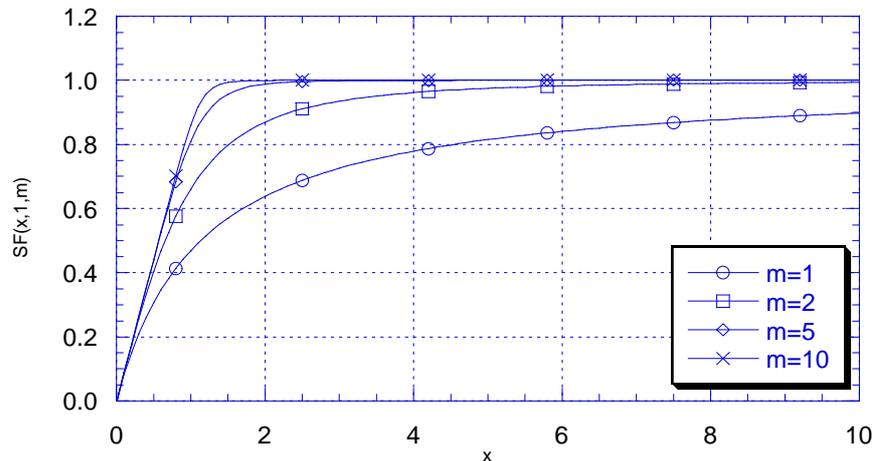
A discontinuity in conductance may lead to problems for the Newton-Raphson algorithm. Fig. 1.8 illustrates the conductance vs. voltage characteristics around one of the model discontinuities. On the first Newton iteration close to the discontinuity, the conductance value leads to a new iterative voltage on the other side of the discontinuity. The next Newton iteration falls on a conductance value which predicts a solution back on the original side of the discontinuity. The third Newton iteration again predicts a solution on the far side of the discontinuity. When SPICE steps close to or on top of a model discontinuity, the Newton-Raphson iterations may begin to oscillate around the discontinuity. These oscillations use up iterations without progressing towards a solution. A solution to this problem is by using mathematical smoothing functions between different operating regions.

### 1.6.2 The smoothing function

While moving from one region of operation of the MOSFET to the other some variables (voltage, charge, current, ...) may have an upper limit to which they tend. The model thus may have an output characteristic composing of segments of different slopes i.e. discontinuity in the output conductance, that may lead to *nonconvergence* problems in the circuit simulator (refer to Section 1.4.1). Besides, this discontinuity may lead to non-practical solutions if the bias is close to it.

In order to prevent such discontinuities, a smoothing function will be used, this function has the form

$$SF(x, x_o, m) = \frac{x}{\left(1 + \left(\frac{x}{x_o}\right)^m\right)^{1/m}} \quad (1.6.1)$$



**Figure 1.9** The smoothing function

and is plotted in Fig. 1.9 for different values of  $m$ , and for  $x_o = 1$ . As shown in Figure, for small values of  $x \ll x_o$ , the function  $SF$  tends to  $x$ , as  $x$  increases,  $SF$  tends to  $x_o$ . The parameter  $m$  determines the width of the transition (knee) region.

## 1.7 Overview of various simulators.

Simulator level	Input data	Objective	Example
Process simulator	Heating process Chemical procedure Ion implant condition Chemical environment	Impurity profile estimation Ion implantation optimization Cross-sectional shape	SUPREM
Device simulator	Electrode structure Oxide layer shape Materials Impurity distribution	Threshold and punch-through d.c. characteristics of MOSFETs Wire capacitance and resistance Latchup and soft errors analysis	MINI-MOS [31] PRISM [10]
Circuit simulator	MOSFET parameters Capacitance parameters Resistance parameters Circuit connectivity	Circuit voltage and current Component parameter optimization Mask pattern verification Worst-case prediction	SPICE ELDO
Logic simulator	Gate logic function Rise and fall time Gate connectivity Gate delay scattering	System function check Logic net optimization Logic connectivity check	HILO QuickSim
Behavior simulator	Block functions Block connectivity	System behavior prediction Block level optimization Block connectivity check	SIMU-LINK [MATLAB]

**Table 1.1** Overview of various simulators

# CHAPTER 2

## Model Description

### 2.1 Introduction

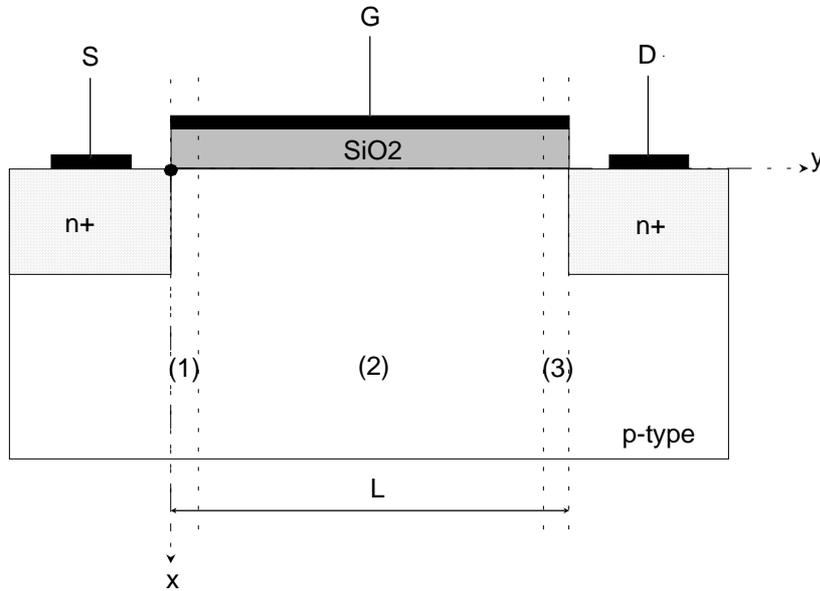
The modeling procedure is introduced in this chapter, taking into consideration the requirements for a *good* MOSFET analog model, discussed in the previous chapter.

We note here two main aspects of our modeling approach;

- a. The model must describe *accurately* all the operating regions in order to be integrated in a circuit simulator.
- b. The current, conductance, and transconductance must be continuous in all regions of operation.

Our main goal in this chapter is to determine the drain current for any combination of terminal voltages. The chapter is divided into two main parts. Throughout the first part, it is assumed that the channel is sufficiently *long* and *wide*, so that edge effects are confined to a negligible part of it. While in the second part we incorporate the short and narrow channel effects to the model. We also assume that the substrate is *uniformly* doped. The doping concentration will be assumed to be *p*-type and the modification to non uniform doping will be discussed later in this chapter.

## 2.2 Gradual Channel approximation (GCA)



**Figure 2.1** *The MOSFET structure.*

Analytical or semi-analytical modeling of MOSFET characteristics is usually based on the so-called *Gradual Channel Approximation* (GCA) [11]. In this approximation, we assume that the gradient of the electric field in the  $y$  direction,  $\partial F/\partial y$  is much smaller than the gradient of the electric field in the  $x$  direction,  $\partial F/\partial x$ . Which enable us to determine the inversion and depletion charge densities under the gate in terms of a one-dimensional electrostatic problem for the direction perpendicular to the channel. By applying of the two dimensional Poisson's equation for the semiconductor, refer to Fig. 2.1 region (2),

$$\frac{\partial F_x}{\partial x} + \frac{\partial F_y}{\partial y} = \frac{\rho}{\epsilon_s} \quad (2.2.1)$$

if we assume that the GCA is valid equation 2.2.1 may be approximated to the following one dimensional differential equation

$$\frac{\partial F_x}{\partial x} \approx \frac{\rho}{\epsilon_s} \quad (2.2.2)$$

As we approach the source and drain junctions, the GCA becomes invalid (Fig. 2.1 regions (1) and (3)) because of the increasing longitudinal field due to the pn junctions which make  $\partial F/\partial y$  comparable or even larger than  $\partial F/\partial x$ . However, for the long channel MOSFET's these transition regions can be neglected with respect to the total length of the device. In order to account for the effect of these regions, it is necessary to use two-dimensional analysis requiring a numerical solution of 2.2.1.

### Validity of the GCA

The validity of GCA can be checked by making rough estimates of the variation in the longitudinal and vertical field components. We will establish expressions that allow the GCA to be checked under strong inversion<sup>1</sup> [11].

$$\frac{\partial F_x/\partial x}{\partial F_y/\partial y} = \left(\frac{\epsilon_{ox} L}{\epsilon_{si}}\right)^2 \frac{q(V_{GS} - V_T)^2}{kT \cdot t_{ox} \cdot V_{DS}} \gg 1 \quad (2.2.3)$$

For a MOSFET at 300K with  $L = 1.0\mu\text{m}$ ,  $t_{ox} = 30 \text{ nm}$ ,  $V_{GS} - V_T = 0.5$ , and  $V_{DS} = 0.5 \text{ V}$ , the left hand side of inequality 2.2.3 is  $\sim 2300$ , indicating that the GCA is a very good approximation for such a MOSFET. This also implies that the GCA can be valid even in submicron MOSFETs, provided that  $V_{GS} - V_T$  is not too small.

## 2.3 The long channel current model

The derivation of the dc drain current relationship recognizes that, in general, the current in the channel of a MOSFET can be caused by both drift and diffusion current. In an NMOSFET we may assume the following reasonable approximation :

- i- The drain current is mainly carried by electrons .
- ii- The current flows almost in the y direction.
- iii- No sources or sinks in the channel.

<sup>1</sup> Note that in weak inversion the surface potential along the channel in long channel MOSFETs is almost constant. Thus  $\partial F_y/\partial y$  is very small, implying that  $\partial F_y/\partial y \ll \partial F_x/\partial x$ . Thus in long channel MOSFET the GCA is valid both in strong and weak inversion regions [11].

Which enable us to reach to the following general relationship of drain current.

### 1- General Drift-Diffusion current equation in MOSFET:

This is the drift-diffusion drain current of the form [8]

$$I_D(y) = \mu_n W (-Q_i) \frac{d\phi_c}{dy} = \mu_n W (-Q_i(y)) \frac{d\psi_s(y)}{dy} + \mu_n W \phi_t \frac{dQ_i(y)}{dy} \quad (2.3.1)$$

where  $\mu_n$  is the electron surface mobility in the channel,  $W$  is the channel width,  $Q_i$  is the inversion charge density per unit area,  $\phi_c$  is the quasi Fermi potential (the difference between  $E_{fn}$  at the surface of the semiconductor and  $E_{fp}$  in the bulk of the semiconductor),  $\psi_s$  is the surface potential referenced to the bulk potential, and  $\phi_t$  is the thermal voltage ( $=kT/q$ ).

The first term is the *drift current component*, while the second term is the *diffusion current component*. In both components,  $\mu_n$  is the electrons' surface mobility being less than the mobility in the bulk due to surface scattering.

### 2- Voltage-Charge equation from the Transverse electric field:

In order to eliminate the electron charge density  $Q_i$  term in the current-charge equation, a second relationship is required that relates the electron charge density to the applied potentials.

Using the relationship between voltage and charge appearing across the MOS capacitor we have [8]

$$C_{ox}(V_G - \phi_{ms} - \psi_s) = -(Q_i + Q_B + Q_{ox} + Q_{it}) \quad (2.3.2)$$

where  $V_G$  is the gate voltage referenced to the bulk potential,  $\phi_{ms}$  is the metal-semiconductor work function difference,  $Q_B$  is the depletion (bulk impurity) charge density per unit area,  $Q_{ox}$  is the sum of the effective net oxide charge per unit area at the Si-SiO<sub>2</sub> interface, and  $Q_{it}$  is the interface trapped charge density per unit area.

Different approximations have been introduced in order to express the different MOS charges ( $Q_B$ ,  $Q_{ox}$ ,  $Q_{it}$ ) in terms of the applied voltages, then using eq. (2.3.2) to compute the inversion charge density  $Q_i$ . The resulting charge is then used in eq. (2.3.1) to determine the drain current; Four main approaches then follow, after them we shall discuss the proposed approach recently developed in ICL<sup>1</sup> and modified by this work.

### ***2.3.1 The classical long-channel Pao and Sah model***

The Pao-Sah model [11,14], published in 1966, was the first advanced long channel MOSFET model to be developed. While it retained the GCA, it didn't invoke the depletion approximation and permitted carrier transport in the channel by both drift and diffusion current. The formulation of the drain current equation is therefore general, but as a result requires numerical integration in two dimensions, which limits its application in CAD tools.

#### *Approximations:*

- i. Gradual Channel Approximation is used.
- ii. Constant mobility is assumed.
- iii. Uniform substrate doping is considered.

#### *Advantages:*

- i. It is physically based.
- ii. It gives a continuous representation of the device characteristics from weak to strong inversion even to the saturation mode of operation.

#### *Disadvantages:*

- i. It requires excessive computational requirements since it requires numerical integration in two dimension, rendering it unsuitable to be used for circuit CAD.

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### 2.3.2 The charge-sheet based models

The limited practical utility of the Pao-Sah model motivated a search for an approximate advanced analytical model, that is still accurate over a wide range of operating conditions. The charge sheet model, introduced separately by Bacarani and Brews in 1978, has become the most widely adopted long channel MOSFET model that is accurate over the entire range of inversion.

In this model the inversion layer is supposed to be a charge sheet of infinitesimal thickness [11,15,16] (*charge sheet approximation*). The inversion charge density  $Q_i$  can then be calculated in terms of the surface potential  $\psi_s$ .

The drain current (2.3.1) is then expressed in terms of the surface potential at the source and drain boundaries of the channel.

#### *Approximations:*

- i. Gradual Channel Approximation is used.
- ii. The mobility is assumed to be proportional to the electric field and is constant with position along the channel.
- iii. Uniform substrate doping is considered.

#### *Advantages:*

- i. It is physically based.
- ii. It gives a continuous representation of the device characteristics from weak to strong inversion even to the saturation mode of operation.
- iii. The charge sheet approximation introduces negligibly small error, and it is more computationally efficient than the classical model.

#### *Disadvantages:*

- i. The boundary surface potentials cannot be expressed explicitly in terms of the bias voltages applied to the device, but must be found by a numerical process.
- ii. The model is not valid in depletion or accumulation.

Different approaches have been introduced to circumvent this disadvantage. In [17-19] it is shown that accurate numerical solutions for these surface potentials can be obtained with negligible computation time penalty. In [20] the surface potentials are computed using cubic splines functions. In [21] and [22], the implicit equation including the surface potential is replaced by an approximate function. Although all of these approaches have given good results, they have neglected the effect of the *interface trap* charge which is important in determining the subthreshold characteristics of the device, namely the subthreshold swing (the gate voltage swing needed to reduce the current by one decade).

### 2.3.3 Bulk Charge Model

The Bulk Charge model [11], also known as variable depletion charge model, was developed in 1964, describes the MOSFET drain current only in strong inversion but of course has less computational requirements.

#### *Approximations :*

- i. Drift current component only is considered
- ii. Constant surface potential is assumed
- iii.  $I_d$  considered zero below threshold

#### *Advantages :*

- i. Less computational time than the charge sheet model

#### *Disadvantages :*

- i. The subthreshold region not defined

### 2.3.4 Square law model

This model [1,11] has great popularity, when a first estimate to device operation, or simulating a circuit with a large number of devices is required. This model is obtained from the bulk charge model, on the assumption that  $V_{DS} \ll 2\phi_f + V_{BS}$  [11].

*Approximations :*

- i. Drift current component only is considered
- ii. Constant surface potential is assumed
- iii.  $I_d$  considered zero below threshold
- iv.  $V_{DS} \ll 2\phi_f + V_{BS}$

*Advantages :*

- i. Very small computational time than any other model
- ii. Suitable for hand calculations

*Disadvantages :*

- i. The subthreshold region is not defined
- ii. Overestimates the drain current in saturation region

### 2.3.5 Approximate models

There exists a large number of introduced approximate models [8,23-29]. All of these models originate from Brews' charge sheet model, where approximations to the surface potentials in various operating regions of the device have been used. This leads to different current equations each valid only in a specific region. The resulting equations are then empirically joined using different mathematical conditions of continuity.

*Advantages:*

- i. They have good accuracy in the desired region of operation.
- ii. They are very efficient from the point of view of computational time.

*Disadvantages:*

- i. The error increases in the transition regions between different modes of operations.
- ii. They include many non-physical fitting parameters.

### 2.3.6 Modified charge sheet model

The last discussed MOSFET models, have a common illness, no interface charges are included which play a great role in subthreshold region. So a modified model to the charge sheet model, which include the effect of interface charges is carried out in ICL, and will be presented now [30].

The derivation begins by rewriting equation (2.3.1) in the following form :

$$I_D = I_{D1} + I_{D2} \quad (2.3.6.1)$$

where  $I_{D1}$  is due to the presence of drift:

$$I_{D1} = \frac{W}{L} \int_{\psi_{s0}}^{\psi_{sL}} \mu_n (-Q_i) d\psi_s \quad (2.3.6.2)$$

and  $I_{D2}$  is due to the presence of diffusion:

$$I_{D2} = \frac{W}{L} \phi_t \int_{Q_{i0}}^{Q_{iL}} \mu_n dQ_i \quad (2.3.6.3)$$

after mathematical manipulation and following the same approximations as charge sheet model we reach the following drain current equations:

$$I_{D1} = \frac{W}{L} \mu_{eff} C_{ox} [(V_G - V_{FBD})(\psi_{sL} - \psi_{s0}) - \frac{1}{2}(\psi_{sL}^2 - \psi_{s0}^2) - \frac{2}{3} \frac{\gamma}{\beta^{3/2}} ((\beta\psi_{sL} - 1)^{3/2} - (\beta\psi_{s0} - 1)^{3/2})] \quad (2.3.6.4)$$

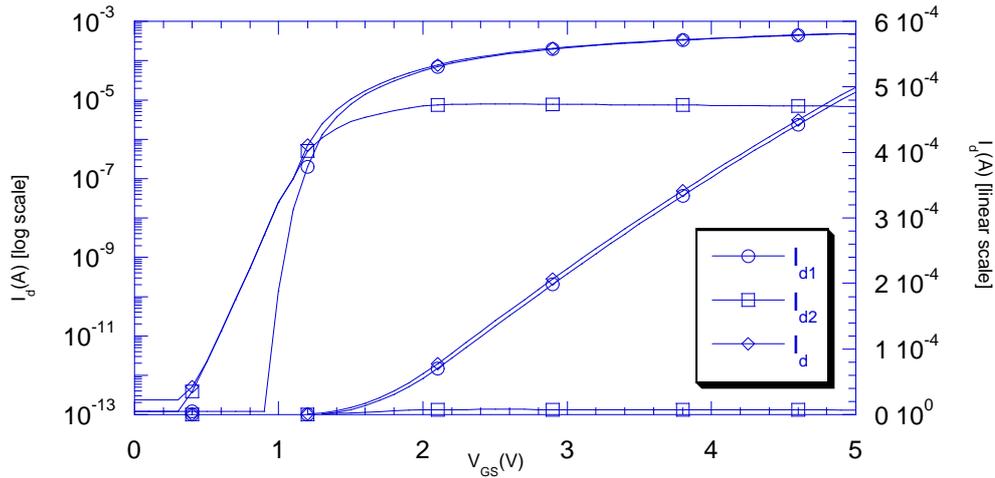
$$I_{D2} = \frac{W}{L} \frac{\mu_{eff} C_{ox}}{\beta} [(\psi_{sL} - \psi_{s0}) + \frac{\gamma}{\sqrt{\beta}} (\sqrt{\beta\psi_{sL} - 1} - \sqrt{\beta\psi_{s0} - 1}) - \frac{1}{C_{ox}} (Q_{it}'(\psi_{sL}, V_D) - Q_{it}'(\psi_{s0}, V_S))] \quad (2.3.6.5)$$

where  $\psi_{s0}$  is the surface potential at the source end of the channel,  $\psi_{sL}$  is the surface potential at the drain end of the channel, both are referred to the bulk. And their values are computed from the following two implicit equations.

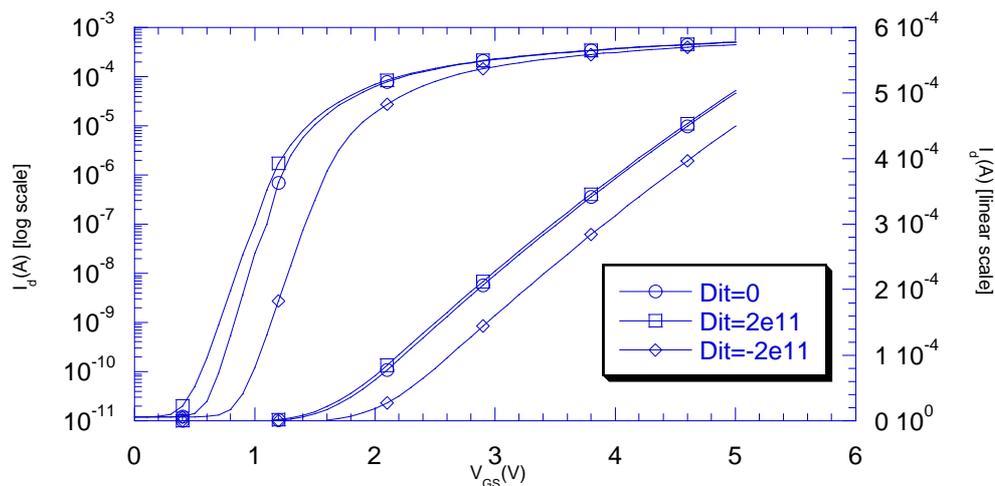
$$C_{ox}(V_G - V_{FB} - \psi_{s0}) = \frac{\gamma C_{ox}}{\sqrt{\beta}} \sqrt{(\beta\psi_{s0} - 1) + e^{\beta(\psi_{s0} - V_s - 2\phi_f)}} + \frac{q D_{it}}{\beta} [\beta(\psi_{s0} - V_s) + \ln(1 + e^{-\beta(E_g/2 - \phi_f + \psi_{s0} - V_s)})] \quad (2.3.6.6)$$

$$C_{ox}(V_G - V_{FB} - \psi_{sL}) = \frac{\gamma C_{ox}}{\sqrt{\beta}} \sqrt{(\beta \psi_{sL} - 1) + e^{\beta(\psi_{sL} - V_D - 2\phi_f)}} \quad (2.3.6.7)$$

$$+ \frac{q D_{it}}{\beta} [\beta(\psi_s - V_D) + \ln(1 + e^{-\beta(E_g/2 - \phi_f + \psi_{sL} - V_D)})]$$



**Figure 2.2** Drain current components: The drift current,  $I_{d1}$ , and the diffusion current,  $I_{d2}$ . The device has  $W/L=50\mu/6\mu$ ,  $N_{sub}=5E16 \text{ cm}^{-3}$ , and  $Tox=40 \text{ nm}$ . [30]



**Figure 2.3** Drain current for different interface trapped charge densities. Positive  $D_{it}$  are donor like traps, while negative  $D_{it}$  are acceptor like. The device has  $W/L=50\mu/6\mu$ ,  $N_{sub}=5E16 \text{ cm}^{-3}$ , and  $Tox=40 \text{ nm}$  [30].

Fig. 2.2 shows the current components: the drift current component,  $I_{D1}$ , and the diffusion current component,  $I_{D2}$ . The logarithmic scale is used to show the exponential subthreshold current. The plot is computed by the model using equations (2.3.6.4) and (2.3.6.5). Fig. 2.3, on the other hand, shows the effect of the interface trapped charge density  $D_{it}$  on the total drain current. The curve for  $D_{it}=2E11$   $1/(\text{cm}^2\text{e.V.})$ , only donor-like traps are considered to be present, i.e. the interface trapped charge is a positive one. As shown in Fig. 2.3, as  $V_{GS}$  increases the surface potential  $\psi_s$  increases, more trap levels capture new electrons, empty levels thus decreases and so is the interface trapped charge, thus the curve approaches that for  $D_{it}=0$ . The curve for  $D_{it}=-2E11$   $1/(\text{cm}^2\text{e.V.})$ , only acceptor-like traps are considered to be present, i.e. the interface trapped charge is a negative one. As shown from Fig. 2.3, as  $V_{GS}$  increases the surface potential  $\psi_s$  increases, more trap levels capture new electrons, filled levels thus increases and so is the interface trapped charge, thus the curve deviates more from that for  $D_{it}=0$ . As shown the interface trapped charge affects both the slope of the subthreshold characteristics (shown on the logarithmic scale), as well as the threshold voltage value. It is to be noted that the slope of the subthreshold characteristics is equal for equal densities of interface trapped charge  $D_{it}$ , irrelevant of the type of this traps.

## 2.4 The Short Channel Model

The two major goals of MOSFET scaling are to increase the density and speed of the digital ICs in which such scaled down devices are used. Increasing density of course means using smaller channel lengths and widths, also increasing speed means to increase saturation drain current  $I_{D\text{sat}}$  (to allow faster charging and discharging of parasitic capacitance).

Long-Channel MOSFET Behavior	Short-Channel MOSFET Behavior
The threshold voltage $V_T$ is independent of channel length $L$ and channel width $W$	$V_T$ is decreased as $L$ is decreased, and may be also affected by changes in $W$
$V_T$ is independent of drain voltage	$V_T$ decreases with increasing $V_{DS}$
$V_T$ depends on $V_{BS}$ according to equation (2.6.15)	$V_T$ increases less rapidly with $V_{BS}$ than predicted by equation (2.6.15)
The subthreshold current $I_{Dst}$ increases linearly as $L$ decreases	$I_{Dst}$ increases more rapidly than linearly as $L$ decreases
$I_{Dst}$ is independent of drain bias	$I_{Dst}$ increase with increasing $V_{DS}$
The subthreshold swing $S_t$ is independent of gate length	$S_t$ increases with decreasing $L$
The drain saturation current $I_{Dsat}$ is independent of $V_{DS}$	$I_{Dsat}$ increases as $V_{DS}$ increases
$I_{Dsat}$ is proportional to $(V_{GS}-V_T)^2$	$I_{Dsat}$ is proportional to $(V_{GS}-V_T)$
$I_{Dsat}$ is proportional to $1/L$	As $L \rightarrow 0$ , $I_{Dsat}$ becomes indep. of $L$

**Table 2.1** Comparison of Long-Channel and Short-Channel MOSFETs  
C/Cs

From long-channel current equation discussed in the previous section it is apparent that this may be achieved by either reducing channel length ( $L$ ), oxide thickness  $t_{ox}$ , or both. The long channel equation predicts an indefinite increase in  $I_{Dsat}$  by this decrease in  $L$  and  $t_{ox}$ , seeming to imply that only the limitations of process technology (and not device effects) prevent the manufacture of even smaller, higher-performing MOSFETs.

However, as process technology improved to the point where channel lengths smaller than  $\sim 1 \mu\text{m}$  were fabricated, it turned out that MOSFETs began to exhibit phenomena not predicted by the long channel MOSFET models. Such phenomena were thus termed *short channel effects*.

Table 2.1 show us a brief comparison between long and short channel MOSFETs model which will be discussed in the following sections.

Two- and three-dimensional analyses can be carried out numerically with the help of a computer [31]. However, such analyses, although accurate, do not provide a simple model for efficient calculation. Thus, much has been done on the way to simplification by using empirical approximations and semi-empirical approaches. In these approaches, usually the complex two- or three-dimensional phenomena are broken down into simple, separate phenomena *examined one at a time*. A number of simplifying assumptions are then made, and relatively simple relations are derived. Often such techniques are characterized by an attempt to maintain the general form of the  $I$ - $V$  relations for the long- and wide-channel devices, and to *stretch* these relations by modifying them somewhat so that they can be used in the case of short and/or narrow channels.

### 2.4.1 Channel Length Modulation

The GCA is assumed to be valid in the whole channel, except in the regions near the source and the drain. The net effect can then be taken into account by replacing the channel length  $L$  in the current equations by an equivalent channel length  $L_{eff}$ , in which the GCA is still valid. It is now required to calculate this effective channel length.

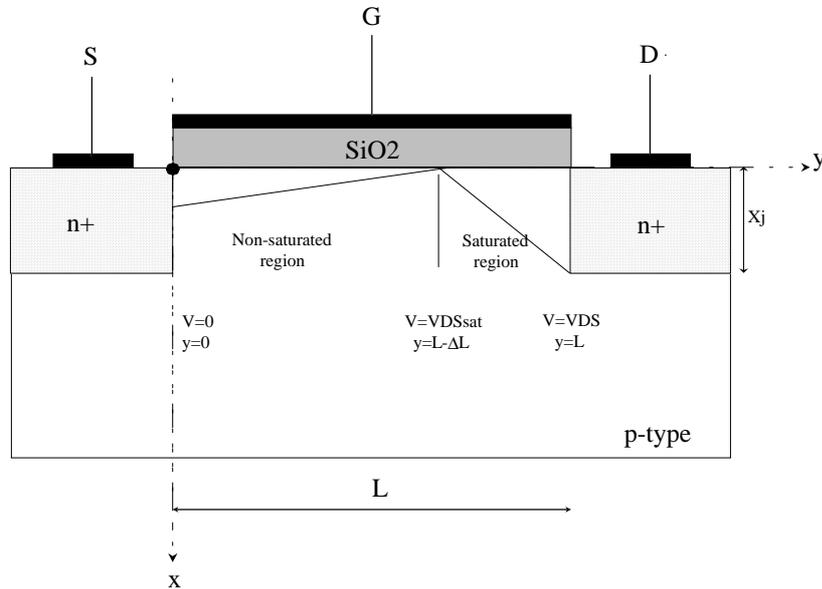
#### A) Subthreshold Operation

Since the channel is nearly depleted of carriers, we can use the abrupt  $p$ - $n$  junction approximation to compute the length of the depletion regions

near the source and drain [32,33], i.e. applying the depletion approximation for these two regions and solving Poisson's equation in the  $x$ -direction, we get

$$L_s = \sqrt{\frac{2\epsilon_s}{qN_A}(V_{bi} + V_s - \psi_{s0})} \quad (2.4.1)$$

$$L_d = \sqrt{\frac{2\epsilon_s}{qN_A}(V_{bi} + V_D - \psi_{sL})} \quad (2.4.2)$$



**Figure 2.4** Schematic representation of a MOSFET in saturation, where the channel is divided into a non-saturated region and a saturated region.

where  $L_s$  and  $L_d$  are the lengths of the source and drain depletion regions respectively,  $V_{bi}$  is the built in potential of the source and drain regions,  $V_{bi} = \phi_t \ln((N_A N_{sd})/n_i^2)$ ,  $\psi_{s0}$  and  $\psi_{sL}$  are the surface potentials at the source and drain ends of the channel respectively referenced to the bulk.

The channel length  $L$  in the diffusion current component (which represent subthreshold conduction) is replaced by the effective channel length equal to  $(L-L_s-L_d)$ .

## B) Strong Inversion Operation

When a MOSFET is biased in saturation, the GCA fails in a small region near the drain. This so-called saturated part of the channel is characterized by a two-dimensional electric field pattern. Hence it is natural to describe the channel in terms of a two region model, as indicated in Fig. 2.4.

The long channel model discussed in the previous chapter takes into consideration the strong inversion saturation operation by allowing the inversion charge near the drain to drop to very small values (pinch-off condition) and the current is continuous from the linear to the saturation region.

Fig. 2.4 shows a transistor in saturation with  $V_{DS}$  greater than  $V_{DSsat}$ . The channel cannot support more voltage than  $V_{DSsat}$ , since it becomes pinched off when the voltage across it reaches that value. The *excess* voltage  $V_{DS} - V_{DSsat}$  must then be dropped between the drain and the tip of the channel. Such a nonzero voltage can only exist over a region of nonzero length  $\Delta L$ , as shown. If  $V_{DS}$  is raised still further, more excess voltage must be dropped across this region. To support this voltage, the region must widen, and the inversion layer will shrink somewhat in length. This channel length shortening  $\Delta L$  is found to be of the form [34]:

$$\Delta L = L \frac{\sqrt{V_{sl}^2 + 2A(1 + BI_{Dsat})(V_D - V_{Dsat})} - V_{sl}}{A(1 + BI_{Dsat})} \quad (2.4.3)$$

where

$$\begin{aligned} V_{sl} &= F_{\max} L \\ A &= qN_A L^2 / 2 \epsilon_s \\ B &= [\ln(x_j / d_{inv}) - 1] / (qN_A W v_{\max} x_j) \end{aligned} \quad (2.4.4)$$

### 2.4.2 Velocity Saturation

As indicated in the previous section, the long channel model takes into consideration the strong inversion saturation operation by allowing the inversion charge near the drain to drop to very small values, i.e. pinch off, thus the carrier velocity is assumed to approach infinity. This description works reasonably well for long-channel devices, but the notion of an infinite carrier velocity is, of course, unphysical. Instead, current saturation is better described in terms of a saturation of the carrier velocity when the electric field near the drain becomes sufficiently high.

An approximation often used for the carrier mobility to represent this effect is [21]

$$\mu_{eff} = \frac{\mu_g}{\left[1 + \left(\frac{\mu_g F_x}{v_{max}}\right)^m\right]^{1/m}} \quad (2.4.5)$$

where  $\mu_g$  is the mobility including the gate scattering effects (equal to the effective mobility taking only the gate field scattering effect into consideration, calculated in Section 1.4),  $F_x$  is the lateral electric field approximated by the average value  $F_x = (\psi_{sL} - \psi_{s0})/L$ , and  $m=2$  for electrons, and  $m < 2$  for holes. Note that the functional form of the effective mobility is the same as the smoothing function (Section 1.6), with  $x = \mu_g$ , and  $x_o = F_x/v_{max}$  which is plotted in Fig. 1.9 for different values of  $m$ .

The long channel current model discussed above does not include the effects of velocity saturation in the channel at high drain-source bias. An extension of this model, incorporating velocity saturation, is to consider the effect of velocity saturation on the saturation voltage  $V_{DSsat}$ .

In order to calculate  $V_{DSsat}$ , taking the effect of velocity saturation, an analysis is carried to get the following results :

$$I_{Dsat} = \beta_g V_L^2 \left[ \sqrt{1 + \left(\frac{V_{GT}}{V_L}\right)^2} - 1 \right] \quad (2.4.6)$$

where

$$\beta_g = C_{ox} \mu_g \frac{W}{L} \quad (2.4.7)$$

is the transconductance parameter, and  $V_{GT} = V_G - V_T$ .

$$\begin{aligned} V_L &= F_{max} L \\ F_{max} &= F_x(L) \end{aligned} \quad (2.4.8)$$

$$V_{DSsat} = V_{GT} - \frac{I_{Dsat}}{\beta_g V_L} = V_{GT} + V_L - \sqrt{V_{GT}^2 + V_L^2} \quad (2.4.9)$$

We use here a modification to eq. (2.4.9), in order to improve the accuracy of  $V_{DSsat}$  calculation, by substituting  $V_{GT}$  with  $V_{GT}/(1+FB)$ , where  $FB$  is given by  $FB = 1/(2(1+2\phi_f+V_S)^{1/2})$ . The physical origin of this  $(1+FB)$  factor is to try to compensate for the variation of the bulk charge with potential neglected while calculating the current to get equation (2.4.6).

This last equation for  $V_{DSsat}$  is of course meaningful only above threshold where  $V_G > V_T$ .

In order to incorporate this velocity saturation effect in our model, we have to limit the drain-source voltage  $V_{DSsat}$ . To avoid model discontinuities, we perform this limiting using the smoothing function (refer to Section 1.6). Thus in model equations we use a modified drain-source voltage, namely  $V_{DS1} = SF(V_{DS}, V_{DSsat}, I0)$ , which approaches  $V_{DS}$  in the linear region when  $V_{DS} < V_{DSsat}$ , and tends to  $V_{DSsat}$  in saturation when  $V_{DS} > V_{DSsat}$ .

As mentioned above, the drain-source saturation voltage  $V_{DSsat}$  tends to zero below threshold, and so does the modified drain-source voltage  $V_{DS1}$ . Since the drift current component also tends to zero below threshold, this does not affect the accuracy of the model. But for the diffusion current component we can't use this modified drain-source voltage during its calculation. Another drain-source voltage  $V_{DS2}$  is used that tends to  $V_{DS}$  below threshold, and to  $V_{DS1}$  above threshold. The modified drain-source voltages used in the calculation of the drift and diffusion current components are thus given by

$$V_{DS1} = \frac{V_{DS}}{[1 + (\frac{V_{DS}}{V_{DSsat}})^{10}]^{1/10}} \quad (2.4.10)$$

$$V_{DS2} = V_{DS}(1 - XI) + V_{DS1} XI \quad (2.4.11)$$

where

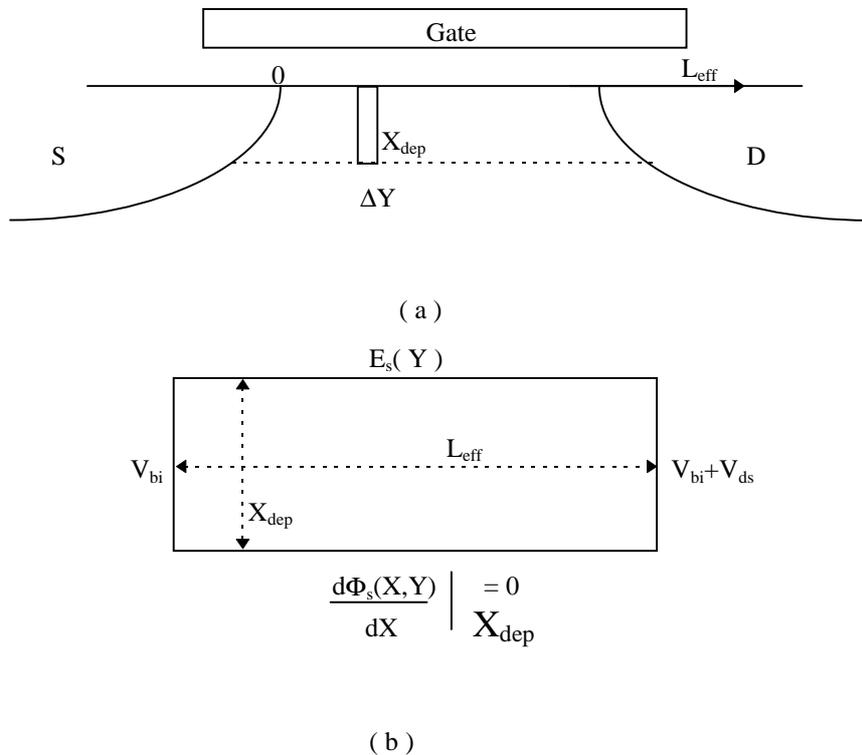
$$XI = \frac{(V_G/V_T)^{1.5}}{1 + (V_G/V_T)^{1.5}} \quad (2.4.12)$$

and

$$V_T = 2\phi_f + 6\phi_t + V_s + \gamma\sqrt{2\phi_f + 6\phi_t + V_s} \quad (2.4.13)$$

### 2.4.3 Drain induced barrier lowering

It has been observed experimentally that the threshold voltage does not remain the same if the length  $L$  is reduced. As the channel length continues to decrease, the depletion layer of the drain starts to interact with the source-channel junction to lower the source junction potential barrier. This is known as *drain induced barrier lowering* (DIBL).



**Figure 2.5** Diagram showing (a) the Gaussian box used in the quasi-two-dimensional analysis, (b) the boundary conditions for solving eq. (2.4.14).

[35]

The lowering of the source barrier allows electrons to be injected into the channel regardless of the gate voltage. As a result, the gate voltage loses control of the drain current in the subthreshold regime.

To describe this effect analytically, we have two approaches:

- i. The charge sharing approach [32,33].
- i .Solving Poisson's equation in the depletion region, between the source and drain region [35-37].

We use here the second approach as it yields a better representation of the DIBL as shown in [36].

Solving Poisson's equation in the depletion region was done by many authors [33,34,36], each introducing his own simplifications. In our model, we use the method introduced recently by Liu [35], as it gives satisfactory results in representing the threshold voltage shift produced by the DIBL. The derivation is demonstrated as shown below:

Here, we proceed to develop a model for the distribution of the surface potential,  $\psi_s$ . From such a model, it is possible to calculate the interface potential near its minimum, which defines the barrier for charge injection into the channel. In principle, this involves the solution of a two-dimensional Poisson's equation for the whole device, using proper boundary conditions.

By applying Gauss' law to a rectangular box of height  $X_{dep}$  and length  $\Delta y$  in the channel depletion region Fig. 2.5 and neglecting mobile carrier charge, the following equation can be derived:

$$\epsilon_s \frac{X_{dep}}{\eta} \frac{\partial F_y(y)}{\partial y} + \epsilon_o \frac{V_G - V_{FB} - \phi_s(y) - V_S}{T_{ox}} = q N_A X_{dep} \quad (2.4.14)$$

where  $F_x(y)$  is the lateral surface electric field.  $\phi_s$  is the surface potential referenced to the interior bulk potential at  $V_S = 0$ ,  $V_G$  and  $V_S$  are the gate and source potentials referenced to the bulk potential respectively. The depletion layer thickness,  $X_{dep}$ , is equal to

$$X_{dep} = \sqrt{\frac{2 \epsilon_s (\phi_{si} + V_s)}{q N_A}} \quad (2.4.15)$$

where  $\phi_{si}=2\phi_f$  is the surface potential at the threshold of surface inversion, and  $\eta$  is a fitting parameter.

The first term on the left hand side of eq. (2.4.14) is equal to the net electric flux entering the Gaussian box along the  $y$  direction. The second term represents the electric flux entering the top surface of the Gaussian box. There is no electric flux passing through the bottom of the Gaussian box.

The solution to eq. (2.4.14) under the boundary conditions of  $\phi_s(0)=V_{bi}$  and  $\phi_s(L)=V_{DS}+V_{bi}$  is

$$\phi_s(y) = V_{sL} + (V_{bi} + V_{DS} - V_{sL}) \frac{\sinh(y/l)}{\sinh(L/l)} + (V_{bi} - V_{sL}) \frac{\sinh[(L-y)/l]}{\sinh(L/l)} \quad (2.4.16)$$

In eq. (2.4.16),  $V_{sL} = V_{GS} - V_{tho} + \phi_{si}$  represents the long-channel surface potential, and  $V_{tho} = V_{FB} + qN_a X_{dep} T_{ox} / \epsilon_o + \phi_{si}$  represents the long channel threshold voltage.  $V_{bi}$  is the built-in potential between the source-substrate and drain-substrate junctions, and  $l$  is the characteristic length defined as

$$l = \sqrt{\frac{\epsilon_s T_{ox} X_{dep}}{\epsilon_o \eta}} \quad (2.4.17)$$

Note that  $X_{dep}$  is assumed to be a constant when solving eq. (2.4.14). In reality,  $X_{dep}$  is a function of the drain voltage and the channel length [35]. One may treat the term  $X_{dep}/\eta$  in eq. (2.4.17) as an average of the depletion layer thickness along the channel.

At a given  $V_G$ ,  $V_B$ ,  $V_D$ , the channel potential distribution calculated using eq. (2.4.17) is plotted in Fig. 2.6 for devices of different channel lengths.

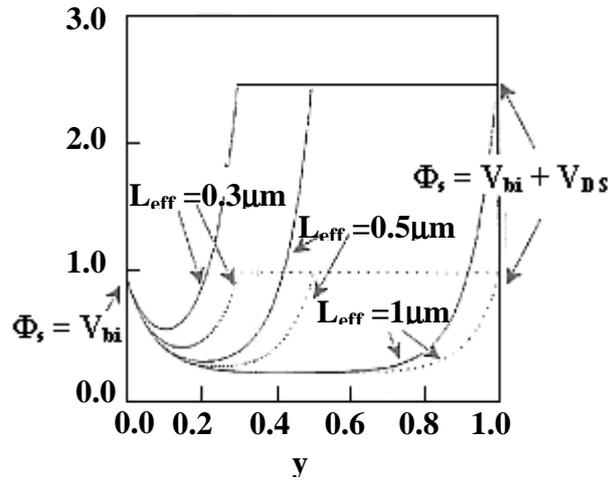
The model [35] predicts a large variation in potential along the channel for devices with short-channel length even when the drain voltage is low. The

channel potential has a minimum at  $y_o$  which can be found by solving the equation  $d\phi_s(y)/dy = 0$ . The minimum value of channel potential increase, i.e. the potential barrier for electron flow from source to drain will decrease, with decreasing channel length and increasing the drain voltage. Location  $y_o$  and minimum potential  $\phi_s$  can be obtained by solving

$$\begin{aligned} \phi_{smin} &= \phi_s(y_o) \\ \frac{\partial \phi_s}{\partial y} \Big|_{y=y_o} &= 0 \end{aligned} \quad (2.4.18)$$

For  $L \gg l$  and small  $y$ , eq. (2.4.16) can be approximated as

$$\phi_s(y) = V_{sL} + (V_{bi} + V_{DS} - V_{sL})e^{(y-L)/l} + (V_{bi} - V_{sL})e^{-y/l} - (V_{bi} + V_{DS} - V_{sL})e^{-L/l} \quad (2.4.19)$$



**Figure 2.6** Calculated surface potential along the channel for different channel lengths. The dashed lines show the data for  $V_{DS}=0.05V$  and the solid lines show the data for  $V_{DS}=1.5V$ . [35]

Using eqs (2.4.18) and (2.4.19),  $y_o$  can be found to be

$$y_o = \frac{L}{2} - \frac{l}{2} \ln\left(\frac{V_{bi} - V_{sL} + V_{DS}}{V_{bi} - V_{sL}}\right) \quad (2.4.20)$$

Then using eq. (2.4.16),  $\phi_{smin}$  can be found using eq. (2.4.14)

$$\phi_{smin} = V_{sL} - (V_{bi} + V_{DS} - V_{sL})e^{-L/l} + 2\sqrt{(V_{bi} - V_{sL} + V_{DS})(V_{bi} - V_{sL})}e^{-L/l} \quad (2.4.21)$$

Thus, defining the threshold voltage as the gate voltage which causes  $\phi_{smin}$  to be equal to  $2\phi_f$ ,  $V_{th}$  can be solved as [35]

$$V_{th}(L) = V_{th0} - \Delta V_{th} \quad (2.4.22)$$

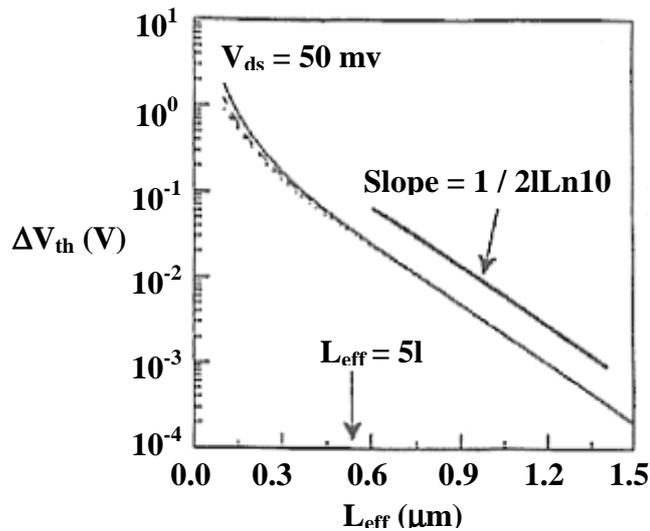
where

$$\Delta V_{th} = \frac{2V_1 + V_2(1 - e^{-L/l}) + 2\sqrt{V_1^2 + V_1V_2(e^{L/l} - 1)}}{4\sinh^2(L/2l)} \quad (2.4.23)$$

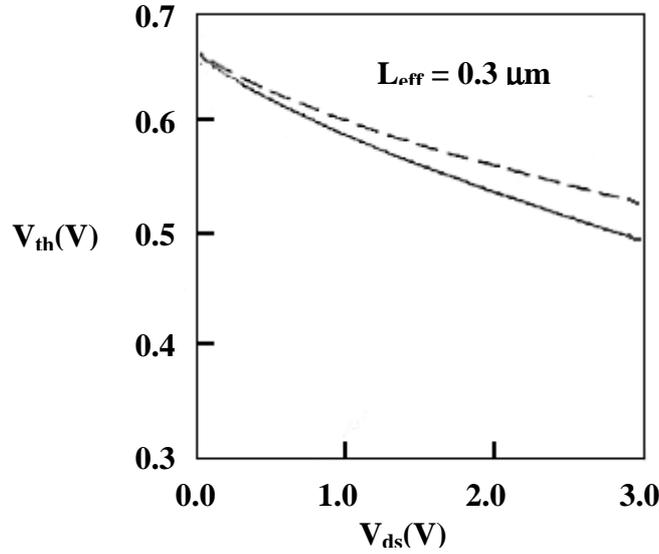
and

$$\begin{aligned} V_1 &= V_{bi} - \phi_{si} \\ V_2 &= V_1 + V_{DS} \end{aligned} \quad (2.4.24)$$

Figures 2.7 and 2.8 show this threshold shift given by eq. (2.4.23), versus the channel length  $L$  and the drain-source voltage  $V_{DS}$  respectively, compared to numerical simulations, obtained from [35].



**Figure 2.7** Calculated  $V_{th}$  shifts versus channel length at  $V_{DS} = 0.05$  V. The continuous line denotes numerical calculations, while the dashed one is obtained by eq. 2.4.23 [35].



**Figure 2.8** Calculated  $V_{th}$  shifts versus the drain voltage  $V_{DS}$  at a channel length of  $0.3\mu\text{m}$ . The continuous line denotes numerical calculations, while the dashed one is obtained by eq. 2.4.23.[35]

Although the calculated  $l$  from eq. (2.4.17) has the correct order of magnitude and function form, exact values of  $l$  need to be extracted from actual devices because of the unknown parameter  $\eta$ . The extraction of  $l$  can be done by fitting the experimental data of  $\log(\Delta V_{th})$  versus  $L_{eff}$  in the region of  $L_{eff} > 5l$ . Based on Fig. 2.7, the slope of the fitted straight lines is equal to  $1/(2l \ln 10)$ . According to, experimentally extracted  $l$ 's versus the depletion layer thickness  $X_{dep}$  for several technologies suggest that  $l$  is proportional to  $X_{dep}^{2/3}$ , i.e. not proportional to  $X_{dep}^{1/2}$  as suggested by 2.4.16. This can be interpreted as saying  $\eta$  is also a function of  $X_{dep}$ . An empirical relation for  $l$  has been established from experimental data, this empirical relation is [35]:

$$l = 0.1(y_j T_{ox} X_{dep}^2)^{1/DSB} \quad (2.4.25)$$

where  $DSB=3.0$  that's to say that  $l$  is proportional to  $(\phi_{si} + V_S)^{1/DSB}$ , refer to eq. (2.4.15). In our model this proportionality exponent ( $DSB$  in the last eq.) is taken as a model parameter which determines the variation of threshold voltage with the substrate bias.

Referring to Section 1.3.3, we recall that any variation in the flat band voltage appears directly as an equal variation in the threshold voltage value.

This fact is used in our model to account for the threshold shift caused by the DIBL by defining an *effective* flat band voltage given by

$$V_{FB}' = V_{FB} + \Delta V_{th} \quad (2.4.26)$$

where  $\Delta V_{th}$  is that threshold shift caused by DIBL.

In this section, the drain induced threshold voltage shift was analyzed in terms of the lowering of the injection barrier between the source and the channel in the subthreshold regime. In strong inversion, however, the injection barrier is reduced owing to the effect of the gate-source bias, and will eventually disappear well above threshold. Hence, the importance of DIBL will decrease with increasing gate-source voltage and should gradually be phased out [21]. To represent this effect in our model, the shift in the threshold voltage  $\Delta V_{th}$  is well reduced to zero above threshold by the following relations

$$V_T = 2.5(2\phi_f + \phi_t + V_S + \gamma\sqrt{2\phi_f + 6\phi_t + V_S}) \quad (2.4.27)$$

$$X2 = \frac{(V_G/V_T)^5}{1 + (V_G/V_T)^5} \quad (2.4.28)$$

$$V_{FB}' = V_{FB} + \Delta V_T(1 - X2) \quad (2.4.29)$$

#### 2.4.4 Series Resistance

The parasitic source/drain resistance due to carrier crowding in the source-to-channel and channel-to-drain regions, is an important device parameter which can affect the MOSFET performance significantly. While scaling down MOSFET channel length, parasitic resistance will not be proportionally scaled, and will become more and more of a problem. The straightforward and accurate way of modeling parasitic resistance effect leads to a complicated drain current expression. In order to make calculations

efficient, we model the parasitic resistance using simple expressions. Fig. 2.9 shows a MOSFET with parasitic resistance  $R_s$  and  $R_d$ . Assume  $R_s=R_d=R_t/2$ .

The effect of this parasitic resistance is apparent only in strong inversion where the drop across it is not negligible, thus we take into account its effect by considering strong inversion operation as follows:

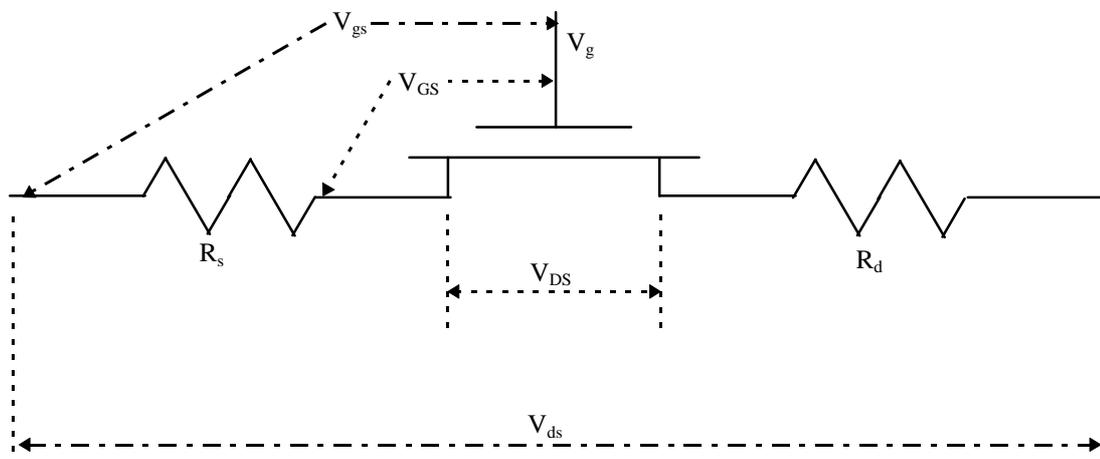
The intrinsic MOSFET model described in the last sections can be converted to an extrinsic model by expressing the intrinsic bias voltages (upper case subscripts) in terms of their extrinsic counterparts (lower case subscripts), i.e.

$$V_{DS} = V_{ds} - I_D R_t \quad (2.4.29)$$

$$V_{GS} = V_{gs} - I_D R_s \quad (2.4.30)$$

Thus the drain drift current reduces to [8]

$$I_D = \frac{W}{L_{eff}} C_{ox} \frac{\mu_{eff}}{\left(1 + \frac{W}{L_{eff}} \mu_{eff} C_{ox} R_t V_{GT}\right)} (V_{GT}) V_{ds} \quad (2.4.31)$$



**Figure 2.9** MOSFET with parasitic source and drain resistance.

We thus represent the effect of the parasitic series resistance by a reduction in the mobility as shown in the previous equation by defining an effective mobility taking into account the series resistance effect ,  $\mu_{eff}'$  , as follows:

$$\mu_{eff}' = \frac{\mu_{eff}}{\left(1 + \frac{W}{L_{eff}} \mu_{eff} C_{ox} R_t V_{GT}\right)} \quad (2.4.32)$$

Also, due to the parasitic resistance, the saturation voltage  $V_{DSsat}$  will be larger than what is predicted by eq. (2.4.9). A calculation of the modified  $I_{DSsat}$  yield [34]:

$$I_{DSsat} = \beta_g V_L^2 \frac{\sqrt{1 + 2\beta_g V_{gt} R_s + (V_{gt} / V_L)^2} - (1 + \beta_g V_{gt} R_s)}{(1 - (\beta_g V_L R_s)^2)} \quad (2.4.33)$$

where  $V_L$  is given by eq. (2.4.8). The extrinsic saturation voltage,  $V_{dssat}$ , can be obtained in the form:

$$\begin{aligned} V_{dssat} &= V_{DSsat} + R_t I_{DSsat} \\ V_{dssat} &= V_{gt} + \left( R_d - \frac{1}{\beta_g V_{ss}} \right) I_{DSsat} \end{aligned} \quad (2.4.34)$$

### 2.5.5 Impact Ionization and the Substrate Current

As characteristic device sizes are scaled down, the electric field in the MOSFET channel increases and, in the saturation regime, the high field region near the drain occupies a large fraction of the device channel. This leads to the so-called hot carrier effects which manifest themselves as a superlinear increase of the drain current in the saturation regime and in the degradation of device parameters with time.

The physics of impact ionization can be described as follows: The high electric field near the drain leads to electron heating. Some electrons acquire so much energy from the electric field that they can cause generation of electron-hole pairs. The generated holes lead to a substrate current whereas the generated electrons increase the drain current. The process of

electron-hole pair generation can be described by a generation rate per unit length  $\alpha(F_x)$  defined by [2,34]

$$\alpha(F_x) = A \exp(-B / F_x) \quad (2.4.35)$$

where  $F_x$  is the tangential electric field,  $A$  and  $B$  are impact ionization constants.

The substrate current,  $I_{st}$  due to impact ionization can thus be calculated by the following formula [38]:

$$I_{st} = I_D \int_{L_{eff} - \Delta L}^{L_{eff}} \alpha(F_x) dx \quad (2.4.36)$$

The tangential field is computed by its average value

$$F_{xav} = \frac{V_{DS} - V_{DSsat}}{\Delta L} \quad (2.4.37)$$

$\Delta L$  is the length of the *impact ionization region* given by

$$\Delta L = l \ln \left( \frac{2(V_{DS} - V_{DSsat})}{lE_{max}} \right) \quad (2.4.38)$$

where  $l$  is a parameter which characterizes the electric field distribution in the impact ionization region.  $l$  depends on  $T_{ox}$  and the junction depth  $y_j$  and is given by

$$l = \sqrt{\frac{\epsilon_s}{\epsilon_{ox}} T_{ox} y_j} \quad (2.4.39)$$

Equation (2.4.38) has been obtained by applying Poisson's equation to the saturated part of the channel (refer to Fig. 2.4) [39].

Substituting with equations (2.4.35), (2.4.37), and (2.4.38) into eq. (2.4.36) we get

$$I_{st} = A I_D (V_{DS} - V_{DSsat}) \exp\left(-\frac{Bl}{V_{DS} - V_{DSsat}}\right) \quad (2.4.40)$$

## 2.5 Narrow Channel Effect

The reduction of channel width causes an increase of the threshold voltage [2]. This shift is related to the depletion region spreading laterally in the substrate along the width (see Fig. 2.10). Assuming that the lateral extension of the depletion region is approximately cylindrical, the total charge in the depletion region,  $Q_B$ , is thus

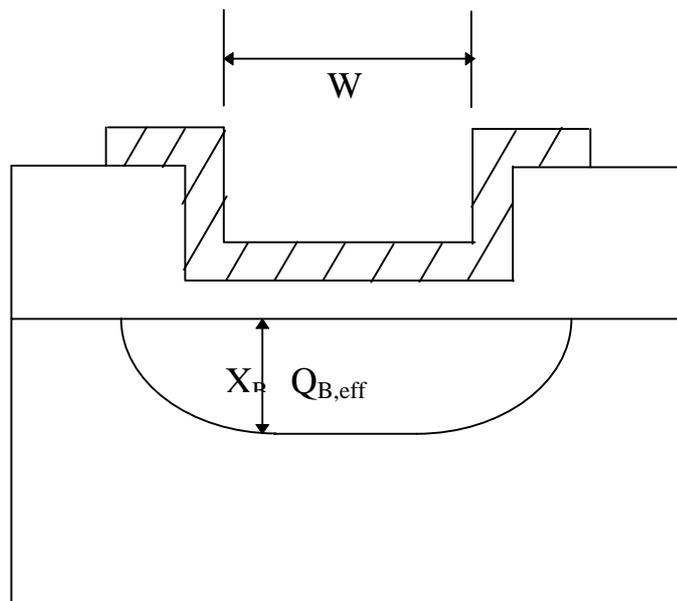
$$Q_B = q N_A L W X_B \left(1 + \frac{\pi X_B}{2 W}\right) \quad (2.5.1)$$

This last equation shows that the bulk charge has increased by a factor of  $(1 + \pi X_B / 2 W)$ . Therefore, the threshold voltage is increased by

$$\Delta V_{th} = \frac{\pi q N_A X_B^2}{2 C_{ox} W} = \pi \frac{\epsilon_s T_{ox}}{\epsilon_{ox} W} (\phi_{si} + V_S) \quad (2.5.2)$$

where  $\phi_{si}$  is the surface potential referenced to the source potential at threshold ( $=2\phi_f$ ).

Similar to the effect of the DIBL, this shift is added to the effective flat-band voltage as in eq. (2.5.25).



**Figure 2.10** Depletion charge along the width of the transistor.

## 2.6 Non uniform doping [40]

In the model discussed above, a uniform substrate doping has been assumed. For practical MOSFETs this assumption is not valid, since ions are normally implanted in the region between the source and the drain, to control threshold voltage and punchthrough of the drain region to the source. Implantation has two aspects, first, new ions are introduced into the depletion layer. Second, these newly introduced ions modify the depletion width. Both effects modify MOSFET behavior, in both strong or weak inversion regions.

### 2.6.1 Non uniform doping profile

In dealing with the enhancement mode MOSFET having an ion-implanted channel, the impurity profile chosen plays a main role in the prediction of the device behavior and also in the simulation time taken by CAD tools especially for large numbers of devices. The most simple model achieved using the so called box profile (step profile) is suitable for CAD tools and is now implemented in BSIM3 model, but this profile proves to give an error as large as a few tenths of a volt in terms of the threshold voltage at a substrate bias of the order of a few volts. This discrepancy is quite large considering a usually designed threshold voltage in the order of 1 V. But also the use of Gaussian profile which is of course in agreement with the implantation process give rise to complicated calculations required by the simulator due to the presence of the error function as a direct result of using the Gaussian profile in Poisson's equation. The chosen profile is a power profile which for some order range gives a good agreement with the Gaussian profile, it takes the following form :

$$N(y) = N_B + (N_o - N_B)(1 - (x/D))^n \quad (2.6.1)$$

where  $N_B$  represents the bulk impurity concentration,  $N_o$  represents the impurity concentration at the channel surface,  $D$  represents the total depth

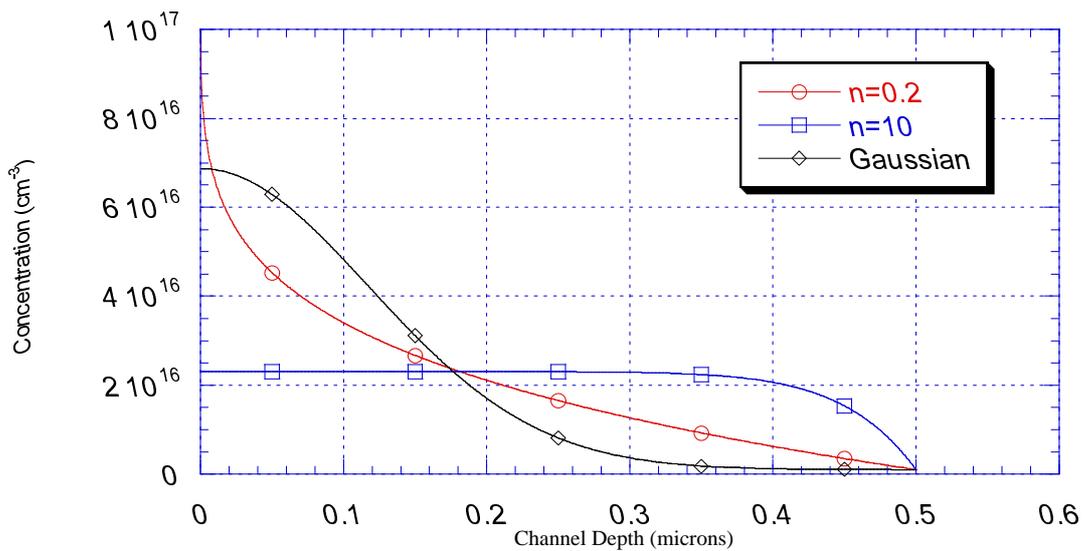
of the implanted layer at the final step of fabrication,  $x$  is the in-depth distance from the channel surface and  $n$  is a positive real number determining the shape of the impurity profile.

Using Fig. 2.11 we may calculate the value of  $N_0$  from the assumption of constant implanted dose; i.e.

$$Dose = \int_0^D (N(x) - N_B) dx \quad (2.6.2)$$

which yields  $N_0$  in the form :

$$N_0 = (1 + 1/n)(Dose/D) + N_B \quad (2.6.3)$$



**Figure 2.11** Comparison between Gaussian profile and suggested profile using equation (2.6.1) for  $n=0.2$  and  $n=10$

From Fig. 2.11 it is clear that the value of  $n=0.2$  will give a behavior close to the Gaussian one, while  $n=10$  will give a behavior close to the box profile discussed earlier. So we shall take the value of  $n=0.2$  in our model. Now if we substitute by the impurity profile into the one dimensional Poisson's equation we may solve it to get the depletion width as follow :

i) For  $W \leq D$

$$\frac{2}{n+2} \left( \frac{N_o}{N_B} - 1 \right) \left( \frac{W}{D} \right)^{n+2} - \frac{N_o}{N_B} \left( \frac{W}{D} \right)^2 + \frac{V}{V^*} = 0 \quad (2.6.4)$$

ii) For  $W \geq D$

$$W = D \sqrt{1 + \frac{V}{V^*} - \frac{1}{n+2} \left( n \frac{N_o}{N_B} + 2 \right)} \quad (2.6.5)$$

where  $V = 2\phi_f - V_B$ ,  $V^* = qN_B D^2 / (2\epsilon_s)$  with  $V_B$  being the substrate bias,  $\phi_f$  is the Fermi potential, and  $\epsilon_s$  is the dielectric constant of the substrate material. The depletion width will play a main role in our model as will be shown in the next section. The critical value of  $V$  at which  $W=D$  is determined by direct substitution in (2.6.4) or (2.6.5), if we denote this value by  $V_{thro}$  we obtain :

$$V_{thro} = \frac{1}{n+2} \left( n \frac{N_o}{N_B} + 2 \right) V^* \quad (2.6.6)$$

## 2.6.2 Model implementation

In our model we assume that the effect of the implanted layer is the modification of MOSFET parameters which is doping dependent such as Fermi voltage  $\phi_f$ , and body factor  $\gamma$ . Of course this variation is from high bulk doping when the depletion layer width is much smaller than  $D$  to light bulk doping when it is much greater than  $D$ , also this variation must be simple and continuous to fulfill the simulator requirements. So we use the smoothing function discussed in Section 1.6 of the form  $SF(1, 1/W_n, m)$

The parameters are suggested to vary according to the following simple equation :

$$\theta = \theta_l + SF(W_n) \cdot (\theta_h - \theta_l) \quad (2.6.7)$$

where  $\theta$  represents the parameter of interest, which is doping dependent, suffix  $l$  stands for lightly doped bulk ( $N_B$ ), and suffix  $h$  stands for highly doped bulk  $N_o$ .

The dependent parameters which are chosen in our model are Fermi voltage ( $\phi_f$ ), body factor ( $\gamma$ ), and fixed oxide charge ( $N_{ox}$ ).

The high and low doping values will be shown below :

$$\phi_{fl} = \phi_T \cdot \ln\left(\frac{N_B}{n_i}\right) \quad (2.6.8)$$

$$\phi_{fh} = \phi_T \cdot \ln\left(\frac{N_o}{n_i}\right) \quad (2.6.9)$$

$$\gamma_l = \frac{\sqrt{2 \cdot q \cdot \epsilon_s \cdot N_B}}{C_{ox}} \quad (2.6.10)$$

$$\gamma_h = \frac{\sqrt{2 \cdot q \cdot \epsilon_s \cdot N_o}}{C_{ox}} \quad (2.6.11)$$

$$N_{oxl} = N_{ox} + Dose \quad (2.6.12)$$

$$N_{oxh} = N_{ox} \quad (2.6.13)$$

where  $n_i$  is the intrinsic concentration of the semiconductor material,  $\phi_T$  is the thermal voltage and  $C_{ox}$  is the oxide capacitance.

### 2.6.3 Effect on threshold voltage

Now we shall use the proposed model to calculate the threshold voltage dependence on the substrate bias and compare the results with the experimental data.

The used formula is the usual formula for large channel MOSFET which is :

$$V_T = V_{FB} + 2\phi_f + \gamma \sqrt{2\phi_f - V_{bs}} \quad (2.6.15)$$

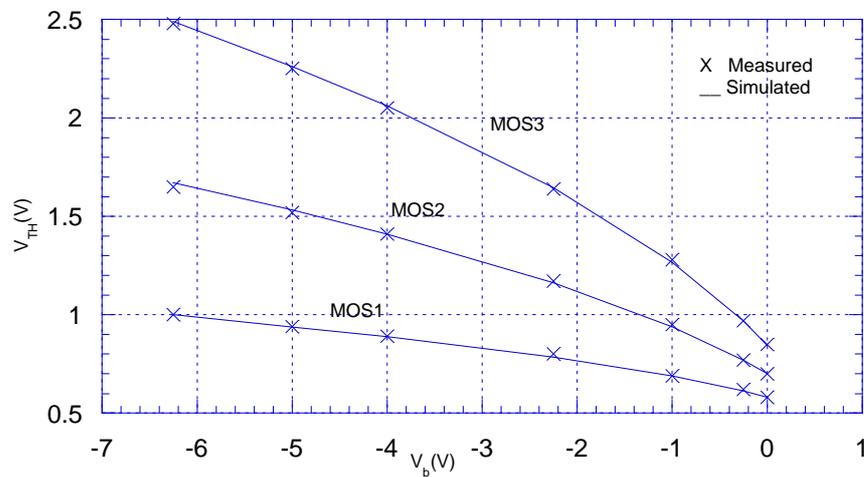
where  $V_{FB}$  is the flat band voltage which depends on  $N_{ox}$ .

We shall refer to the sample devices by MOS1, MOS2 and MOS3 where their parameters are as shown in Table 2.2. The obtained results are shown in Fig. 2.12, and the percentage error in  $V_T$  is plotted in Fig.2.13.

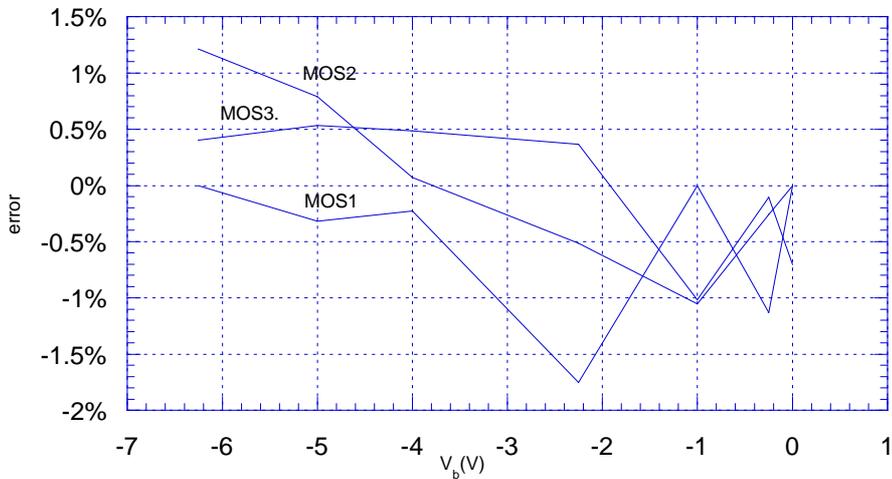
From Fig. 2.12 it is clear that, the results obtained using the proposed model are in good agreement with the experimental results.

Sample	MOS1	MOS2	MOS3
$t_{\text{ox}}$ (Angstroms)	500	710	300
$N_{\text{B}}$ (atom/cm <sup>3</sup> )	$7 \times 10^{14}$	$1.8 \times 10^{15}$	$2.5 \times 10^{16}$
Dose (atom/cm <sup>2</sup> )	$1 \times 10^{12}$	$2.2 \times 10^{11}$	$5.5 \times 10^{11}$
$D$ (microns)	0.3187	0.3586	0.3928

**Table 2.2** Sample devices parameters

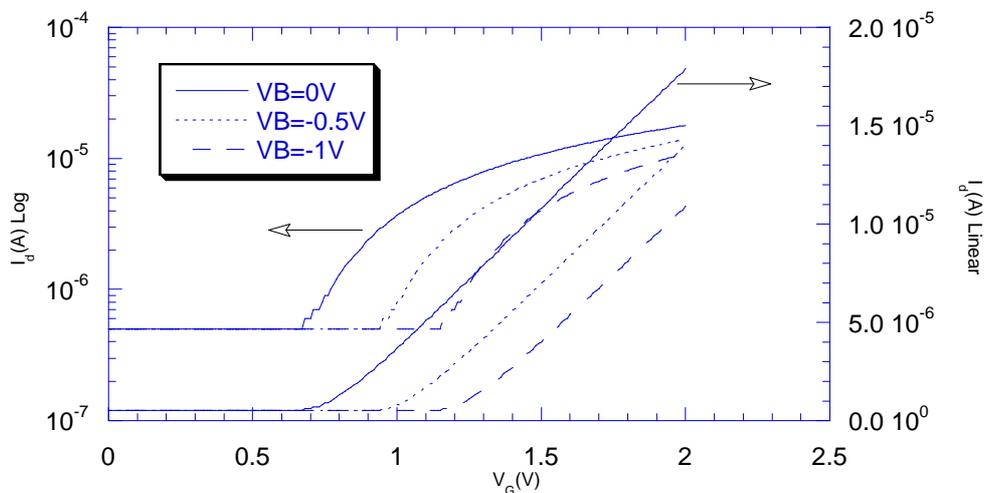


**Figure 2.12** Obtained results for sample devices in Table 2.2

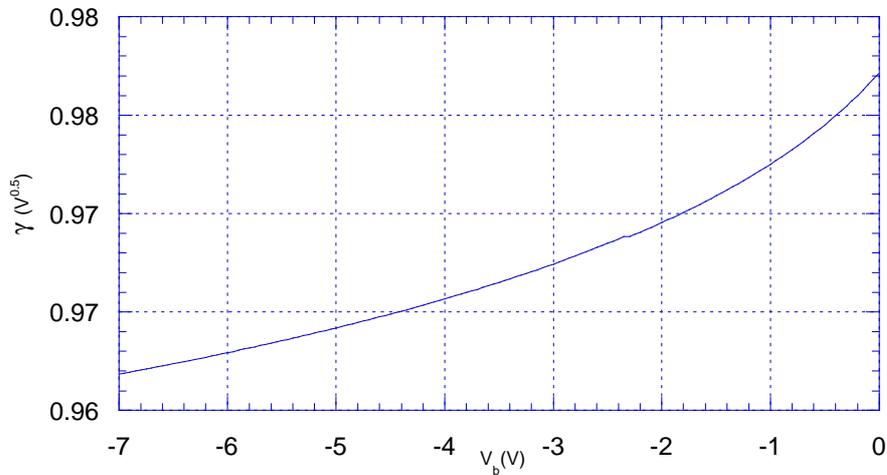


**Figure 2.13** Percentage error in the threshold voltage calculations for sample devices in Table 2.2.

Since the slope of the drain current in subthreshold region depends mainly on the body factor, it is clear that this model will predict the behavior in this region. Fig. 2.14 shows the drain current versus gate voltage for the sample device MOS3, and Fig. 2.15 shows the body factor variation for the same sample.



**Figure 2.14** Drain current dependence on the substrate bias at subthreshold region .



**Figure 2.15** Variation of the body factor ( $\gamma$ ) parameter for sample device MOS3

## 2.7 Temperature effects

MOS transistor characteristics are strongly temperature-dependent [2,8,39]. The threshold voltage is found to exhibit an almost linear decrease with temperature, thus as temperature increases, the drain current also increases due to the decrease in threshold voltage. The current is also affected by temperature through the carrier mobilities, since also the effective mobility is decreased with temperature.

Temperature effects are included in the model through the following parameters: The parameter  $n_i$ , the concentration of intrinsic carriers,  $E_g$ , the energy gap and  $\mu_o$ , the low field mobility, where all depend on temperature through the following semi-empirical relations [2,39,41]:

$$n_i = 1.45 \times 10^{10} \left( \frac{T}{300} \right)^{1.5} e^{l \frac{q E_g}{2K} \left( \frac{1}{300} - \frac{1}{T} \right)} \quad (2.7.1)$$

$$E_g = 1.16 - 7.02 \times 10^{-4} \frac{T^2}{T + 1108} \quad (2.7.2)$$

and

$$\mu_o(T) = \mu_o \left( \frac{300}{T} \right)^{1.5} \quad (2.7.3)$$

# CHAPTER 3

## Measurements and Parameter Extraction

### 3.1 Introduction

In the previous chapter the proposed model was presented, and the model equations have several parameters. Some of these parameters are process and technology dependent, others are fitting parameters, but all of them play a major role in the determination of the device characteristics. Our purpose in this chapter is the determination of these parameter values, to best fit our devices. The first step to achieve this purpose is the development of an automated measurement procedure, the second step is to present an extraction algorithm.

Finally we develop an optimization algorithm to best fit the obtained data. This optimization algorithm and its implementation will be discussed in the next chapter.

### 3.2 Model Parameters

The model parameters, defined by the equations of the preceding chapter, are listed in Table 3.1:

**Table 3.1** Model parameters.

Name	Description	Default	Units
L	Channel length	20.0	$\mu\text{m}$
W	Channel width	20.0	$\mu\text{m}$
DEL	Lateral diffusion into channel from drain and source diffusion	0	$\mu\text{m}$
DEW	Total channel width reduction	0	$\mu\text{m}$
rj	Source-Drain junction depth	0.5	$\mu\text{m}$
Tox	Oxide thickness	20.0	nm
Dose	Ion implantation dose	0.0	$\text{cm}^{-2}$
D	Implanted layer depth at final step of fabrication	0.5	$\mu\text{m}$
nimp	Parameter to control the implanted layer shape	0.2	-
mimp	Non uniform doping dependent parameters knee factor	5	-
VTO <sup>(1)</sup>	Threshold voltage at $V_S=0$ , for a large channel length $L$	0	V
Gamma <sup>(2)</sup>	Body factor	0	$\text{V}^{1/2}$
PHI <sup>(3)</sup>	Surface potential at threshold	0	V
VFB	Flat-band voltage	0	V
Nsub	Effective substrate doping	1.0E+16	$1/\text{cm}^3$
Nsd	Effective source-drain doping	1.0E+19	$1/\text{cm}^3$
Pms <sup>(4)</sup>	Work function difference (if Pms is not given, it is computed internally using the parameter TPG)	0	V
TPG <sup>(4)</sup>	Gate material type (metal: TPG=0, P-poly: TPG=1, N-poly: TPG=-1)	-	-

**Table 3.1:** (continued).

Name	Description	Default	Units
Nox <sup>(4)</sup>	Effective number of the oxide charge density per unit area	1.0E+10	1/cm <sup>2</sup>
Dit	Interface trapped charge density (+ve: donor like, and -ve: acceptor like).	0	1/cm <sup>2</sup> - .eV
Muo	Low field mobility	650.0	cm <sup>2</sup> /V.- sec
THETA	Normal field mobility coefficient	0.05	1/V
vmax	Maximum drift velocity of carriers	1.0E+7	cm/sec
beta	Mobility lateral field knee factor	2.0	-
xsat	Saturation voltage knee factor	10.0	-
Ileak	Leakage current of the source-drain junctions	1.0E-12	A
AI	Impact ionization pre-exponential constant	1.0	1/V
BI	Impact ionization exponent constant	1.0E+6	V/cm
Rt	Series resistance of the source and drain terminals	10	Ohm
Ld <sup>(5)</sup>	DIBL characteristic length (if Ld is not given it is calculated internally)	0	μm
DSB	Bulk effect on the threshold voltage	3	-

(1) This parameter is optional. If it is not given, it is calculated internally using  $V_{tho} = V_{FB} + \phi_{si} + \gamma (\phi_{si})^{0.5}$ .

(2) This parameter is optional. If it is not given, it is calculated internally using  $\gamma = \frac{\sqrt{2 \cdot q \cdot \epsilon_s \cdot N_{sub}}}{C_{ox}}$ .

(3) This parameter is optional. If it is not given, it is calculated using

$$\phi_f = \phi_T \cdot \ln\left(\frac{N_{sub}}{n_i}\right).$$

(4) This parameter is discarded if either *VTO* or *VFB* is given.

(5) If this parameter is not given, it is calculated internally using

$$ld = \sqrt{\frac{\epsilon_s T_{ox} X_{dep}}{\epsilon_o \eta}}.$$

### 3.3 Measurement Procedure

In the next section we shall discuss the measurement requirements which is the first stage to get good parameter extraction scheme.

#### 3.3.1 Required equipment and samples

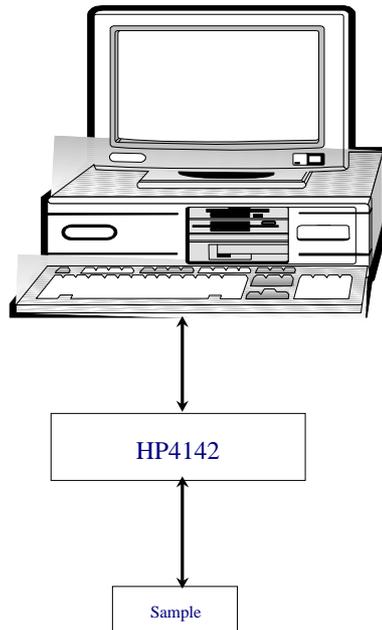
In order to carry the required automated measurements, the following equipment is required as shown in Fig. 3.1.

- IBM-PC with labVIEW<sup>1</sup> [42] (or HP VEE<sup>2</sup>) software
- A device analyzer (e.g. HP4142 Modular DC Source/Monitor)
- Probe Station (or suitable casing for device connections)
- Printer (optional)

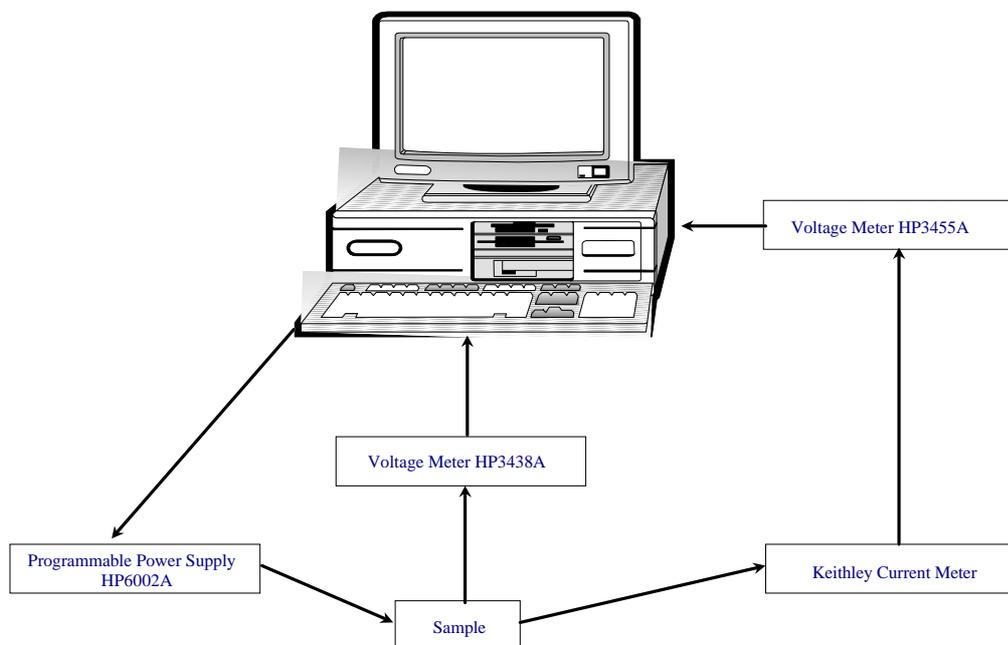
note that: we may replace the HP4142 by the system in Fig. 3.2

<sup>1</sup> Laboratory Virtual Instrument Engineering Workbench. © National Instruments Corporation.

<sup>2</sup> Hewlett Packard Visual Engineering Environment. © Hewlett Packard Corporation.



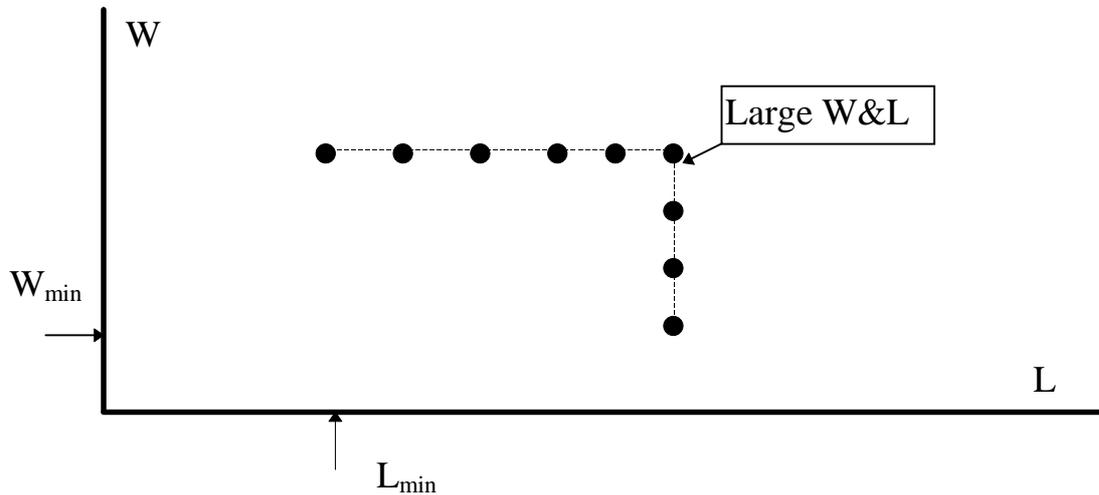
**Figure 3.1** Automated measurement using HP4142



**Figure 3.2** Automated measurement connections

*Devices needed for measurements*

One large size device and two sets of smaller size devices are needed, as shown in Fig. 3.3.

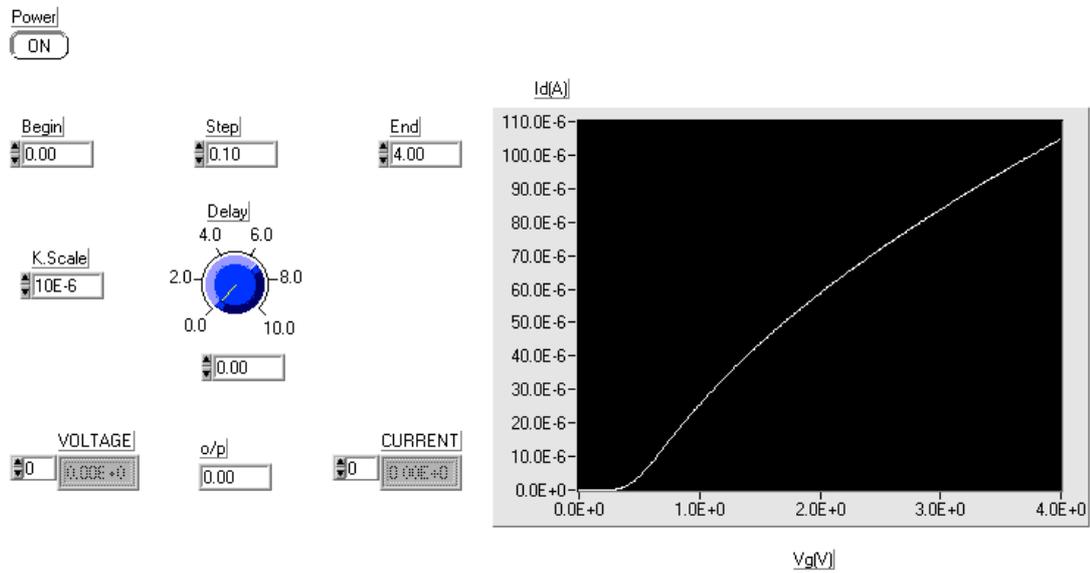


**Figure 3.3** *Distribution of device's sizes used for parameter extraction*

The large size device ( $W \& L \geq 10 \mu\text{m}$ ) is used to extract the parameters which are independent of short/narrow channel effects such as  $V_{T0}$ . One set of devices with fixed large channel width, but different channel lengths is used to extract parameters which are related to the short channel effects such as DIBL characteristic length ( $L_d$ ) and maximum drift velocity of carriers ( $v_{\text{max}}$ ). The other set of devices have a fixed, long channel length, but different channel widths. This set of devices is used to extract parameters which are related to narrow width effects.

**3.3.2 Measurement procedure**

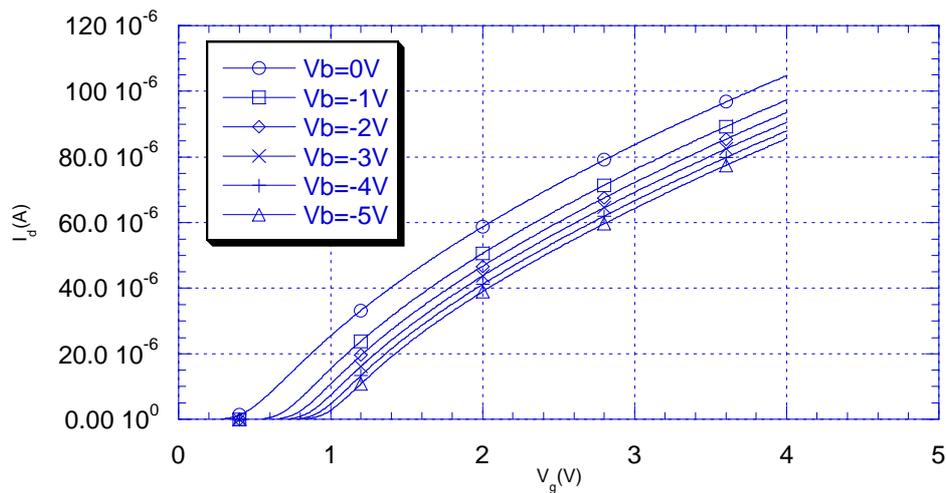
The measurement is done by an automated program written with the G language implemented in the LabView program [42]. The program has a simple user interface as shown in Fig. 3.4



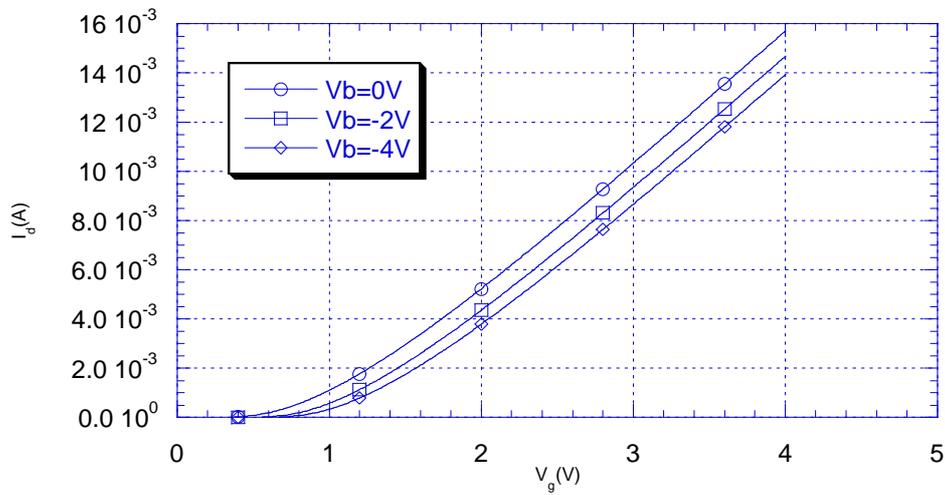
**Figure 3.4** User interface for the measurement program

### 3.3.3 Results

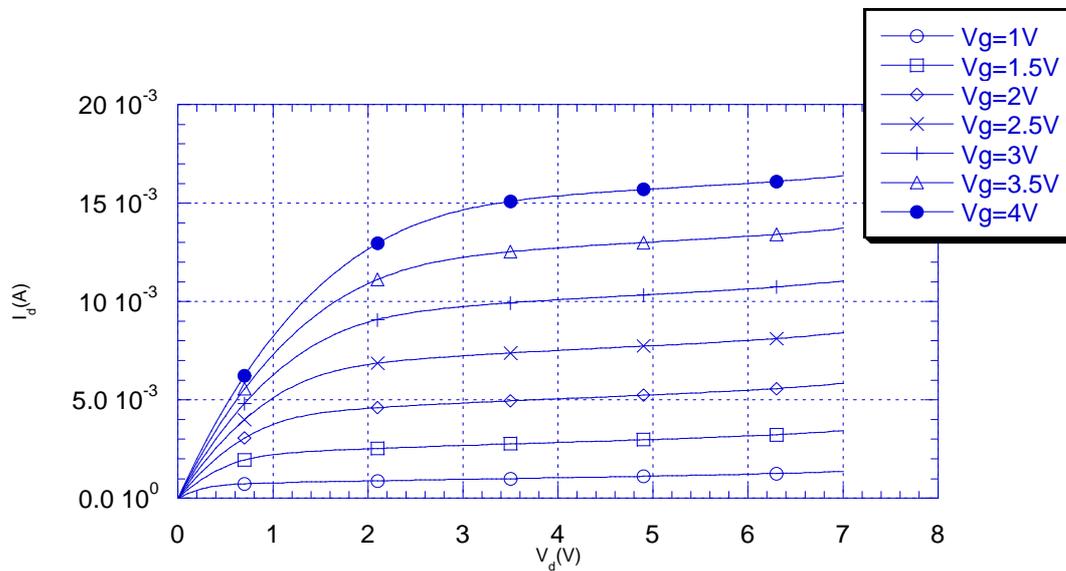
Now we represent the obtained results using the last procedure, and we shall apply the optimization algorithm for them, in the next chapter.



**Figure 3.5** Drain Current versus Gate voltage for low drain voltage (10mV) [ $W/L=50\mu/1.2\mu$ ]



**Figure 3.6** Drain Current versus Gate voltage for high drain voltage (5V) [ $W/L=50\mu/1.2\mu$ ]



**Figure 3.7** Drain Current versus Drain voltage for  $V_{bs}=0$  [ $W/L=50\mu/1.2\mu$ ]

## 3.4 Parameter extraction

By parameter extraction we mean: to find the model parameters described in Section 3.2 which best fit a given set of  $I$ - $V$  data. Parameter extraction is an important part of model development. Because without a good parameter extraction algorithm, even a perfect device model is useless.

### 3.4.1 Extraction Strategy

There are two different strategies for extracting parameters: the single device extraction strategy and group device extraction strategy [39].

#### Single device extraction strategy

In the single device extraction strategy, one uses the obtained data from a single device to extract the complete set of model parameters.

*Advantages:*

- i-* It may be used even if one transistor only is available
- ii-* This strategy can fit one device very well.

*Disadvantages:*

- i-* It may not fit other devices with different geometry.
- ii-* The single device extraction strategy can not guarantee that extracted parameters are physical. The only concern is to fit the given device.

In the next chapter we will consider this procedure (optimization).

#### The Group device extraction strategy

In the group device extraction strategy, we extract parameters using obtained data from different devices with different channel lengths, and fabricated by the same technology. This data is taken in the same operating region for each device.

*Advantages:*

- i- It can fit many devices with different geometries.
- ii- The obtained parameters are near to the physical ones.
- iii- The complete set of model parameters is effectively a characterization statement for a given IC processing technology. The electrical performance of all device structures fabricated by this technology should be accurately represented by this set of model parameters.

*Disadvantages:*

- i- It may not fit each device perfectly as in the Single device extraction strategy.
- ii- It can't work if only one transistor is available.

**3.4.2 Parameters extraction procedure**

In this section we shall use the second strategy, namely the group device extraction strategy. But since required sample dimensions are not available, we shall use MINIMOS [31] simulations instead of actual measurements. The device parameters were: the gate type was chosen to be *N*-poly, the oxide thickness is 20 nm, the bulk concentration is  $5E16 \text{ cm}^{-3}$ , a fixed oxide charge of  $1E10 \text{ cm}^{-2}$  is present, the junction depth computed by MINIMOS is approximately 0.5  $\mu\text{m}$ , the gate width is large  $W=50 \mu\text{m}$  and the gate lengths are 20 $\mu\text{m}$ , 6 $\mu\text{m}$ , 2 $\mu$ , 1.5 $\mu\text{m}$ , 1.2 $\mu\text{m}$  and 1 $\mu\text{m}$ .

**3.4.2.1 Theory**

Most parameters are obtained from the strong inversion region of operation, thus we use the simplified current expression in this region given by eq. (2.4.31). After the substitution with  $\mu_{\text{eff}}$ , also if we operate at a very low  $V_{DS}$  ( $V_{DS}=0.05 \text{ V}$ ), we may neglect the velocity saturation effects to get

$$I_D = \frac{W}{L_{\text{eff}}} C_{\text{ox}} \frac{\mu_o}{[(1 + \theta Q) + (\theta + \frac{W}{L_{\text{eff}}} \mu_o C_{\text{ox}} R_t) V]} (V) V_{ds} \quad (3.4.1)$$

where  $Q=2\gamma(\phi_{st}+V_s)^{1/2}$  and  $V=V_{gs}-V_{th}-V_{ds}/2$ .

The transconductance,  $g_m$ , is obtained by differentiating eq. (3.4.1) w.r.t.  $V_{gs}$  (or  $V$ ), such that

$$g_m = \frac{W}{L_{eff}} \mu_o C_{ox} \frac{I + \theta Q}{[(1 + \theta Q) + (\theta + \frac{W}{L_{eff}} \mu_o C_{ox} R_t) V]^2} V_{ds} \quad (3.4.2)$$

From equations (3.4.1) and (3.4.2), the ratio  $I_D/(g_m)^{1/2}$  takes the form

$$\frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{W \mu_o C_{ox} V_{ds}}{L_{eff} (I + \theta Q)}} V \quad (3.4.3)$$

It is seen that the ratio  $I_D/(g_m)^{1/2}$  does not depend on  $R_t$  and is directly proportional to  $V$ .

#### **A) Determination of threshold voltage ( $V_{T0}$ )**

From equation 3.4.3 it is clear that, when  $I_D/(g_m)^{1/2}$  is plotted against  $V_{gs}$ , we get a straight line with slope,  $m_1=(W\mu_o C_{ox} V_{ds}/(L_{eff}(I+\theta Q)))^{1/2}$  and the intercept on the  $V_{gs}$  axis equal  $(V_{th}+V_{DS}/2)$  so if we use large device length we obtain the threshold voltage for long channel device,  $V_{T0}$ . (See Fig. 3.8).

#### **B) Determination of $\Delta L$**

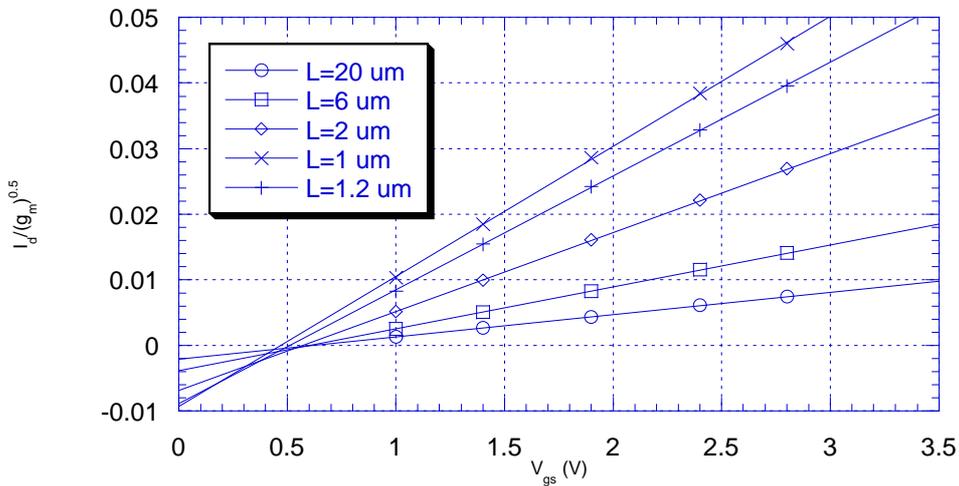
Consider the quantity:

$$\frac{I}{m_1^2} = \frac{(L - \Delta L)(I + \theta Q)}{W \mu_o C_{ox} V_{ds}} \quad (3.4.4)$$

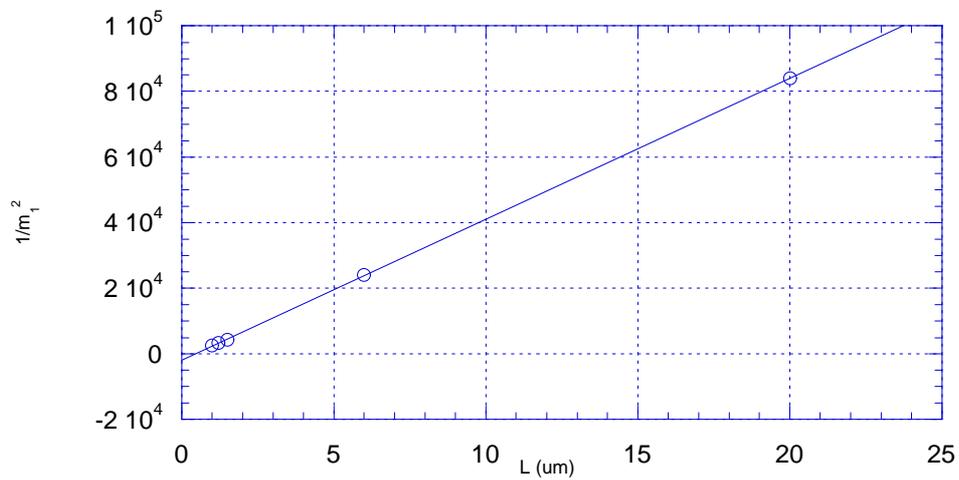
if it is plotted against the mask channel length  $L$ , the slope,  $m_2$ , of this straight line is equal to

$$m_2 = \frac{(I + \theta Q)}{W \mu_o C_{ox} V_{ds}} \quad (3.4.5)$$

and the intercept on the  $L$ -axis is  $\Delta L$ , allowing  $\Delta L$  to be determined. (See Fig. 3.9).



**Figure 3.8** The variation of  $I_D/g_m^{1/2}$  as a function of gate voltage for different channel lengths.



**Figure 3.9** The variation of  $1/m_1^2$  as a function of channel length.

### C) Determination of the parasitic resistance ( $R_t$ )

From eq. (3.4.1) the output resistance,  $R_o$ , defined by  $V_{ds}/I_D$  is equal to

$$R_o = R_t + (L - \Delta L) \frac{I + \theta(V + Q)}{W \mu_o C_{ox} V} \quad (3.4.6)$$

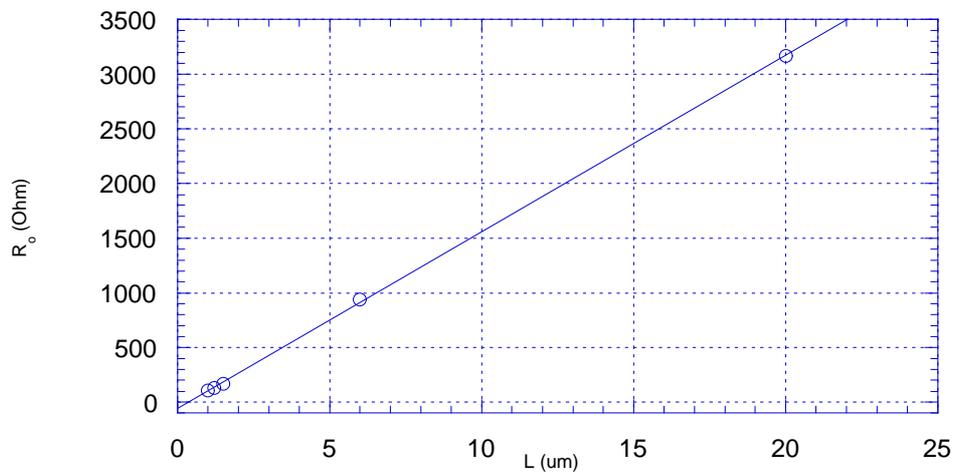
When  $R_o$  is plotted against the mask channel length  $L$ , for a given value of  $V$ , we get a straight line, the slope of such straight line is

$$m_3 = \frac{I + \theta(V + Q)}{W \mu_o C_{ox} V} \quad (3.4.7)$$

and from the intercept we can determine the parasitic series resistance  $R_t$  as :

$$R_t = \text{Intercept} + \Delta L * m_3 \quad (3.4.8)$$

(See Fig. 3.10).



**Figure 3.10** The variation of  $R_o$  as a function of the mask channel length  $L$

### D) Determination of low field mobility parameters ( $\mu_o$ and $\theta$ )

Dividing equations (3.4.5) and (3.4.7), we get the parameter  $\theta$  as

$$\theta = \frac{\frac{m_2 V_{ds}}{m_3 V} - I}{Q - \frac{m_2 V_{ds}}{m_3 V} (V + Q)} \quad (3.4.9)$$

then using eq. (3.4.5) we can determine  $\mu_o$  as

$$\mu_o = \frac{1 + \theta Q}{W C_{ox} V_{ds} m_2} \quad (3.4.10)$$

### ***E) Determination of high field mobility parameters ( $v_{max}$ )***

The effective mobility  $\mu_{eff}'$  given by eq. (2.4.32) can be written as

$$\mu_{eff}' = \frac{\left(\frac{\mu_g}{D}\right)}{1 + \frac{W}{L_{eff}} \left(\frac{\mu_g}{D}\right) C_{ox} R_t V} \quad (3.4.11)$$

where

$$D = \left[ 1 + \left( \frac{\mu_g V_{DS}}{L_{eff} v_{max}} \right)^m \right]^{1/m} \quad (3.4.12)$$

$$\mu_g = \frac{\mu_o}{1 + \theta(Q + V)} \quad (3.4.13)$$

The factor (D) represents the velocity saturation effect (refer to Section 2.4.2). Thus if the effective mobility is found in strong inversion at a given value of  $V$ , using the strong inversion approximated current equation at high  $V_{DS}$  (but still in the linear region),  $\mu_h$ , and knowing  $\mu_o$  and  $\theta$  i.e. knowing  $\mu_g$  at the specified  $V$ , and  $R_t$ , we can find  $v_{max}$  using

$$D = \frac{\mu_g \left( 1 - \mu_h \frac{W}{L_{eff}} C_{ox} R_t V \right)}{\mu_h} \quad (3.4.14)$$

and eq. (3.4.12).

### ***F) Determination of the characteristic length of barrier lowering ( $L_d$ )***

Referring to Section 2.4.3, we can find the parameter  $L_d$  by measuring the slope of  $\Delta V_{th}$  versus  $L_{eff}$ , where  $\Delta V_{th}$  is drawn on logarithmic scale. (See Fig. 2.7 and Fig. 3.11).

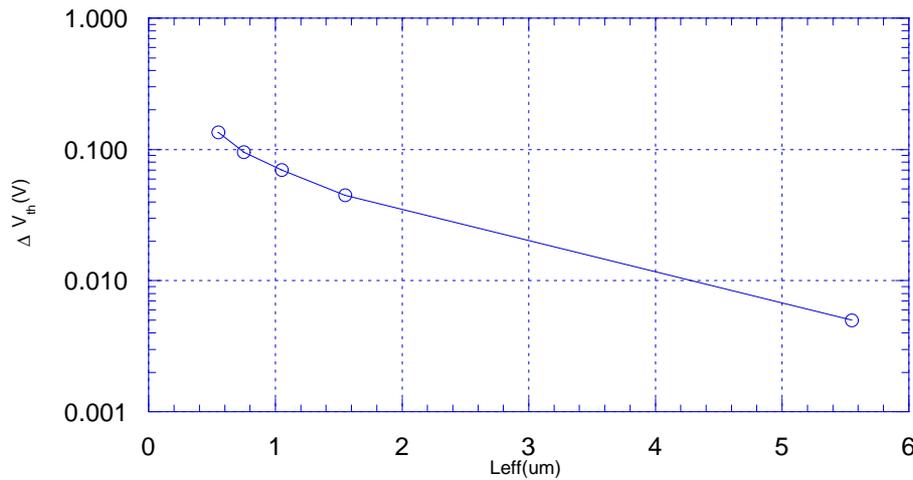
### G) Determination of the Impact ionization parameters (AI and BI)

We may find these parameters, by referring to eq. 2.4.40, this curve is bell shape, so if we find the point at which maximum bulk current occur ( $V_{gsm}, I_{bm}$ ) we find BI from the relation

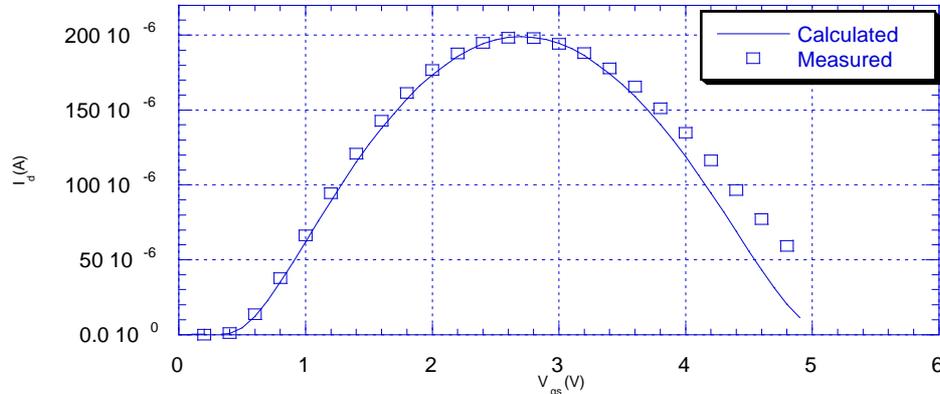
$$BI = \left( \frac{g_{mm}(V_{ds} - V_{gsm} + V_{th})}{I_{dm}} - 1 \right) (V_{ds} - V_{gsm} + V_{th}) \quad (3.4.15)$$

$$AI = \frac{I_{bm}}{I_{dm}(V_{ds} - V_{gsm} + V_{th}) \exp\left(-\frac{BI}{V_{ds} - V_{gsm} + V_{th}}\right)} \quad (3.4.16)$$

where  $g_{mm}$  and  $I_{dm}$  are the transconductance and drain current at this maximum point respectively. (See Fig. 3.12).



**Figure 3.11**  $\Delta V_{th}$  as a function of the effective channel length.



**Figure 3.12** Determination of Impact ionization parameters

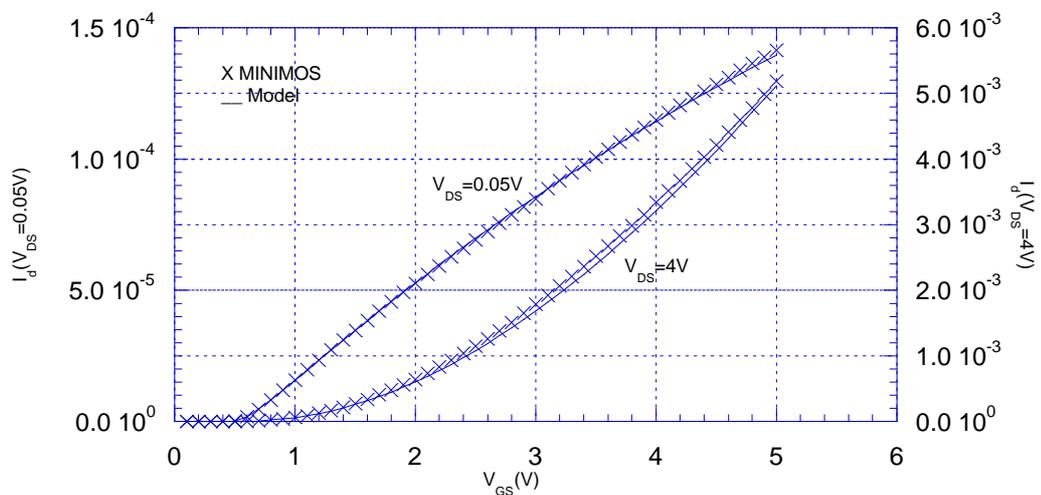
### 3.4.2.2 Extraction Results

From the above, we get the parameters' values shown in Table 3.2. Also we have made small manual optimization to the mobility parameters to get best fit to the measured data.

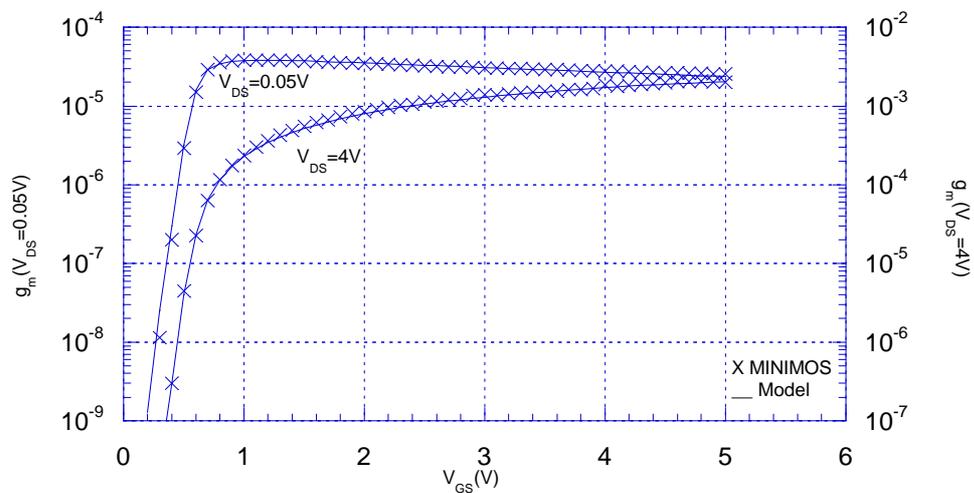
**Table 3.2** Obtained parameters

Parameter	Value	After Optimization	Unit
VTo	0.58	0.58	V
DEL	0.45	0.45	$\mu\text{m}$
Rt	10	10	Ohm
Muo	610	670	$\text{cm}^2/\text{V.s ec}$
THETA	0.097	0.091	1/V
vmax	7e6	1.2e7	cm/sec
Ld	0.155	0.155	$\mu\text{m}$
AI	1.148e-6	1.148e-6	1/V
BI	4.185e4	4.185e4	V/cm

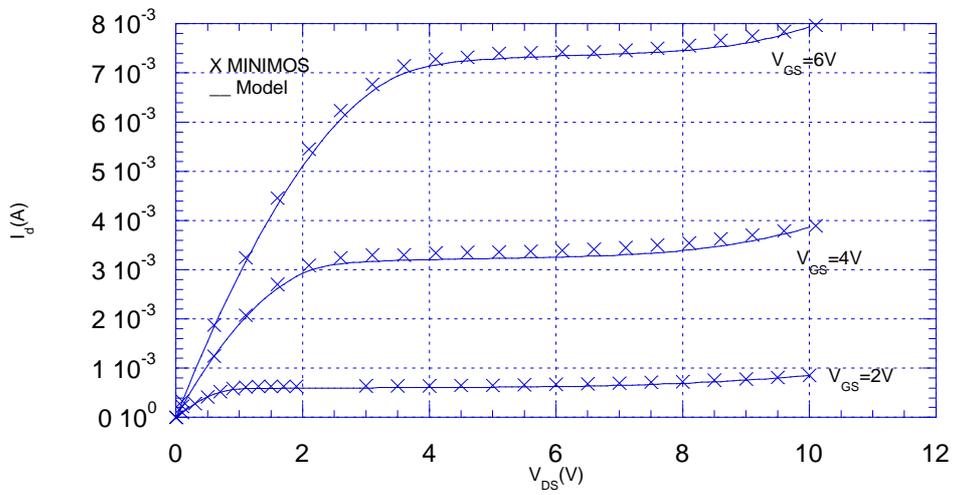
Now to validate the used extraction method, we use the extracted parameters for two different channel lengths  $6\ \mu\text{m}$  (long channel), and  $1\ \mu\text{m}$  (short channel), and we compare the obtained results with the MINIMOS results. See Figures from 3.13 to 3.18 for comparison, from these figures we note the good agreement between the simulated results and the experimental results, for both short and long channel transistors.



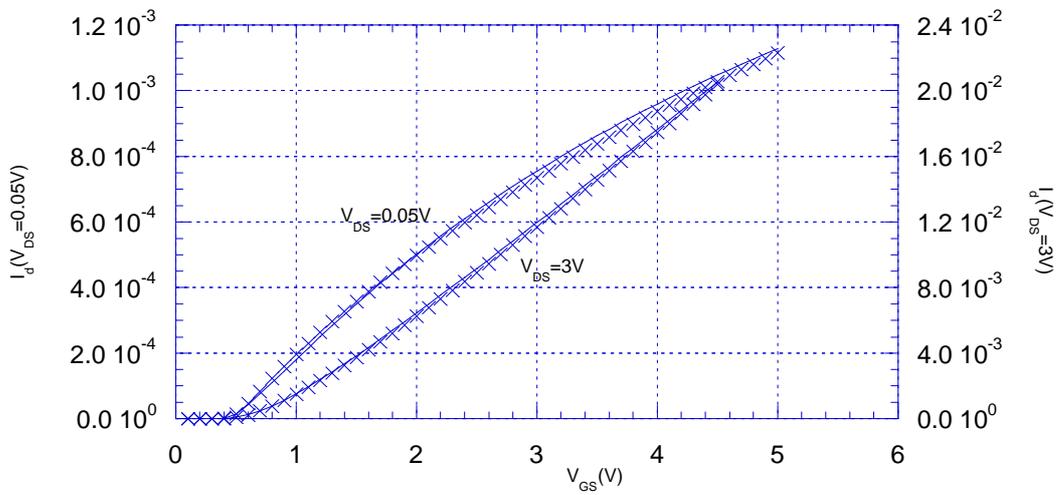
**Figure 3.13** Drain current versus gate voltage for long device ( $6\ \mu\text{m}$ )



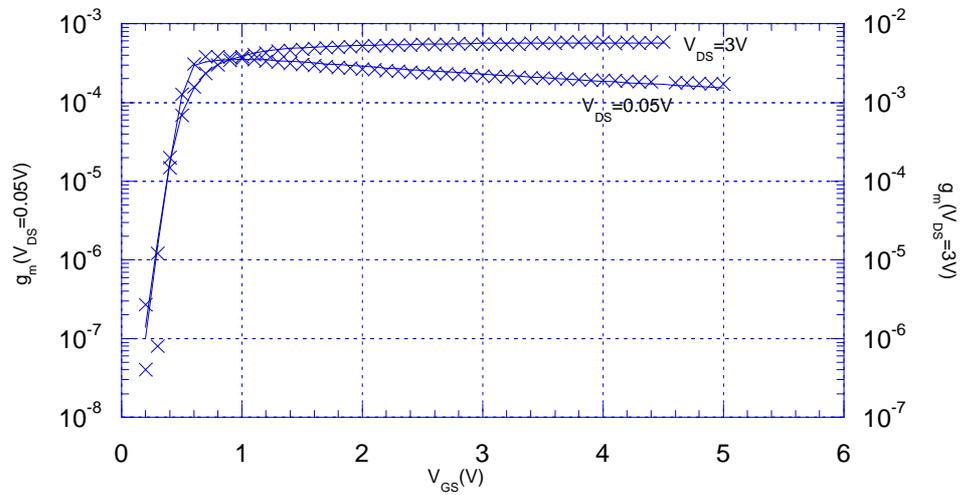
**Figure 3.14** Transconductance versus gate voltage for long device ( $6\ \mu\text{m}$ )



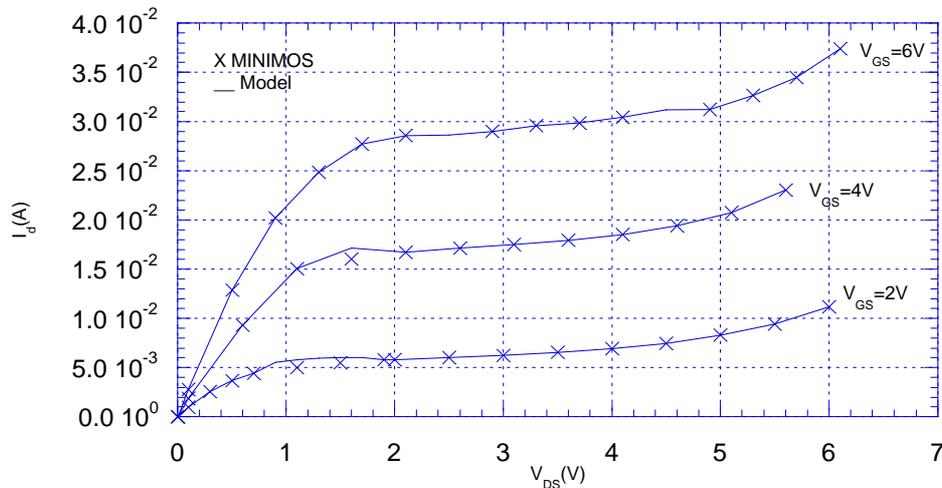
**Figure 3.15** Drain current versus drain voltage for long device ( $6\mu\text{m}$ )



**Figure 3.16** Drain current versus gate voltage for short device ( $1\mu\text{m}$ )



**Figure 3.17** Transconductance versus gate voltage for short device ( $1\mu\text{m}$ )



**Figure 3.18** Drain current versus drain voltage for short device ( $1\mu\text{m}$ )



# CHAPTER 4

## Optimization Algorithm and Results

### 4.1 Introduction

An optimization problem begins with a set of independent variables and/or parameters, a set of dependent variables, and the existing or simulated functional relationship between the two sets. This relation can have various level of complexity and is inherently nonlinear in nature. In general, its evaluation consists of the execution of some underlying simulation tools that involve highly complex solution techniques which are computationally expensive. Furthermore, they are not suited for analytical manipulation and the use of numerical approximation is normally required. Typically, they have a continuous and well-behaved functional behavior. These characteristics influence the choice of the appropriate solution algorithm for any particular task.

It is clearly desirable to have a standard model formulation suitable for the description of the diverse tasks algorithms. In mathematical terms such an expression takes the form:

$$Y=f(X,P) \tag{4.1.1}$$

where

$$Y = [y_1, y_2, \dots, y_q] \tag{4.1.2}$$

$$X = [x_1, x_2, \dots, x_m] \tag{4.1.3}$$

$$P = [p_1, p_2, \dots, p_n] \tag{4.1.4}$$

are vectors of  $q$  model outputs,  $m$  independent variables and  $n$  model parameters respectively.  $f$  can also be formulated in terms of the individual output functions as:

$$f = [f_1, f_2, \dots, f_q] \quad (4.1.5)$$

where each

$$y_i = f_i(X, P) \quad (4.1.6)$$

represent the model evaluation that relates the input and parameter vectors to the  $i$ -th response.

In the rest of this chapter the used algorithm is presented and discussed. It is a nonlinear least-squares optimization module which forms the nucleus of our work.

## 4.2 Nonlinear Least Squares Optimization

Given a certain CAD model and a set of observations (i.e. data) that relate the model independent variables ( $X$ ) to its calculated responses ( $Y$ ), the problem of optimization consists of finding the model parameter vector ( $P$ ) that will result in the best possible fit between measurements and model predictions. In the present work, the weighted *sum of squares* ( $F$ ) is used as a measure of the accuracy of fit:

$$F = \sum_{j=1}^q \sum_{i=1}^m w_{ji} r_{ji}^2 \quad (4.2.1)$$

where  $w_{ji}$  and  $r_{ji}$  are the weight and the residual for the  $j$ -th response at the  $i$ -th data point respectively. The residual is defined as the relative error at that data point:

$$r_{ji} = \frac{f_j(X_i, P) - y_{ji}^{\text{exp}}}{y_{ji}^{\text{exp}}} \quad (4.2.2)$$

where  $y_{ji}^{\text{exp}}$  is the measured  $j$ -th response at  $X_i$ . The weight is a user-defined positive value that increases or decreases the significance of a data point in the overall fit. This can be related to the user desire to achieve higher accuracy for a certain input or output variable range or to the prior knowledge about the expected accuracy of the measurements. It is noted that this definition of the objective is a variation on the *Chi-Square* fitting

criterion where the standard deviation of each measurement data point is used in the formulation.

By defining  $\mathbf{R}$ , a vector of the  $n \times q$  residuals, (4.2.1) can be written as:

$$\mathbf{F} = \mathbf{R}^T \mathbf{W} \mathbf{R} \quad (4.2.3)$$

where  $\mathbf{W}$  is a  $nq \times nq$  diagonal matrix whose elements  $W_{ii}$  are the weights  $w_i$ . The solution of the nonlinear least squares problem reduces to minimizing (4.2.1). In general, the nonlinearity of CAD models dictates the use of gradient based iterative methods. The present implementation is based on the Levenberg-Marquardt (LM) algorithm [43-45] which has become the standard of nonlinear least squares routines [46]. The Levenberg-Marquardt method combines the inherent stability of steepest descent with the quadratic convergence rate of the Gauss-Newton method as described in the next section.

#### 4.2.1 Algorithm Description

A Taylor series expansion of (4.2.1) around a nominal point  $\mathbf{P}_o$  can be written as:

$$F(\mathbf{P}_o + \Delta \mathbf{P}) = F(\mathbf{P}_o) + \mathbf{g}^T \Delta \mathbf{P} + \frac{1}{2} \Delta \mathbf{P}^T \mathbf{H} \Delta \mathbf{P} + O(\|\Delta \mathbf{P}\|^3) \quad (4.2.4)$$

where

$$\mathbf{g} = \left[ \frac{\partial F}{\partial p_1}, \frac{\partial F}{\partial p_2}, \dots, \frac{\partial F}{\partial p_m} \right] \quad (4.2.5)$$

is the gradient of the objective function, and  $\mathbf{H}$  is an  $m \times m$  matrix of second derivatives called the Hessian matrix whose elements are given by:

$$H_{ij} = \frac{\partial^2 F}{\partial p_i \partial p_j} \quad (4.2.6)$$

An intuitive iterative solution scheme consists of taking a step in the negative gradient direction:

$$\Delta P = -g \quad (4.2.7)$$

When the size of the step ( $\alpha_k$ ) is chosen appropriately, a monotonic decrease in the objective function is ensured. At each iteration, the size of the step can be determined via a line search along the negative gradient direction using a one-dimensional optimization technique (e.g. Brent's parabolic). The new values of the parameters are then calculated as:

$$P_{k+1} = P_k + \alpha_k \Delta P_k \quad (4.2.8)$$

This procedure is called steepest descent. It is a reliable and inherently stable method that will always lead to a minimum of  $F$ . Its disadvantage is that the step often has to be so small that it results in a very slow convergence especially as the minimum is approached.

An alternative solution technique is the Gauss-Newton method which is based on the premise that a quadratic approximation is an accurate representation of  $F$  at  $P_0$ . In this case, the  $O(\|\Delta P\|^3)$  terms in (2.10) are dropped, and the necessary condition for the minimum of  $F$ , namely that the gradient must be zero, can be written as:

$$g + 2H \Delta P = 0 \quad (4.2.9)$$

which yields the following equation for  $\Delta P$ :

$$\Delta P = -\frac{1}{2} H^{-1} g \quad (4.2.10)$$

In the case of the least-squares objective  $F$ , the elements of the gradient and the Hessian matrix can be expressed as:

$$g_j = \frac{\partial F}{\partial p_j} = 2 \sum_{i=1}^m w_i r_i \frac{\partial r_i}{\partial p_j} \quad (4.2.11)$$

and

$$H_{jk} = \frac{\partial^2 F}{\partial p_j \partial p_k} = 2 \sum_{i=1}^m w_i \left( \frac{\partial r_i}{\partial p_j} \frac{\partial r_i}{\partial p_k} + r_i \frac{\partial^2 r_i}{\partial p_j \partial p_k} \right) \quad (4.2.12)$$

For sufficiently small residuals, the second term in (4.2.12) can be neglected and the elements of the Hessian matrix are approximated as:

$$H_{jk} = \frac{\partial^2 F}{\partial p_j \partial p_k} \approx 2 \sum_{i=1}^n w_i \left( \frac{\partial r_i}{\partial p_j} \frac{\partial r_i}{\partial p_k} \right) \quad (4.2.13)$$

By introducing the  $n \times m$  Jacobian matrix  $\mathbf{J}$  whose elements are the partial derivative of the individual residual with respect to the parameters:

$$J_{ij} = \frac{\partial r_i}{\partial p_j} \quad (4.2.14)$$

(4.2.11) and (4.2.13) can be written in vector form as:

$$\mathbf{g} = 2\mathbf{J}^T \mathbf{W} \mathbf{R} \quad (4.2.15)$$

$$\mathbf{H} \approx 2\mathbf{J}^T \mathbf{W} \mathbf{J} \quad (4.2.16)$$

The above equations are the basis of the Gauss-Newton iteration scheme:

$$\Delta \mathbf{P} = -\frac{1}{2} (\mathbf{J}^T \mathbf{W} \mathbf{J})^{-1} \mathbf{J}^T \mathbf{W} \mathbf{R} \quad (4.2.17)$$

$$\mathbf{P}_{k+1} = \mathbf{P}_k - \frac{1}{2} (\mathbf{J}_k^T \mathbf{W} \mathbf{J}_k)^{-1} \mathbf{J}_k^T \mathbf{W} \mathbf{R}_k \quad (4.2.18)$$

Given an initial guess sufficiently close to the solution, the Gauss-Newton method has a quadratic convergence rate. However, a poor starting vector could cause the method to diverge due to the size of the neglected second term in (4.2.12). Furthermore, the method always fails when the Hessian matrix becomes singular or ill-conditioned. Several modifications have been proposed to the basic scheme to ensure convergence [47-48].

In the Levenberg-Marquardt method, the approximate Hessian matrix is replaced by:

$$\mathbf{J}^T \mathbf{W} \mathbf{J} + \lambda \mathbf{D} \quad (4.2.19)$$

and the iteration scheme becomes:

$$\mathbf{P}_{k+1} = \mathbf{P}_k - (\mathbf{J}_k^T \mathbf{W} \mathbf{J}_k + \lambda \mathbf{D})^{-1} \mathbf{J}_k^T \mathbf{W} \mathbf{R}_k \quad (4.2.20)$$

where  $\lambda$  is a conditioning factor and  $D$  is a diagonal matrix with entries equal to the diagonal elements of  $J^T W J$ . The essence of the *Levenberg-Marquardt compromise* is that the step direction is intermediate between the steepest descent and the Gauss-Newton directions. As  $\lambda \rightarrow 0$  the search direction approaches the Gauss-Newton direction. Alternatively when  $\lambda \rightarrow \infty$ , the method reduces to a steepest descent minimum search. A simple strategy to update the values of  $\lambda$  consists of decreasing its value when an iteration is successful in reducing the sum of squares fit criterion, and increasing it when the iteration fails:

$$\begin{aligned} \text{if } F_{k+1} < F_k \quad &\rightarrow \quad \lambda_{k+1} = \lambda_k / \text{factor} \\ \text{else } \lambda_{k+1} &= \lambda_k * \text{factor} \end{aligned} \quad (4.2.21)$$

where *factor* is a user defined parameter (default of 5).

### 4.2.2 Calculation of the Jacobian Matrix

The calculation of the elements of the jacobian matrix requires the values of the derivatives of the model function at the input data points. The used model functions are generally smooth but their analytical derivatives are unavailable. Numerical differentiation techniques are used to approximate the derivative using forward differences formula:

$$J_{ij} = \frac{r_i(P_k + h_j) - r_i(P_k)}{h_j} \quad (4.2.22)$$

where  $h_j$  represents a small increment.

It was proven that the use of numerical approximation in the Levenberg-Marquardt algorithm does not jeopardize its convergence properties [45].

### 4.2.3 Parameters Constraints

To avoid deviations outside the expected range of the parameters during the initial stages of the solution, linear interval inequality constraints of the form:

$$\mathbf{L} \leq \mathbf{P} \leq \mathbf{U} \quad (4.2.23)$$

are enforced on the parameters. In the above equation  $\mathbf{L}$  and  $\mathbf{U}$  are vectors of lower and upper bounds on each of the model parameters. The constraints are incorporated into the Levenberg-Marquardt algorithm using a simple technique based on the concept of active constraints. A constraint becomes active if it is violated when the parameters are updated (i.e. if  $p_i < l_i$  or if  $p_i > u_i$ ). The parameters corresponding to the set of active constraints are not allowed to change by enforcing that  $\Delta P_i = 0$ . This is accomplished by removing the appropriate equations from the linear system of (4.2.20).

#### 4.2.4 Termination Criteria

The iterations are continued until convergence which is denoted by either a small relative change in the sum of squares error (F), or by a small change in each parameter value relative to the previous iteration values. Other termination criteria are indicative of error conditions that occur when the optimization problem is ill posed such as when:

- The number of iterations exceeds a maximum number ( $N_{iter} > N_{max}$ )
- The conditioning factor exceeds a preset maximum value ( $\lambda > \lambda_{max}$ ). In this case, the algorithm is failing to move forward even though the method of steepest descent is used.
- The norm of the gradient is very small. This indicates the failure to find a search direction:  $\|g\| < \epsilon$ .

As in other optimization problems, the convergence to a solution does not guarantee that the global minimum of F has been reached.

### 4.3 Results

To validate our system, measurement programs, model functions and optimization program we carry our measurements and characterization on sample transistor with the following parameters gate mask length=1.2  $\mu\text{m}$ , gate mask width=100  $\mu\text{m}$ , gate oxide thickness=28 nm, and bulk doping= $5\text{E}16 \text{ cm}^{-3}$ . We adopt the procedure explained in Section 3.4.2.1(G) to determine the impact ionization parameters, the low field mobility

parameters, threshold voltage, and series resistance are obtained by applying the developed program for the least squares error discussed in this chapter to the drain current vs. gate voltage at low drain voltage (10 mV), finally the high field mobility parameters are obtained from the drain current vs. gate voltage at high drain voltage (5V)

#### 4.3.1 Obtained parameters

We present here the obtained parameters after optimization procedure, which will be used beside the given technological parameters mentioned above in our simulation.

**Table 4.1** *Obtained parameters*

Parameter	Value	Unit
VTo	0.349	V
DEL	0.052	$\mu\text{m}$
Rt	24	Ohm
Muo	532	$\text{cm}^2/\text{V.s ec}$
THETA	0.093	1/V
vmax	7e6	cm/sec
AI	6.693E-7	1/V
BI	4.911E5	V/cm

## 4.4 Comparison with simulation results

Comparison between the measured data, and the obtained results from our model simulations, is carried using the same set of the extracted parameters.

Figs. 4.1,4.2 show the comparison of the  $I_D$ - $V_{GS}$  characteristics and the corresponding transconductances, on both linear and logarithmic scales, of the obtained measured data with those of our model at a small  $V_{DS}$  ( $V_{DS}=0.01$

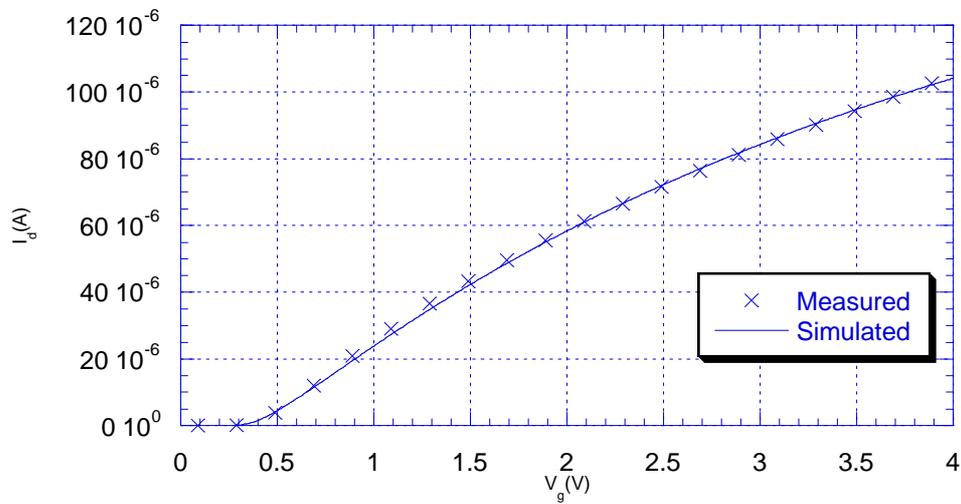
V). Continuity of the current model and its first derivative from subthreshold to strong inversion is clearly demonstrated.

Figs. 4.3,4.4 shows the same results but at a high  $V_{DS}$ . Effect of Longitudinal field on the mobility together with the series resistance effect are adequately modeled as shown in Figures.

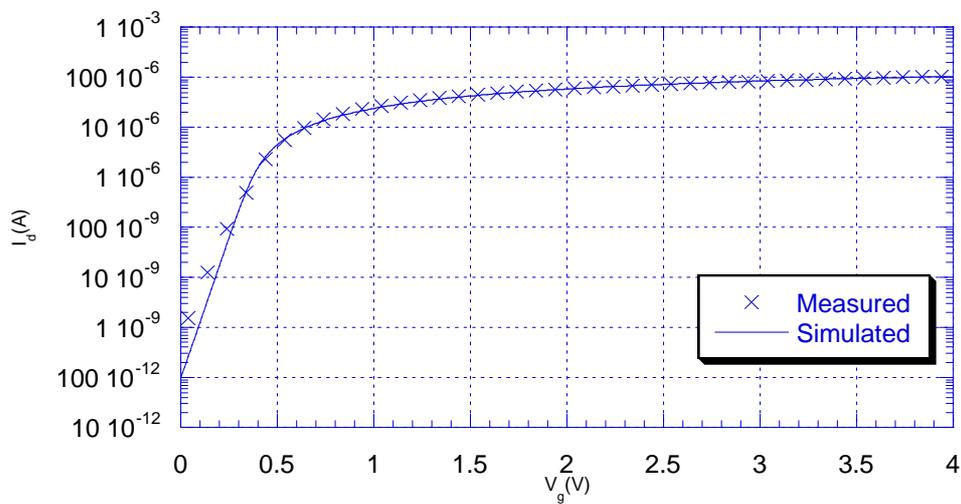
Fig. 4.5 demonstrates the effect of  $V_{DS}$  on the threshold voltage (DIBL). The ability of the model to predict the dc characteristics in the vicinity of threshold and in the subthreshold region under different drain bias for short channel transistors is demonstrated by the results of this figure.

Fig. 4.6 shows the  $I_D$ - $V_{DS}$  characteristics for four values of  $V_{GS}$  ( $V_{GS}=1$  V, 2 V, 3V, and 4 V). Continuity of the model from linear to saturation operation is clearly demonstrated. The modeling of saturation region characteristics is more clearly shown by the corresponding output drain conductance given in Fig. 4.7. From the results it is clear that the model is shown to fit the obtained data in all operating regions.

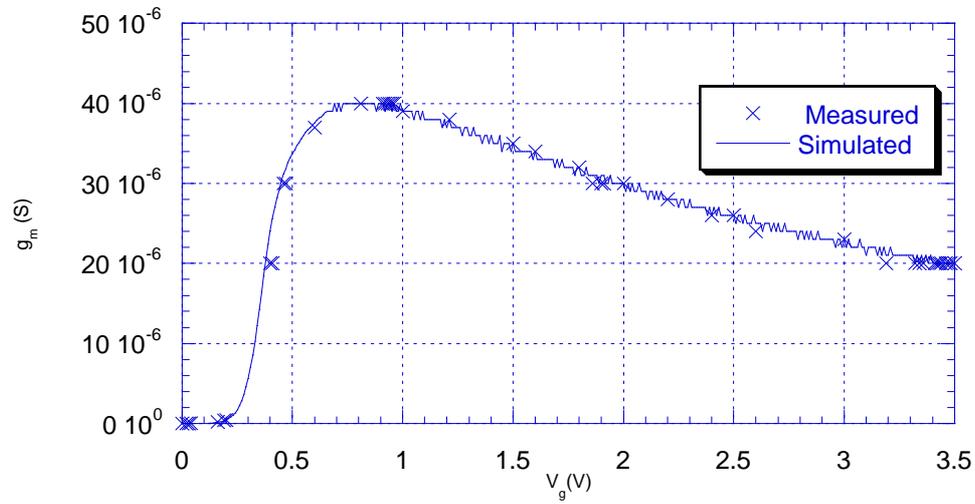
An additional test suggested by Tsvividis and Suyama [12] is to compare measured and modeled  $g_m/I_D$  versus  $V_{GS}$ . They point out that some of the commonly used models show an anomalous spike as the drain current crosses the boundary between weak and strong inversion. We have performed this test and the result is shown in Fig. 4.8. The exponential relationship between  $I_D$  and  $V_{GS}$  results in a constant  $g_m/I_D$  in the subthreshold region. No anomalous spike is observed at the transition to strong inversion because in our model  $g_m$  is continuous across the boundary.



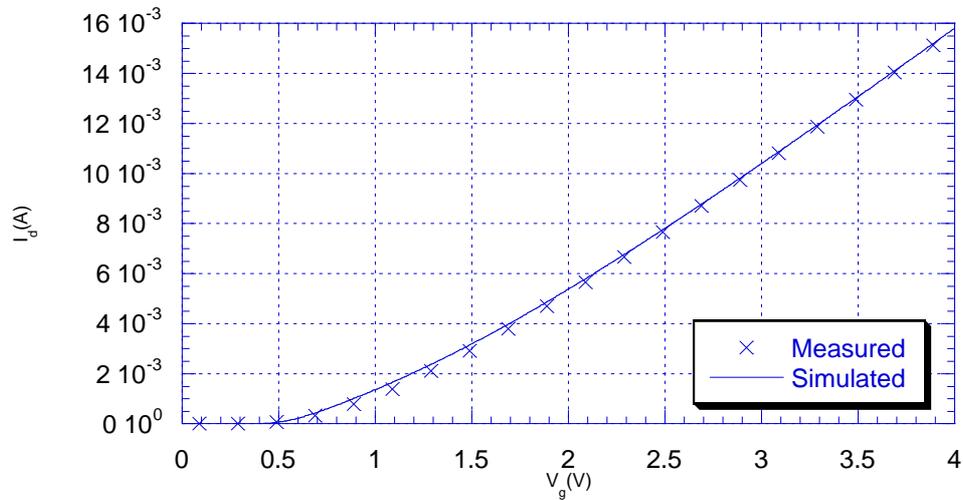
**Figure 4.1.a** Drain current versus gate voltage for drain voltage=10mV [Linear Scale]



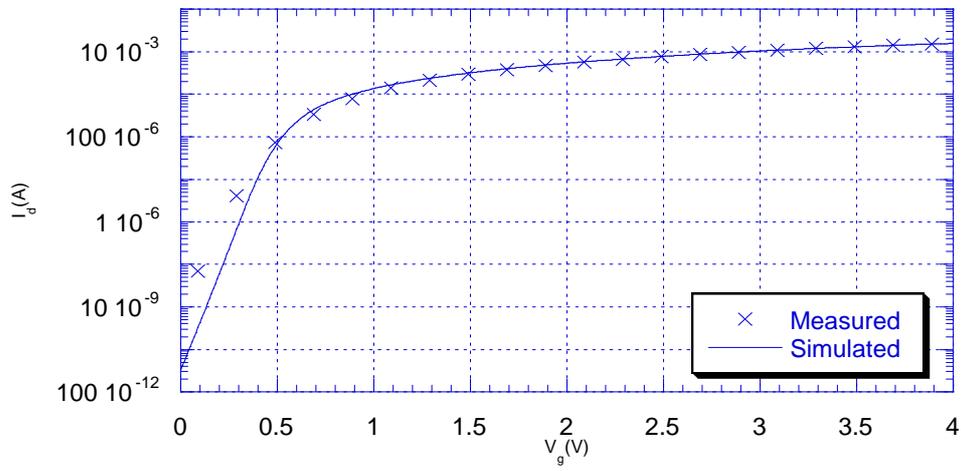
**Figure 4.1.b** Drain current versus gate voltage for drain voltage=10mV [Log Scale]



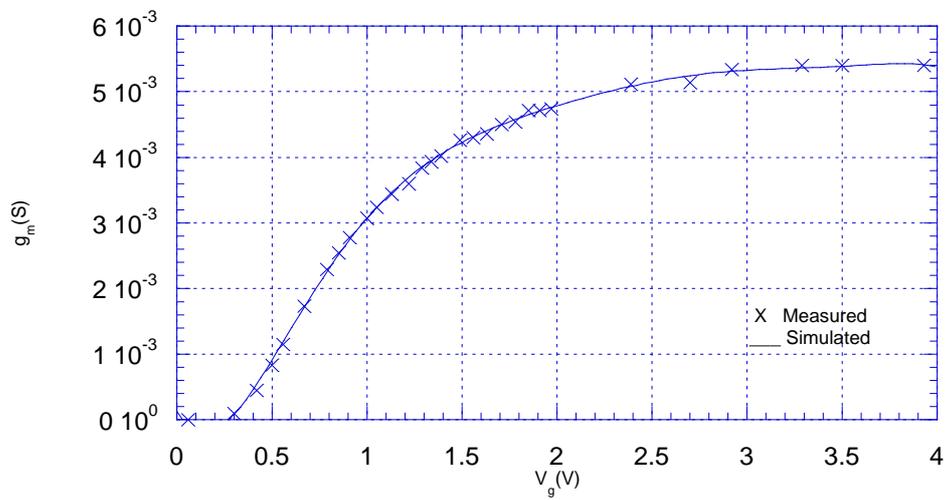
**Figure 4.2** Transconductance versus gate voltage for drain voltage=10mV



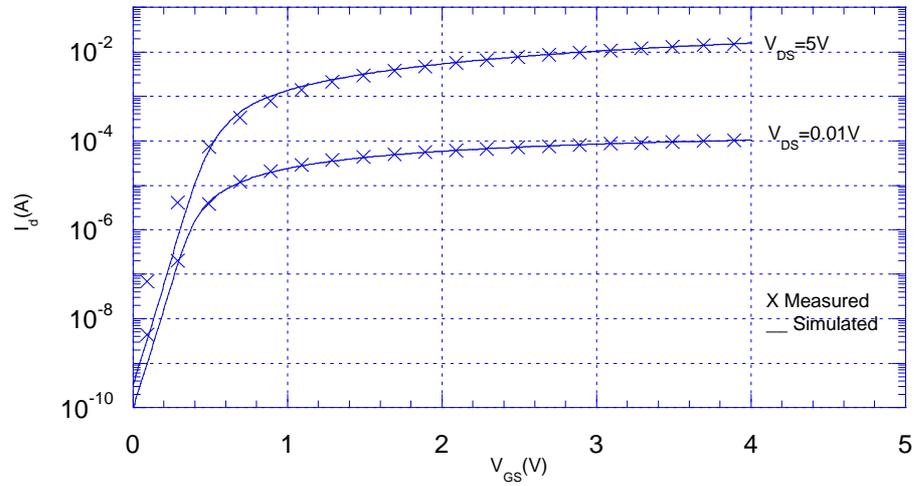
**Figure 4.3.a** Drain current versus gate voltage for drain voltage=5V



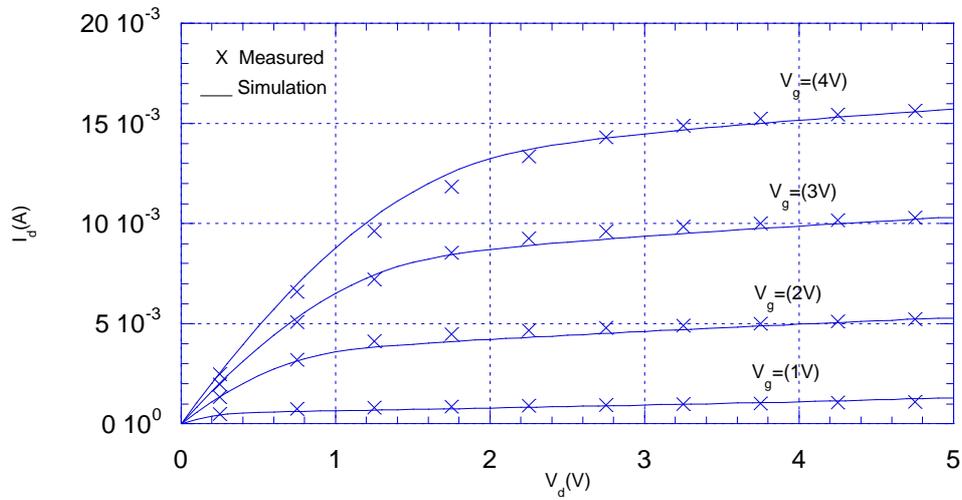
**Figure 4.3.b** Drain current versus gate voltage for drain voltage=5V



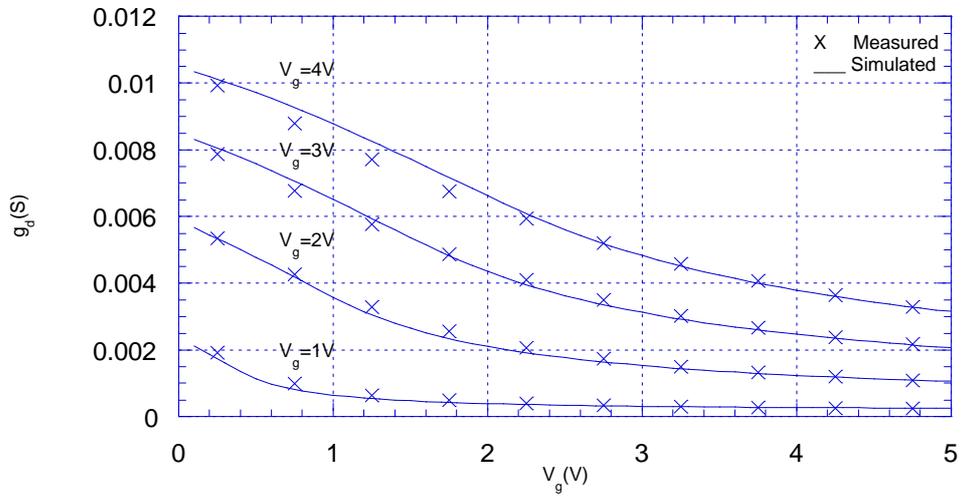
**Figure 4.4** Transconductance versus gate voltage for drain voltage=5V



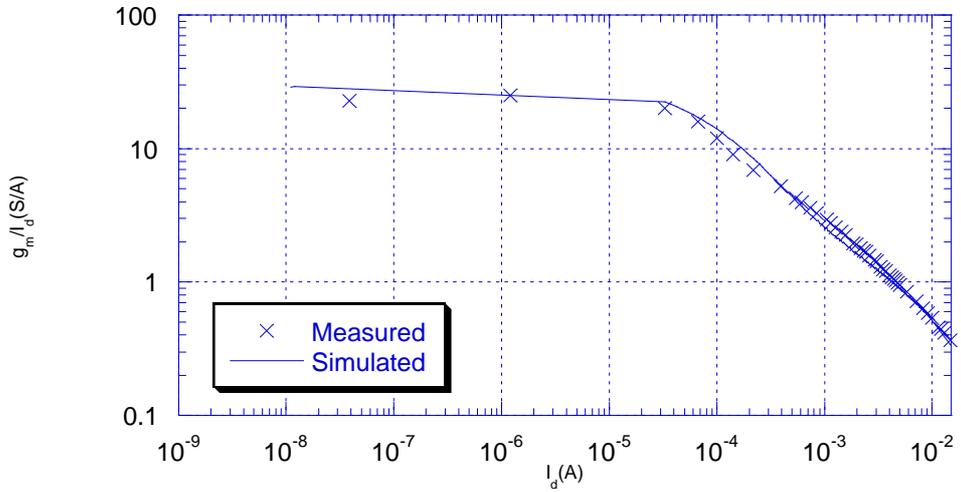
**Figure 4.5** Drain current versus gate voltage for different drain voltages



**Figure 4.6** Drain current versus drain voltage for different gate voltages



**Figure 4.7** Output conductance versus drain voltage for different gate voltages



**Figure 4.8**  $g_m/I_d$  versus Drain current

## 4.5 Other Models

Table 4.2 shows a comparison of the MOS Level (2) (SPICE) [49], BSIM [50], and aMOS [51] models with the proposed model. The table shows that the proposed model has a small number of parameters compared to the BSIM and aMOS models, while maintaining a good accuracy for the drain current and small signal parameters

## 4.6 Conclusion

The model presented in this thesis is a physical, scaleable and efficient model for VLSI analog/digital circuit simulation. It has built-in dependencies on geometry and process parameters. Small-size and non-uniform doping effects which are important in today's IC devices are built in the model. It also has a relatively small number of parameters which can be easily extracted and optimized. The continuity of the model reduces the number of iterations and CPU time during circuit simulation. The automated measurements programs presented in this work, make the measurements procedure more easier and accurate, since we adopted a good measurement technique as the first step to obtain good extracted parameters. Also the use of Levenberg-Marqudet algorithm which has become the standard of nonlinear least squares routines is used to develop parameters optimization program, which give us more accuracy to our extracted parameters. The developed program can be used in any other environment require least squares error method for optimization.

**Table 4.2.** Comparison between SPICE Level (2) model, BSIM model, aMOS model, and this work.

<i>Model</i>	<i>Developers</i>	<i>No. Of Parameters</i>	<i>Conductances</i>	<i>Small geometry effect</i>	<i>Applicability of parameter set</i>	<i>Moderate inversion</i>	$g_m/I_D$	$D_{it}$
<i>SPICE Level (2)</i>	Vladimirescu & Liu (1980)	21	Not Continuous	Charge Sharing	Limited	Discontinuity in slope	Spike	Simple model
<i>BSIM</i>	Sheu, Ko & Jeng (1985)	67	Not Continuous	Semi-empirical	Limited by abnormal sec. effects	Discontinuity in slope	Discontinuity in slope	Simple model
<i>aMOS</i>	Chartterje & Machala (1995)	56	Continuous	Semi-empirical	Limited by minimum dimensions	Continuous	Discontinuity in slope	Simple model
<i>Our model</i>	This+previous work[30]	31	Continuous	Quasi 2D analysis	Limited by minimum dimensions	Continuous	Continuous	Physical

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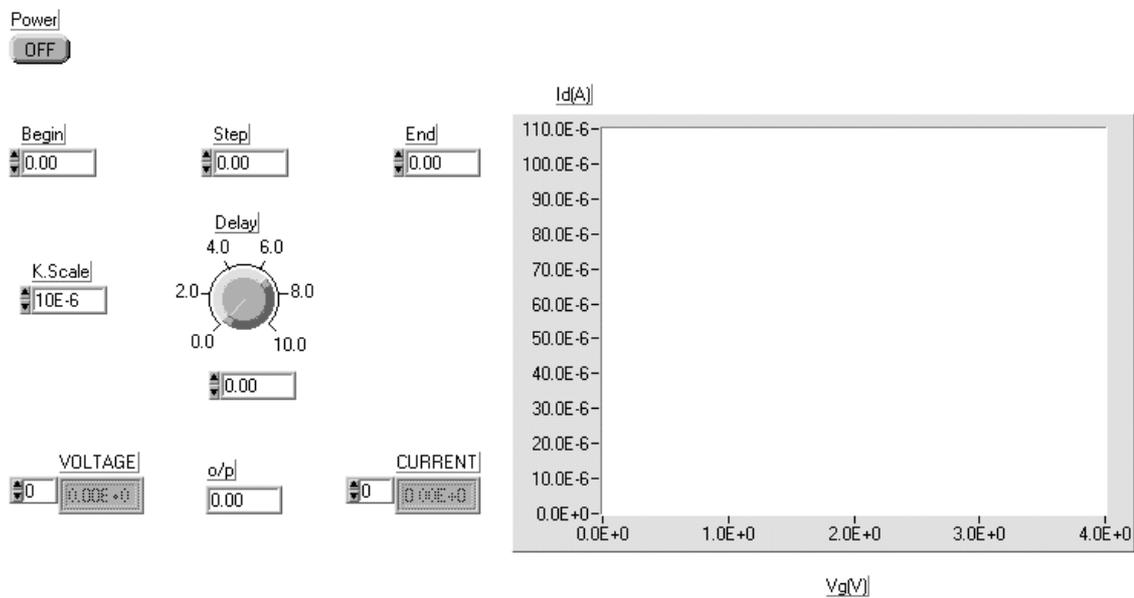
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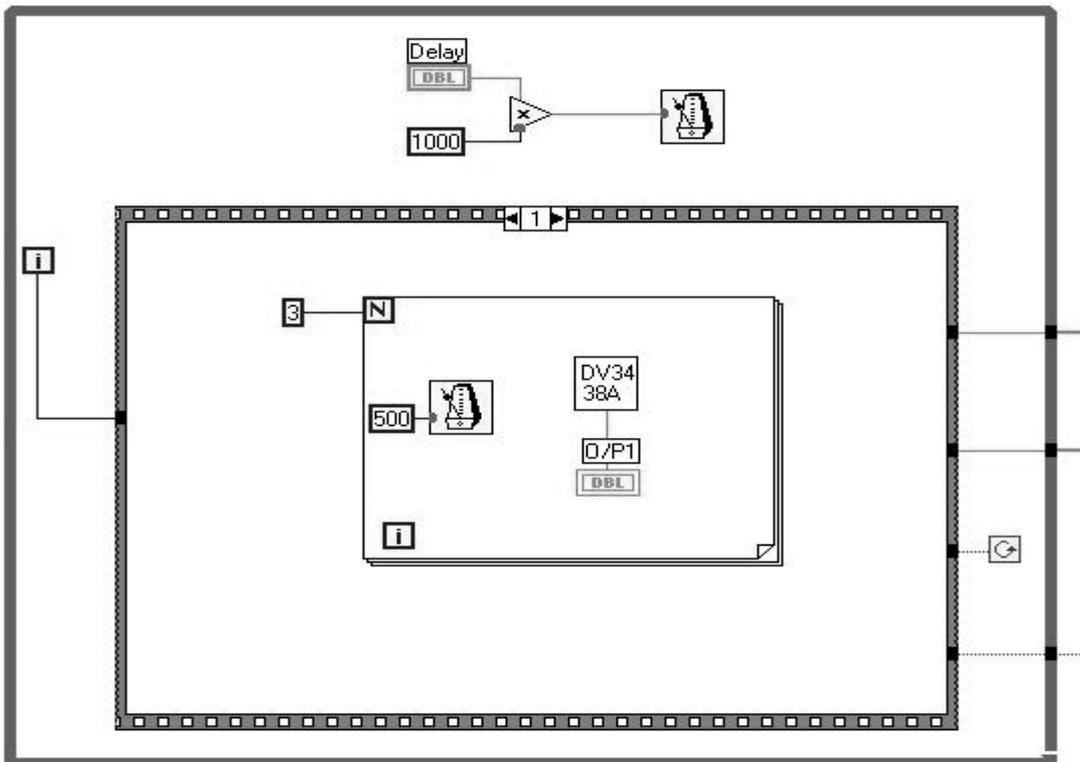
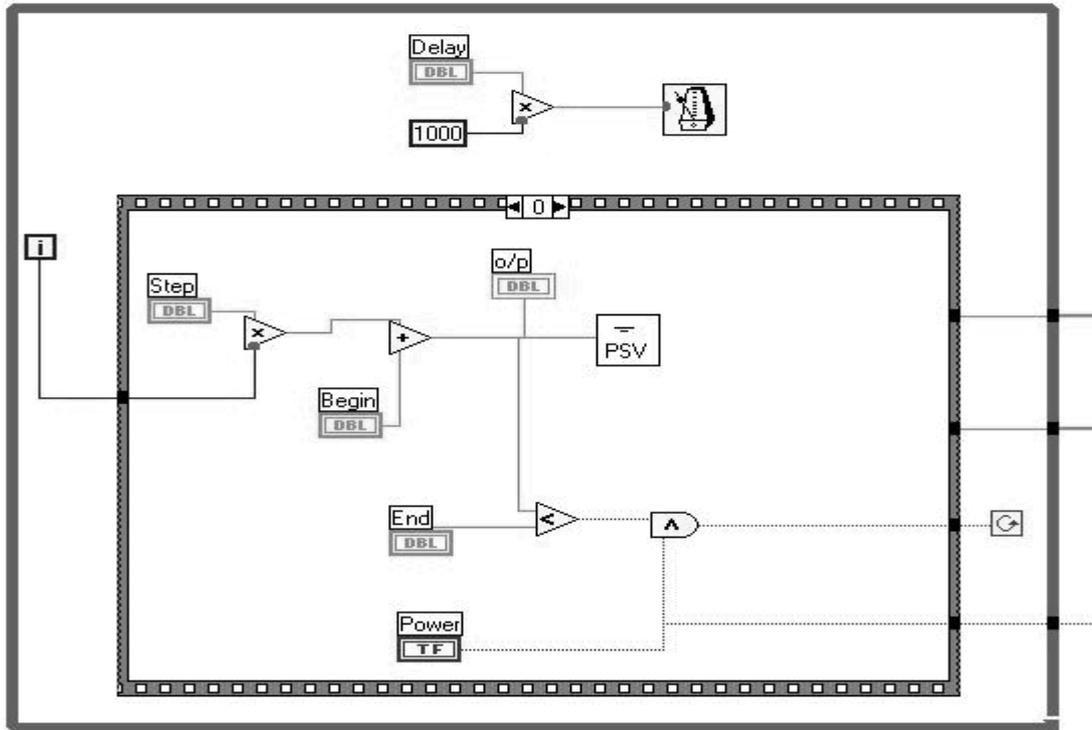
# Appendix A

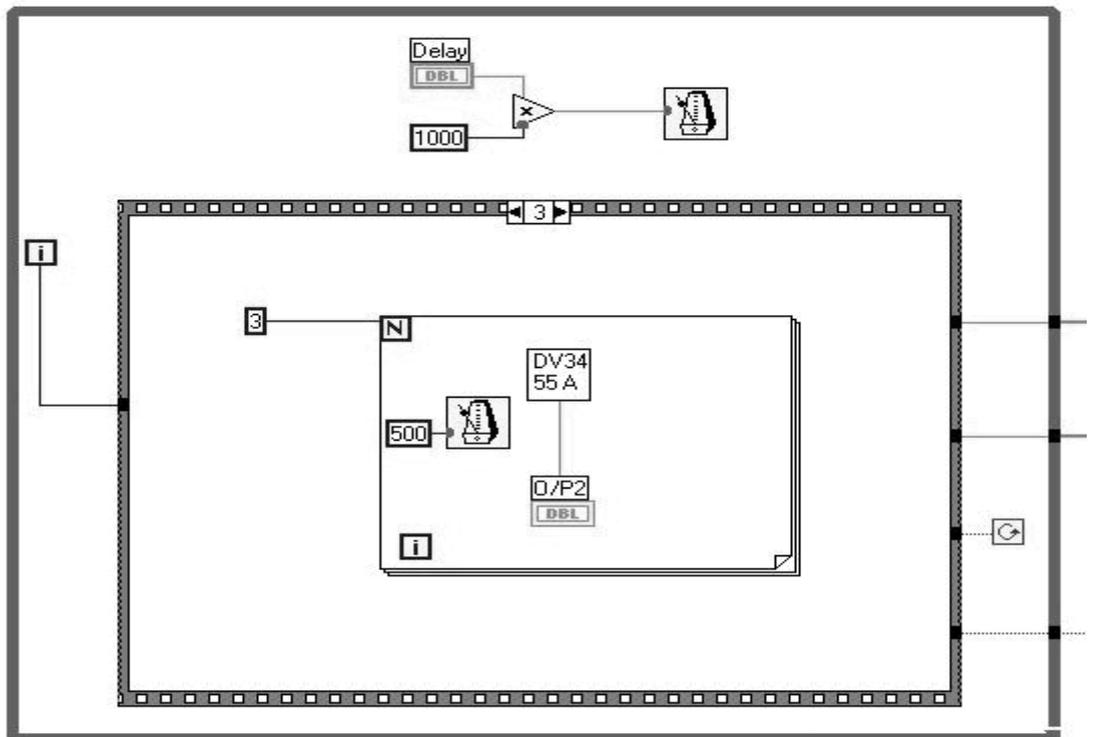
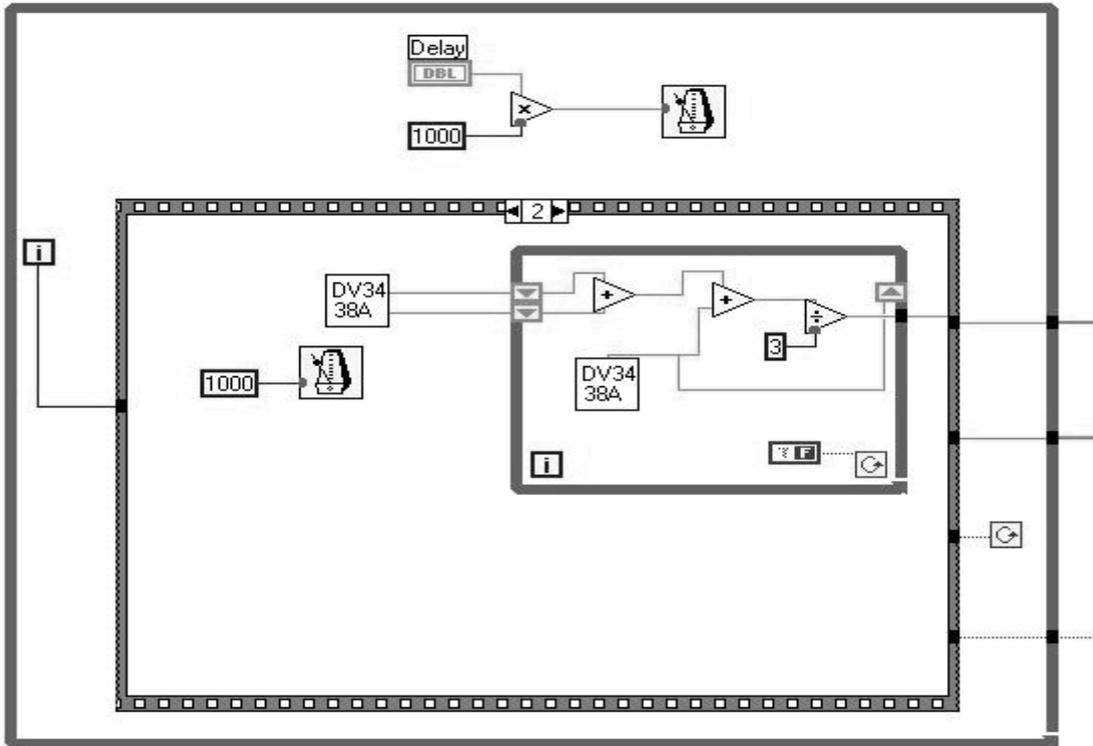
## Measurement program in G language

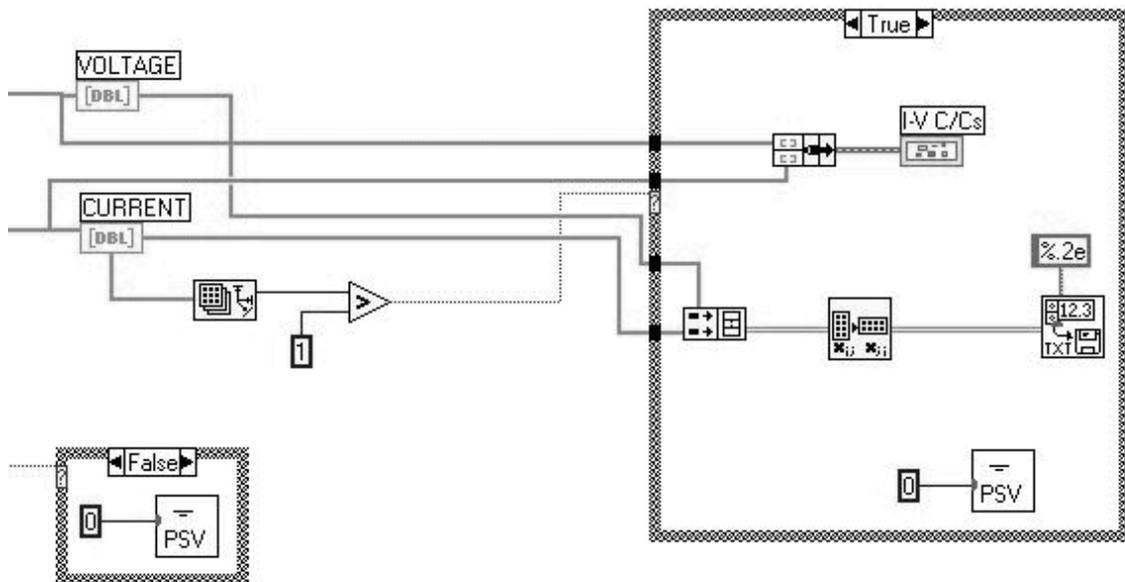
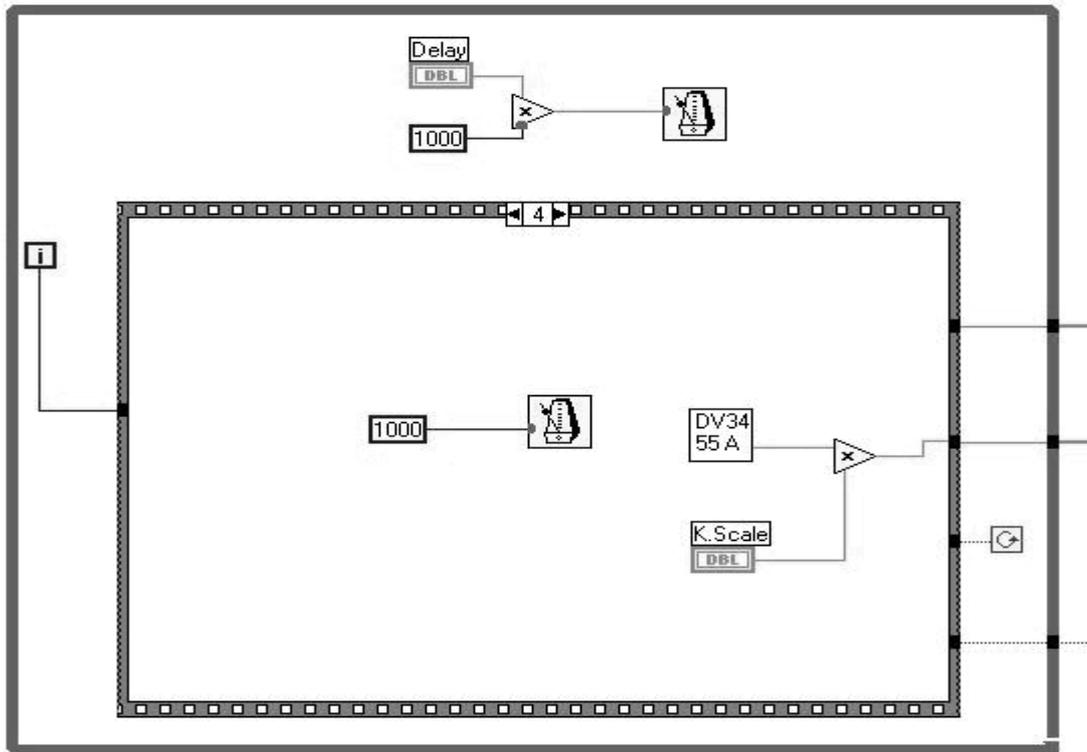
In this appendix we present the measurement program, which is written in the G language and run under LABView program. Fig. A.1 shows the control panel which represents the user interface to the program, while Fig. A.2 shows the block diagram which represents the program code in graphic format.



**Figure A.1** *Measurement program control panel*







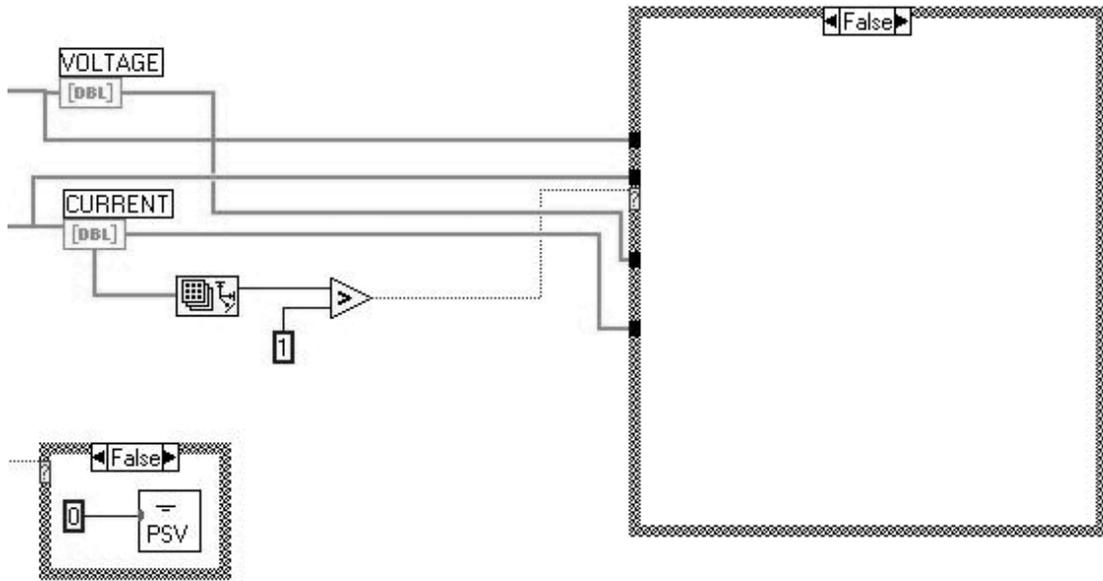


Figure A.2 Measurement program block diagram



# Appendix B

## Model Formulation in

### HDL-A<sup>1</sup> Language

```
--  
-- ICL Model for MOSFET  
--  
ENTITY NMOS IS  
  
GENERIC (  
    W,L,LDEL,DEW,yj,Tox,VTO,Gamma,PHI,VFB,Nsub,Nsd,Nox,  
    Dit,TPG,PMS,MUo,Theta,vmax,beta,Rt,Ld,xsat,Neff,  
    DSB,AI,BLI,I_leak,Sleak,Dose,D,nimp,mimp :REAL );  
  
PIN ( D,G,S,B: ELECTRICAL );  
END ENTITY NMOS;  
  
ARCHITECTURE a OF NMOS IS  
  
-- (* Constants *)  
    CONSTANT K,Eo,PHIt,q,ni,Eg,EGP :real;  
    CONSTANT Ko,Ks,Cox,PHIf,Vbi :real;  
    CONSTANT PHImS,Dit1,KP,EPSt :real;  
--(* Constant model parameter *)  
    CONSTANT VFB1,Gamma1:real;  
    CONSTANT Leff,Weff,Rs :real;  
    CONSTANT xep,EPS_MIN,lc :real;  
    CONSTANT xdibl,K1,KW :real;  
  
-- (* Variables *)  
  
    STATE VGB,VGB1,VGB2,VGBD,VSB:ANALOG ;  
    STATE VDB,VDB1,VDB2,VDS,VDS1,VDS2:ANALOG ;  
-- (* EPS calculation numerically *)
```

---

<sup>1</sup> HDL-A is a Hardware Description Language developed by ANACAD Electrical Engineering Software.

```

VARIABLE ii: integer;
VARIABLE xd1,xd2:real;
STATE EPSw1,EPSw2,EPSw3,EPSw4:ANALOG;
STATE EPSst1,EPSst2,EPSst4:ANALOG;
STATE EPS1,EPS2,EPS3,EPS4:ANALOG;
-- (* NOTE: EPS with
-- (1) -> at the source without Dit
-- (2) -> at the drain without Dit taking the effect of Dit on Vth
-- (3) -> at the source with Dit
-- (4) -> at the drain with Dit *)
VARIABLE X1,X2:real;
VARIABLE d2Qsc_dEP,d2Qit_dEP:real;
VARIABLE FF0,FF1,dFF1_dEP,d2FF1_dEP:real;

-- (* Charges *)
STATE Qit_s1,Qit_d1:ANALOG;
STATE Qvs1,Qvd1:ANALOG;

-- (* Currents *)
VARIABLE ED,ED1,ED2,ED32,ED12,EPSs,EPSd:real;
STATE ID,IDD,IDS,IDdiff,Idrift :ANALOG;

-- (* Mobility model *)
STATE FG,FL,FL0,j1:ANALOG;
STATE MU,MU1,MU2:ANALOG;

-- (* Saturation *)
STATE VTH1,VTH,VDSsat,Vss,Vsl,A,B1:ANALOG;
STATE DL,Idrift1,Isat,bb,bb1,FB:ANALOG;

-- (* Impact ionization current *)
STATE Isub,Idam :ANALOG;

-- (* Threshold shift + DIBL *)
STATE ddep,LAMDA,VGTH,V1,V2,k2:ANALOG;
VARIABLE alaa1,alaa2,alaa3,alaa4,alaasnh1:real;
STATE DIBL,DIBL1,XDIBL1,XDIBL2:ANALOG;
STATE Vb_PHIs3,Vb_PHIs4:ANALOG;
STATE PHIs3,PHIs4,L4,L5,L1,L2,L3:ANALOG;

-- (* Test variables *)
STATE reg,j2,n1,n2,n3,n4:ANALOG;

```

**BEGIN RELATION****PROCEDURAL FOR INIT =>**

```

-- (*Parameters' default values*)
W := 20.0e-4;      -- (*Width (cm) 20 um*)
L := 20.0e-4;      -- (*Length (cm) 10 um*)
LDEL := 0.0;      -- (*Total Length shortening (cm)*)
DEW := 0.0;      -- (*Total Width shortening (cm)*)
yj := 0.5e-4;     -- (*Junction depth (cm) 0.4 um*)
Tox := 20.0e-7;   -- (*Oxide thickness (cm) 20 nm*)
VTO := 0.0;      -- (*OPTIONAL, Threshold voltage at VSB := 0
-- and for large L)
Gamma := 0.0;     -- (*OPTIONAL, Body factor*)
PHI := 0.0;      -- (*OPTIONAL, Surface potential at threshold*)
VFB := 0.0;      -- (*OPTIONAL, Flat-band voltage*)
Nsub := 1.0e+16;  -- (*Substrate doping (1/cm^3)*)
Nsd := 1.0e+19;  -- (*Source/drain doping (1/cm^3)*)
Nox := 0.0;      -- (*Oxide charge density (1/cm^2)*)
Dit := 0.0;      -- (*Interface trap density (1/cm^2.V*)
-- (*+ve -> Donor like
-- -ve -> Acceptor like *)
TPG := 0.0;      -- (*Gate type: 0 := Metal(Al),
-- -1 := NPOLY, +1 := PPOLY*)
PMS := 0.0;      -- (*Work funcion difference (V)
-- 0 use analytical model*)
MUo := 650.0;    -- (*Low field mobility (cm^2/V.s)*)
Theta := 0.05;   -- (*Gate effect on the mobility (1/V)*)
vmax := 1.0e+7;  -- (*Electrons saturation velocity (cm/s)*)
beta := 2.0;     -- (*Lateral mobility exponent (for electrons) *)
Rt := 0.0;      -- (*Total series resistance (Ohm)*)
Ld := 0.0;      -- (*DIBL charachteristic length (cm)*)
xsat := 10.0;   -- (*Saturation velocity knee factor*)

-- (*Saturation *)
Neff := 1.0;     -- (*Saturation slope factor*)
DSB := 3.0;     -- (*DIBL dependence on the bulb voltage*)
AI := 1.2;      -- (*Impact ionization multiplication coeff (V^-1)*)
BI := 1.3e6;    -- (*Impact ionization c/c field (V/cm)*)
-- (* BI postpones the rise of the current,
-- AI controls the magnitude of the
-- impact ionization current *)

```

```

I_leak := 1.0e-20;    -- (*Leakage current (amp)*)
Sleak := 100.0;     -- (*Leakage current division factor.
                    -- Determines the knee of leakage current*)
Dose := 0.0;        -- Dose in cm-3
D := 0.5e-4;       -- Non uniform doping effective width in cm
nimp := 0.2;       -- Control doping shape
mimp := 5.0;       -- Non uniform doping knee factor

-- (*Constants*)
Eo := 8.854e-14;    -- (*Permittivity of free space (F/cm)*)
K := 1.38066e-23;  -- (*Boltzmann's constant *)
q := 1.6e-19;      -- (*Magnitude of electron charge (C)*)
Ko := 3.9;         -- (*SiO2 relative permittivity*)
Ks := 11.9;        -- (*Si relative permittivity*)

-- (*Temperature dependent constants*)
PHIt := K * Temperature/q;  -- (*Thermal voltage (V)*)
Eg := (1.16-7.02e-4*(Temperature ** 2.0)/(Temperature+1108.0)) /PHIt;
      -- (*Si energy gap (eV)*)
      -- (*Normalized to PHIt*)
ni := (1.45E10)*((Temperature/300.0) ** 1.5)*exp((q*Eg*PHIt)
      /(2.0*K)*(1.0/300.0-1.0/Temperature));
      -- (*Intrinsic density (1/cm3)*)

-- (*constant model parameters*)
lc := sqrt(Ks/Ko*Tox*yj);
Rs := Rt/2.0;
Leff := L-LDEL;    -- (*Effective channel length*)
Weff := W-DEW;     -- (*Effective channel width*)
IF (PHI = 0.0) THEN
  PHIf := ln(Nsub/ni); -- (*Ei-Ef in the bulk (V)*)
                -- (*Normalized to PHIt*)
ELSE
  PHIf := PHI/(2.0*PHIt);
END IF;
EGP := EG/2.0-PHIf;
EPS_MIN := 2.0;    -- (*Minimum EPSI allowed, ELSE current :=
I_leak*)
EPSt := 2.0*PHIf;  -- (*Strong inversion surface potential (V)*)
                -- (*Normalized to PHIt*)
Cox := Eo*Ko/Tox;  -- (*Oxide capacitance/area (F/cm2)*)
IF (Gamma = 0.0) THEN  -- (*Body factor (V1/2)*)

```

```

-- (*Normalized to PHIt1/2*)
Gamma1 := sqrt(2.0*q*Ks*Eo*Nsub/PHIt)/Cox;
ELSE
Gamma1 := Gamma;
END IF;

KW := pi*Ks*Tox/(Ko*Weff);
-- (*Constants used in narrow channel effect*)

-- (* Threshold model *)
IF (VTO = 0.0) THEN
IF (VFB = 0.0) THEN

IF (PMS = 0.0) THEN -- (*Use analytical model for PMS *)
-- (*Normalized to PHIt1/2*)
IF (TPG = 1.0) THEN -- (*PPOLY Gate*)
PHImS := EG/2.0-PHIf;
ELSE IF (TPG = -1.0) THEN -- (*NPOLY Gate*)
PHImS := -EG/2.0-PHIf;
ELSE -- (*METAL Gate*)
PHImS := -0.05/PHIt-EG/2.0-PHIf;
END IF;
END IF;
ELSE -- (*Use the given PMS*)
PHImS := PMS/PHIt;
END IF;
VFB1 := PHImS-(q*Nox)/Cox/PHIt;

ELSE -- (*VFB*)
VFB1 := VFB/PHIt;
END IF; -- (*VFB*)
ELSE -- (*VTO*)
VFB1 := VTO/PHIt-EPSt-Gamma1*sqrt(EPSt);
END IF; -- (*VTO*)

IF (Dit = 0.0) THEN
Dit1 := 0.0;
ELSE IF (Dit > 0.0) THEN
Dit1 := Dit;
Vfb1 := Vfb1-(q*Dit1*(EG-EGP))/Cox;
ELSE
Dit1 := -Dit;

```

```

    Vfb1 := Vfb1+q*Dit1*EGP/Cox;
  END IF;
  END IF;
      -- (*Flat band voltage (V)*)
      -- (*Normalized to PHIt*)
  Vbi := ln(Nsub*Nsd/ni/ni);
      -- (*Built-in junction voltage (V)*)
      -- (*Normalized to PHIt*)
  KP := (Weff/Leff)*Cox*(PHIt ** 2.0);
      -- (*Transconductance parameter (F.V2/cm2)*)
  xep := 10.0;      -- (*Knee factor for limiting EPSI in
      -- Qit calculation *)

-- (* Threshold shift + DIBL *)
  K1 := (PHIt)*(2.0*Ks*Eo)/(q*Nsub);
      -- (*Normalized to PHIt (V-1)*)
  xdibl := 5.0;      -- (*Diffusion current CLM knee factor*)
  LAMDA := Ld;

PROCEDURAL FOR DC =>
-- (* All voltages are normalized to PHIt, and are referenced to
-- the bulk potential VB*)

-- (***** Measure the pins' voltages *****)
  VSB := (S.v-B.v)/PHIt;
  VGB := (G.v-B.v)/PHIt-VFB1-KW*(EPSt+VSB);
  VDB := (D.v-B.v)/PHIt;
  VDS := (D.v-S.v)/PHIt;

-- (*NOTE: VDB1, VGB1, VDS1 are used in strong inversion, while
-- VDB2, VGB2, VDS2 are used in weak inversion *)

  IF (VDS = 0.0) THEN
    IDdiff := I_leak/Sleak;
    IDdrift := I_leak/Sleak;
  ELSE

  IF (VGB <= 0.0) THEN
    REPORT "VG-VB-Vfb is negative, the device is in
accumulation" SEVERITY WARNING;
    IDdiff := I_leak/Sleak;
    IDdrift := I_leak/Sleak;

```

```

ELSE

-- (**** Threshold shift + DIBL using the threshold surface potential ****)

    EPSs := EPSt+real(VSB);

    IF (Ld = 0.0) THEN
        ddep := sqrt(K1*EPSs);
        LAMDA := 0.1 * ((yj*real(ddep)*Tox) ** (1.0/3.0));
    ELSE IF (B.v /= 0.0) THEN
        k2 := (real(LAMDA) ** (DSB))/EPSt;
        LAMDA := (real(k2)*(EPSs)) ** (1.0/DSB);
    END IF;
END IF;

    alaa1 := exp(Leff/real(LAMDA));
    alaa2 := exp(-Leff/real(LAMDA));
    alaa3 := exp(Leff/(2.0*real(LAMDA)));
    alaa4 := exp(-Leff/(2.0*real(LAMDA)));
    alaa1 := (alaa3-alaa4) ** 2.0;

    V1 := Vbi+VSB-EPSs;
    V2 := V1+VDS;

    DIBL := (2.0*real(V1)+real(V2)*(1.0-alaa2)+2.0*sqrt((real(V1) **
    2.0)+real(V1*V1)*(alaa1-1.0)))/alaa1; -- (*DIBL with VDS*)

    VGB2 := VGB+DIBL;
        -- (*VGB to be used in the diffusion component*)

-- (*Local bias dependent constants*)
    FB := 1.0+GAMMA1/(2.0*sqrt(1.0/PHIt+VSB+EPSt));
        -- (*Saturation voltage division factor
        -- as in Tsividis*)

    VTH1 := (EPSt+VSB+Gamma1*sqrt(EPSt+VSB)-DIBL)*2.5;
    VGTH := real(VGB2/VTH1) ** 5.0;
    XDIBL1 := 1.0-VGTH/(1.0+VGTH); -- (*Used in VGB1*)

    VTH1 := (EPSt+6.0+VSB+Gamma1*sqrt(EPSt+6.0+VSB)-DIBL);
    VGTH := real(VGB2/VTH1) ** 15.0;

```

```

XDIBL2 := 1.0-VGTH/(1.0+VGTH);    -- (*Used in VDB2*)

VGB1 := VGB+DIBL*xdibl1*1.2;
      -- (*VGB to be used in the drift component*)

-- (***** Initial Guess for the surface potentials *****)

-- (* Weak inversion estimated maximum surface potential *)

IF ((Gamma1/2.0) ** 2.0 + VGB2-1.0 < 0.0) THEN
  REPORT "Weak inversion Surface potential is negative"
SEVERITY WARNING;
  IDdiff := I_leak/Sleak;
  IDdrift := I_leak/Sleak;
ELSE

-- (* Estimated EPSW without Dit *)
EPSw1 := VGB1+(Gamma1 ** 2.0)/2.0-Gamma1 *
  sqrt((Gamma1/2.0) ** 2.0 + VGB1-1.0);
  -- (*used in EPS1 and EPS2*)
EPSw2 := VGB2+(Gamma1 ** 2.0)/2.0-Gamma1 *
  sqrt((Gamma1/2.0) ** 2.0 + VGB2-1.0);
  -- (*used in EPS3 and EPS4*)

-- (* Estimated EPSW with Dit *)
IF (Dit1 /= 0.0) THEN

  X1 := 1.0+q*Dit1/Cox;

  X2 := real(VGB2)-q*Dit1*(-real(VSB)+ln(1.0+exp(-
    (real(EPSw2)+EGP-real(VSB)))))/Cox;
  EPSw3 := (X1*X2+(Gamma1 ** 2.0) / 2.0 - Gamma1 *
    sqrt((Gamma1/2.0) ** (2.0) + X1*X2 - X1 ** (2.0)))
    / (X1 ** 2.0);

  X2 := real(VGB2)-q*Dit1*(-real(VDB2)+ln(1.0+exp(-
    (real(EPSw2)+EGP-real(VDB2)))))/Cox;
  EPSw4 := (X1*X2+(Gamma1 ** 2.0) / 2.0 - Gamma1 *
    sqrt((Gamma1/2.0) ** (2.0) + X1*X2 - X1 ** (2.0)))
    / (X1 ** 2.0);

```

```

ELSE
    EPSw3 := EPSw2;
    EPSw4 := EPSw2;
END IF;
    EPSw2 := EPSw1;

-- (*EPS Check*)

if ( (EPSw1 <= EPS_MIN) OR (EPSw2 <= EPS_MIN) OR
    (EPSw3 <= EPS_MIN) OR (EPSw4 <= EPS_MIN)) THEN
    REPORT "EPSW is negative" SEVERITY WARNING;
    IDdiff := I_leak/Sleak;
    IDdrift := I_leak/Sleak;

ELSE

-- (* Strong inversion estimated surface potential *)

IF (abs(VGB1-EPSt-VSB) < 1.5) THEN
    EPSst1 := EPSt+VSB+2.0;
ELSE
    EPSst1 := EPSt+VSB+2.0*ln(abs(VGB1-EPSt-VSB)/Gamma1);
END IF;

-- (Continuous estimated surface potential (first approximation, empirical))

    xd1 := 9.0+9.0*real(VSB)*PHIt;
    xd2 := 9.0+9.0*real(VDB)*PHIt;

-- (* xd := 9 in the above calculations the error in epsi is less than 0.08%
-- in the range of Nsub := 1e15-1e18 and Dit1 := 0-3e11 *)

    EPS1 := real(EPSw1)/(1.0+(real(EPSw1)/real(EPSst1)) **
    xd1)**(1.0/xd1);
    EPS3 := real(EPSw3)/(1.0+(real(EPSw3)/real(EPSst1)) **
    xd1)**(1.0/xd1);

-- (*To compute EPS2 and EPS4 we must take into account the saturation
-- effect by calculating VDSsat *)

-- (*Normal field effect on the mobility *)
    EPSs := real(EPS1);

```

```

EPSd := real(EPS1);
ED2 := (EPSd+EPSs)/(2.0);

FG := 1.0+Theta*PHIt*(VGB1-ED2);

MU1 := MUo/FG;

-- (* calculation of pre-VDS1 saturation for EPS2 and EPS4 calculation*)

Vss := vmax*Leff/(MU1*PHIt);
VTH := EPS1+Gamma1*sqrt(EPS1-1.0);
bb := w/Leff*MU1*Cox;
Vsl := (VGB1-VTH)/FB;
bb1 :=
sqrt(1.0+2.0*real(bb)*real(Vsl)*PHIt*Rs+(real(Vsl)/real(Vss))
** 2.0);

Isat := (bb1-(1.0+bb*Vsl*PHIt*Rs))/(bb*
(1.0/((real(bb)*real(Vss)*PHIt)** 2.0)-(Rs** 2.0)));

VDSsat := 0.01+(Vsl*PHIt+(Rs-1.0/(bb*Vss*PHIt))*Isat)/PHIt;

VDS1 := (real(VDS)/(1.0+(real(VDS)/real(VDSsat))**
xsat)**(1.0/xsat));
VDB1 := VDS1+VSB; -- (*VDB taking saturation into effect*)

VDS2 := VDS1*(1.0-Xdibl2)+VDS*Xdibl2;
VDB2 := VDS2+VSB; -- (*VDB taking saturation into effect*)

-- (* EPS2*)

IF (abs(VGB1-EPSt-VDB1) < 1.5) THEN
    EPSst2 := EPSt+VDB1+2.0;
ELSE
    EPSst2 := EPSt+VDB1+2.0*ln(abs(VGB1-EPSt-
VDB1)/Gamma1);
END IF;

EPS2 := real(EPSw2)/(1.0+(real(EPSw2)/real(EPSst2))** xd2)**
(1.0/xd2);

```

```

-- (* EPS4 *)

-- (* For EPS4 the drain saturation voltage is equal to VDS in weak
-- inversion and VDS1at in strong inversion*)

IF (abs(VGB2-EPSst-VDB2) < 1.5) THEN
    EPSst2 := EPSst+VDB2+2.0;
ELSE
    EPSst2 := EPSst+VDB2+2.0*ln(abs(VGB2-EPSst-
    VDB2)/Gamma1);
END IF;

EPS4 := real(EPSw4)/(1.0+(real(EPSw4)/real(EPSst2)) ** xd2) **
(1.0/xd2);

-- (*EPS Check*)

if ((EPS1 <= EPS_MIN) or (EPS2 <= EPS_MIN) or
    (EPS3 <= EPS_MIN) or (EPS4 <= EPS_MIN)) THEN
    REPORT "EPSes is negative" SEVERITY WARNING;
    IDdiff := I_leak/Sleak;
    IDdrift := I_leak/Sleak;
ELSE

--(* Continuous estimated surface potential (second approximation,
-- second order Newton-Raphson) *)

    Qvs1 := real(EPS3)/((1.0+(real(EPS3)/(EG-EGP+real(VSB)))) ** xep)
** (1.0/xep));
    Qvd1 := real(EPS4)/((1.0+(real(EPS4)/(EG-EGP+real(VDB2)))) **
xep) ** (1.0/xep));

    FOR ii IN 1 TO 2 LOOP        -- (*Using 2 iterations*)

-- (* Compute EPS3 and EPS4 used in the calculation of the diffusion
component*)

-- (*Normal field effect on the mobility *)
    EPSs := real(EPS1);

```

```

    EPSd := real(EPS2);
    ED := EPSd-EPSs;
    ED2 := (EPSd+EPSs)/(2.0);
    ED32 := (EPSd) ** (1.5) -
            (EPSs) ** (1.5);

    IF (ED = 0.0) THEN
        FG := 1.0+Theta*PHIt*(VGB1-ED2);
    ELSE
        FG := 1.0+Theta*PHIt*(VGB1-
ED2+(1.0/1.5)*Gamma1*ED32/ED);
    END IF;

    MU1 := MUo/FG;

-- (* calculation of VDS1 saturation for EPS4 calculation*)

    Vss := vmax*Leff/(MU1*PHIt);
    VTH := real(EPS1)+Gamma1*sqrt(real(EPS1)-1.0);
    bb := w/Leff*MU1*Cox;

    Vsl := (VGB1-VTH)/FB;
    bb1 :=
sqrt(1.0+2.0*real(bb)*real(Vsl)*PHIt*Rs+(real(Vsl)/real(Vss)) ** 2.0);

    Isat := (real(bb1)-(1.0+real(bb)*real(Vsl)*PHIt*Rs))/
            (real(bb)*(1.0/((real(bb)*real(Vss)*PHIt) ** 2.0)-(Rs ** 2.0)));

    VDSsat := 0.01+(Vsl*PHIt+(Rt/2.0-1.0/(bb*Vss*PHIt))*Isat)/PHIt;

    VDS1 := (real(VDS)/(1.0+(real(VDS)/real(VDSsat)) ** xsat) **
(1.0/xsat));
    VDB1 := VDS1+VSB;    -- (*VDB1 taking saturation into effect*)

    VDS2 := VDS1*(1.0-Xdibl2)+VDS*Xdibl2;
    VDB2 := VDS2+VSB;    -- (*VDB2 taking saturation into effect*)

    IF (Dit1 /= 0.0) THEN

-- (*****EPS3**)

    X1 := exp(-(EGP+real(Qvs1)-real(VSB)));

```

```

d2Qit_dEP := -q*Dit1*(X1/(1.0+X1))*(1.0-X1/(1.0+X1));

X2 := exp(real(EPS3)-2.0*PHIf-real(VSB));
FF0 := sqrt(real(EPS3)-1.0+X2);
d2Qsc_dEP := -Gamma1*Cox/(2.0*FF0)*(X2-((1.0+X2)
** (2.0)) / (2.0*FF0 ** 2.0));
FF1 := real(EPS3)-real(VGB2)+(Gamma1*Cox*FF0+q*Dit1*
(real(Qvs1)-real(VSB)+ln((1.0+X1))))/Cox;
dFF1_dEP := 1.0+(q*Dit1*(1.0-X1/(1.0+X1))
+Gamma1*Cox/(2.0*FF0)*(1.0+X2))/Cox;
d2FF1_dEP := -(d2Qsc_dEP+d2Qit_dEP)/Cox;

EPS3 := EPS3-(FF1/dFF1_dEP)/(1.0-(FF1*d2FF1_dEP)/
(2.0*(dFF1_dEP) ** 2.0));

-- (*****EPS4**)

X1 := exp(-(EGP+real(Qvd1)-real(VDB2)));
d2Qit_dEP := -q*Dit1*(X1/(1.0+X1))*(1.0-X1/(1.0+X1));

X2 := exp(real(EPS4)-2.0*PHIf-real(VDB2));
FF0 := sqrt(((real(EPS4)-1.0)+X2));
d2Qsc_dEP := -Gamma1*Cox/(2.0*FF0)*(X2-((1.0+X2)
** (2.0)) / (2.0*FF0 ** 2.0));

FF1 := real(EPS4)-real(VGB2)+(Gamma1*Cox*FF0+q*Dit1*
(real(Qvd1)-real(VDB2)+ln((1.0+X1))))/Cox;
dFF1_dEP := 1.0+(q*Dit1*(1.0-X1/(1.0+X1))
+Gamma1*Cox/(2.0*FF0)*(1.0+X2))/Cox;
d2FF1_dEP := -(d2Qsc_dEP+d2Qit_dEP)/Cox;

EPS4 := EPS4-(FF1/dFF1_dEP)/(1.0-(FF1*d2FF1_dEP)/
(2.0*(dFF1_dEP) ** 2.0));

-- (*****Qit**)

Qvs1 := real(EPS3)/((1.0+(real(EPS3)/(EG-EGP+real(VSB))) **
xep) ** (1.0/xep));
Qvd1 := real(EPS4)/((1.0+(real(EPS4)/(EG-EGP+real(VDB2))) **
xep) ** (1.0/xep));

Qit_s1 := -q*Dit1*(Qvs1-VSB+ln(1.0+(exp(-EGP+VSB-Qvs1))));

```

```

    Qit_d1 := -q*Dit1*(Qvd1-VDB2+ln(1.0+(exp(-EGP+VDB2-
    Qvd1)))));

ELSE                                     -- (*Dit := 0.0*)

-- (*****EPS3**)

    X2 := exp(real(EPS3)-2.0*PHIf-real(VSB));
    FF0 := sqrt(((real(EPS3)-1.0)+X2));
    d2Qsc_dEP := -Gamma1*Cox/(2.0*FF0)*(X2-((1.0+X2)
    ** (2.0)))/(2.0*FF0 ** 2.0));

    FF1 := real(EPS3)-real(VGB2)+(Gamma1*Cox*FF0)/Cox;
    dFF1_dEP := 1.0+(Gamma1*Cox/(2.0*FF0)*(1.0+X2))/Cox;
    d2FF1_dEP := -(d2Qsc_dEP)/Cox;

    EPS3 := EPS3-(FF1/dFF1_dEP)/(1.0-(FF1*d2FF1_dEP)/
    (2.0*(dFF1_dEP) ** 2.0));

-- (*****EPS4**)

    X2 := exp(real(EPS4)-2.0*PHIf-real(VDB2));
    FF0 := sqrt(((real(EPS4)-1.0)+X2));
    d2Qsc_dEP := -Gamma1*Cox/(2.0*FF0)*(X2-((1.0+X2)
    ** (2.0)))/(2.0*FF0 ** 2.0));

    FF1 := real(EPS4)-real(VGB2)+(Gamma1*Cox*FF0)/Cox;
    dFF1_dEP := 1.0+(Gamma1*Cox/(2.0*FF0)*(1.0+X2))/Cox;
    d2FF1_dEP := -(d2Qsc_dEP)/Cox;

    EPS4 := EPS4-(FF1/dFF1_dEP)/(1.0-(FF1*d2FF1_dEP)/
    (2.0*(dFF1_dEP) ** 2.0));

    Qit_s1 := 0.0;
    Qit_d1 := 0.0;

END IF;

-- (*The effect of Qit on the threshold for the drift component*)

    VGBD := VGB1+Qit_s1/Cox;

```

```
-- Compute EPS1 and EPS2 used in the calculation of the drift component
```

```
-- (*****EPS2***)
```

```

X2 := exp(real(EPS2)-2.0*PHIf-real(VDB1));
FF0 := sqrt(((real(EPS2)-1.0)+X2));
d2Qsc_dEP := -Gamma1*Cox/(2.0*FF0)*(X2-((1.0+X2)
** (2.0)) / (2.0*FF0 ** 2.0));

FF1 := real(EPS2)-real(VGBD)+(Gamma1*Cox*FF0)/Cox;
dFF1_dEP := 1.0+(Gamma1*Cox/(2.0*FF0)*(1.0+X2))/Cox;
d2FF1_dEP := -(d2Qsc_dEP)/Cox;

EPS2 := EPS2-(FF1/dFF1_dEP)/(1.0-(FF1*d2FF1_dEP)/
(2.0*(dFF1_dEP) ** 2.0));

```

```
-- (*****EPS1***)
```

```

X2 := exp(real(EPS1)-2.0*PHIf-real(VSB));
FF0 := sqrt(((real(EPS1)-1.0)+X2));
d2Qsc_dEP := -Gamma1*Cox/(2.0*FF0)*((X2)-(1.0+X2)
** (2.0) / (2.0*FF0 ** 2.0));

FF1 := real(EPS1)-real(VGBD)+(Gamma1*Cox*FF0)/Cox;
dFF1_dEP := 1.0+(Gamma1*Cox/(2.0*FF0)*(1.0+X2))/Cox;
d2FF1_dEP := -(d2Qsc_dEP)/Cox;

EPS1 := EPS1-(FF1/dFF1_dEP)/(1.0-(FF1*d2FF1_dEP)/
(2.0*(dFF1_dEP) ** 2.0));

```

```
END LOOP; -- (*End of iteration loop*)
```

```
-- (*EPS Check*)
```

```

IF ((EPS1 <= EPS_MIN) or (EPS2 <= EPS_MIN) or
(EPS3 <= EPS_MIN) or (EPS4 <= EPS_MIN)) THEN
  REPORT "EPS is negative" SEVERITY WARNING;
  IDdiff := I_leak/Sleak;
  IDdrift := I_leak/Sleak;

```

```

ELSE

-- (***** Mobility *****)

-- (* Lateral Mobility model *)
  EPSs := real(EPS1);
  EPSd := real(EPS2);
  ED := EPSd-EPSs;
  ED2 := (EPSd+EPSs)/(2.0);
  ED32 := (EPSd-(1.0)) ** (1.5) -
    (EPSs-(1.0)) ** (1.5);

  FL0 := (PHIt*MU1/(vmax))*(abs(ED))/Leff;
  FL := (1.0+real(FL0) ** beta) ** (1.0/beta);

  MU2 := MU1/FL;

-- (*Series resistance effect*)
  IF (ED = 0.0) THEN
    j1 := 1.0+W/Leff*MU2*Cox*Rt*PHIt*(VGBD-ED2
      -2.0*Gamma1*sqrt(EPSs));
  ELSE
    j1 := 1.0+W/Leff*MU2*Cox*Rt*PHIt*(VGBD-ED2
      +(1.0/1.5)*Gamma1*ED32/ED-2.0*Gamma1*sqrt(EPSs));
  END IF;

  MU := MU2/j1;

-- (***** Current Components *****)

-- (* Drift current *)
  EPSs := real(EPS1);
  EPSd := real(EPS2);
  ED := EPSd-EPSs;
  ED2 := EPSd ** (2.0) - EPSs ** (2.0);
  ED32 := (EPSd-1.0) ** (1.5) -
    (EPSs-1.0) ** (1.5);
  IDdrift1 := KP*MU*(VGBD*ED-0.5*ED2-
(1.0/1.5)*Gamma1*ED32);

```

```

-- (* Channel length modulation *)

-- (* Saturation CLM*)
  A := q*Neff*Nsub*(Leff ** 2.0) / (Eo*Ks*PHIt);
  B1 := 2.0*(ln(yj/1.0e-6)-1.0)/(q*Neff*Nsub*vmax*W*yj);
  DL := (sqrt((real(Vss) ** 2.0) +
  2.0*real(A)*(1.0+real(B1)*real(IDdrift1))*(real(VDS)-real(VDS1)))
  -real(Vss))/(real(A)*(1.0+real(B1)*real(IDdrift1)));

-- (* Subthreshold *)

  PHIs3 := EPS3-VSB;
  PHIs4 := EPS4-VDB;

  n4 := 1.0;
  Vb_PHIs3 := n4*ln(1.0+exp((Vbi-PHIs3)/n4));
  Vb_PHIs4 := n4*ln(1.0+exp((Vbi-PHIs4)/n4));

  L4 := sqrt(K1*(Vb_PHIs3));
  L5 := sqrt(K1*(Vb_PHIs4));

-- (* Preventing the DIBL from diverging *)
  L4 := real(L4)/((1.0+(real(L4)/(Leff-0.2*Leff)) ** xdibl)
  ** (1.0/xdibl));
  L5 := real(L5)/((1.0+(real(L5)/(Leff-real(L4)-0.1*Leff)) ** xdibl)
  ** (1.0/xdibl));
  L2 := Leff-2.0*L4;

  L3 := Leff*(1.0-DL);
  L1 := L2*xdibl2+L3*(1.0-xdibl2);

  IDdrift := IDdrift1*Leff/L1;

-- (* Diffusion current *)
  EPSs := real(EPS3);
  EPSd := real(EPS4);
  ED1 := EPSd-EPSs;
  ED12 := sqrt((EPSd-(1.0))) -
  sqrt((EPSs-(1.0)));
  IDdiff := KP*(Leff/L1)*MU*(ED1+Gamma1*ED12-(Qit_d1-

```

```

    Qit_s1)/Cox);

    IF (IDdrift<I_leak/Sleak) THEN
        IDdrift := I_leak/Sleak;
    END IF;
    IF (IDdiff<I_leak/Sleak) THEN
        IDdiff := I_leak/Sleak;
    END IF;

    END IF;    -- (* IF VDS := 0 *)
    END IF;    -- (* IF VGB2 < 0.0 *)
    END IF;    -- (* IF EPSW < 0.0 *)
    END IF;    -- (* IF EPSw1 < 0.0 *)
    END IF;    -- (* IF EPSES < 0.0 *)
    END IF;    -- (* IF EPS < 0.0 *)
-- (* total current *)
    ID := (IDdrift+IDdiff);

-- (* Impact ionization current *)

    IF (VDS-VDS1 > 0.0) THEN
        Isub := AI*(VDS-VDS1)*PHIt*ID*exp(-BI*lc/((VDS-
VDS1)*PHIt));
        IDam := AI*(VDS-VDS1)*PHIt*ID/Leff*exp(-BI*lc/((VDS-
VDS1)*PHIt));
    ELSE
        Isub := 0.0;
        IDam := 0.0;
    END IF;

-- (* Drain and source currents *)
    IDD := ID+(1.0-2.0/Sleak)*I_leak+Isub+IDam;
    IDS := -ID+(1.0-2.0/Sleak)*I_leak-IDam;

-- (* Application of currents *)
    D.i %= IDD;
    S.i %= IDS;
    B.i %= -Isub;

END RELATION;

END ARCHITECTURE a;

```