A Fractional-N Frequency Synthesizer for Wireless Communications

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Abstract

The wireless market has experienced an exponential growth over the past few years. To sustain this growth along with the increasing demands of new wireless standards the cost, battery lifetime, and performance of wireless devices must all be enhanced.

With the advancement of radio frequency (RF) technology and requirement for more integration, new RF wireless architectures are needed. One of the most critical components in a wireless transceiver is the frequency synthesizer. It largely affects all three dimensions of a wireless transceiver design: cost, battery lifetime, and performance.

The common approach to frequency synthesis design for wireless communication is to design an analog-compensated fractional-N phaselocked loop (PLL). However, this technique lacks of adequate fractional spur suppression for third generation wireless standards. In this paper, a new sigma-delta PLL architectures is reported to enhance the above mentioned limitation with the aid of modified digital sigma-delta modulator to completely randomize fractional spurs present in fractional-N PLLs using feedback signal which serves as a dithering signal.

This aids in fully integrating a high-performance PLL frequency synthesizer, and hence reducing cost. The use of this architecture is examined to give as much as 14 dBs reduction in the fractional spurs.