King Fahd University of Petroleum and Minerals
Department of Electrical Engineering
EE 200 Digital Logic Circuit Design
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HW No. 5 (Due Sat. April 21)

1- Design a full subtractor, that is, a circuit which computes $a - b - c$, where c is the borrow from the next less significant digit and produces a difference, d, and a borrow from the next more significant bit, p.

2- Design an adder to add two decimal digits (plus a carry in), where the digits are stored in BCD code. (Assume that none or the unused combinations of input variables ever occur). The output is the code for a decimal digit plus the carry out.

3- A 4-bit BCD number is assumed to have an even parity bit. Draw the truth table indicating the parity bit column giving 1 to the parity bit for the states which are not included in the BCD. Let the parity bit represent the error-detection function. Design a combinational circuit for the error detection.

4-We have a decoder with three inputs, a, b, and c and eight active low outputs, labeled 0 through 7. In addition, there is an active low enable input *EN*. We wish to implement the following function using the decoder and as few NAND gates as possible. Show the block diagram

$$f(a, b, c, e) = \sum m(1, 3, 7, 9, 15)$$