Experiment
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Delta Modulation (DM)

MATLAB Simulation & Hardware Experimentation

Objectives

The main objectives of this experiment are:

1. To obtain a better understanding of Delta Modulation (DM) theory.
2. To learn how to simulate this digital transmission scheme using MATLAB.
3. To experiment with DM hardware implementation using the DCB platform.

Pre-Lab Work

You should read the relevant material in your textbook, and answer the following questions:

1. What is Delta Modulation comparable to (AM, FM, PCM, DPCM)? Explain.
2. Explain the meaning of “Delta” in the definition of Delta Modulation.
3. What are the advantages of Delta Modulation?

Overview

Like PCM and DPCM, Delta Modulation (DM) is a form of digital signal encoding. DM can be considered as a 1-bit differential PCM (DPCM) system. It converts each message signal amplitude change to a 1-bit sample: Logic 1 (or +E) for an increase, or Logic 0 (or -E) for a decrease. Therefore, the transmitted DM signal is a continuous series of bits indicating an increase or decrease in the message signal’s amplitude.

In a typical realization of DM, the transmitter circuit contains a digital sampler which generates the DM logic pulses. The digital sampler is a compare/hold circuit that compares the message signal’s amplitude with a reconstructed amplitude from a feedback integrator. Ideally, the feedback amplitude should be a close approximation of what the message-signal amplitude was at the previous clock cycle.

The DM receiver contains another integrator (similar to the transmitter's feedback integrator) and a low-pass filter which smoothes the distorted recovered signal out of the integrator.

DM transmission introduces some noise (or distortion) into the signal. There are different sources of distortion, including quantization noise and slope overload (refer to your textbook for a more in-depth description of these problems). DM relies on a very high sampling rate (typically much more than the minimum Nyquist rate of twice the signal bandwidth) to minimize the effects of distortion and to be able to produce an accurate re-construction of the signal.

In the hardware part of this lab, you will be using the DCB which contains a DELTA circuit block. In this block you will identify a comparator and a D-type flip flop which constitute the digital sampler in the DM transmitter. The comparator output feeds the D flip-flop input which latches (i.e., holds) the input value at its Q output (giving the DM transmitted bit sequence) until the next rising edge of the clock signal. The clock frequency is adjustable by control switches SW3&4, and can take any value among 8, 16, 32 and 64 kHz.

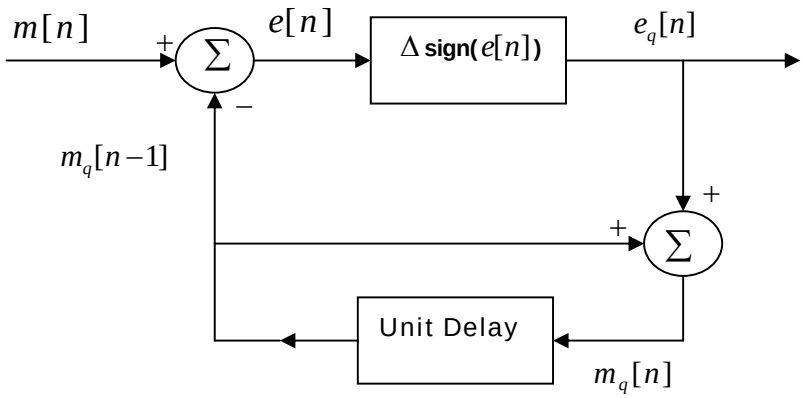
The transmitter feedback integrator is implemented by the INTEGRATE 1 circuit. The REF voltage determines how closely the feedback signal resembles the message signal. This REF value can be adjusted by the positive supply voltage potentiometer on the base unit. An RC time constant sets the positive and negative slope of the integrator output voltage. Each logic 1 DM pulse cause the integrator output voltage to increase by a fixed amount, and each logic 0 pulses causes it to decrease by a similar amount. Notice also the definition of the Baud rate for the transmitter. This simply means the number of signal changes per second. In the case of DM, this Baud rate is simply the bit rate out of the transmitter (true for binary modulation schemes only).

The DM receiver circuit is quite simple. It consists of a receive integrator and a low-pass filter. On the DCB, the receive integrator is the INTEGRATE2 circuit, and the LPF is the FILTER 1 circuit in the PAM-TDM circuit block. This filter recovers an approximate of the original message signal by smoothing out the high-frequency distortion in the integrated signal out of the INTEGRATE 2 circuit. Notice also that clock and synchronization circuits are not required in the demodulation process, which is another advantage of delta modulation.

Lab Work

Part I - MATLAB Simulation:

Consider the signal $m(t) = 2e^{-t/4}\cos(2\pi f_m t)$ where t is between 0 and 20 seconds with a step size equal to 1/the sampling frequency. The sampling frequency should be large as compared to the signal bandwidth. For example, let it equal to 40 times the f_m where $f_m = 0.4$ Hz. In order to specify the quantization step size, use the formula: $\Delta = \max|\frac{dm(t)}{dt}|/5$. Now, quantize $m(t)$ based on the following DM block diagram:



You need first to write down the equations of $e_q[n]$ and $m_q[n]$. Then use a **for**-loop to create $m_q[n]$. That is, implement the formula:

$$m_q[n] = \sum_{i=1}^{length(m[n])} e_q[i]$$

Note: before you start the **for**-loop, you need to initialize the value of $m_q[1]$ to be zero.

I-1) In figure 1, **plot** $m[n]$ vs. t, then **hold** that figure and use **stairs** function to plot $m_q[n]$ vs. t also. Finally, use **hold** again to disable that figure.

I-2) Generate figure 2 with two panels where the first panel plot $e_q[n]$ vs. t using **stem** and in the second panel, **plot** ($m[n] - m_q[n]$) vs. t. What are your observations? Indicate on the figures by using **gtext** command the types of noise you encountered in the quantized signal.

I-3) The above system described so far is the DM Transmitter. Using your knowledge about DM theory, propose a receiver block diagram, and specify its building blocks and how to simulate them in MATLAB.

Useful MATLAB Functions: sign, for, end, stairs, stem, plot, gtext, xlabel, ylabel, title.

Part II - Hardware Experimentation:

II.1) DM Transmission & Reception:

1. On the DELTA and PAM-TDM blocks, use three 2-post connectors to connect the M1 signal to the Digital Sampler input, the output of the Sampler to the input of INTEGRATE 2, and the output of INTEGRATE 2 to the input of FILTER 1 (in PAM-TDM). Verify the frequency & amplitude of the signal M1. Also check the frequency of the clock signal.

2. On the oscilloscope, observe and comment on the analog input M1 and the output signal of FILTER 1. **Note:** you should adjust the reference voltage for INTEGRATE 1 so that the output signal from FILTER 1 is maximized and not distorted. This is done by using the positive supply knob on the base unit.

3. Observe the output of the Digital Sampler on the oscilloscope. What does it correspond to? Measure the DM baud rate (or bit rate). Why is it equal to the clock frequency?

4. Use the oscilloscope to simultaneously display the input message signal and the fed-back signal from INTEGRATE 1. Sketch both signals, and explain why INTEGRATE 1 output closely tracks the input analog signal.

II.2) DM Performance Factors:

1. Observe the output of INTEGRATE 1 (or INTEGRATE 2) on the oscilloscope. Is it similar to the "accumulator" integrator used in the Matlab software part of the lab? Explain why they produce "saw-tooth" signals, and not stair-case signals. Hint: think about the typical response of 1^{st} order, RC & Op-Amp integrator.

2. Delta Modulation introduces **quantization noise**. Explain the impact of the integrator's RC time constant on this noise. Hint: think of the relation between the time constant RC, the integrator slope, and the amount of voltage increase or decrease in a given clock period (i.e., the quantization step size).

   Slope overload noise occurs when the input signal varies too fast for the DM bits to track closely. To study this, disconnect M1 and use the external function generator to apply a sinusoidal input signal of variable frequency. Study the impact of increasing the input signal frequency. To do so, observe the DM bits at the output of the sampler, the signal from INTEGRATE 1 (compared to the analog input) and the receiver output from Filter 1 as well. **Note:** you should also keep in mind that Filter 1 is a low-pass filter with 3dB cutoff frequency around 2.6 kHz.

Homework Questions

Q1. Explain the role of the receive filter (FILTER 1) in the operation of the DM receiver?

Q2. Discuss how the quantization step size affects quantization noise and slope overload noise and why?