KING FAHD UNIVERSITY OF PETROLEUM AND MINERALS
DEPARTMENT OF ELECTRICAL ENGINEERING
Electronic Circuits I - EE203

Experiment # 10

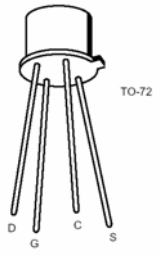
CMOS Inverter

OBJECTIVE

To study the general characteristics of Complementary Metal Oxide Semiconductor (CMOS) Logic as a circuit element.

COMPONENTS REQUIRED

- Resisters 1KΩ, 2KΩ, 5KΩ, 10KΩ,
- MOSFETS 2N4351, 2N4352



SUMMARY OF THEORY

The inverter is truly the nucleus of all digital designs. Once its operation and properties are clearly understood, designing more intricate structures such as NAND gates, adders, multipliers, and microprocessors is greatly simplified. The electrical behavior of these complex circuits can be almost completely derived by extrapolating the results obtained for inverters. The analysis of inverters can be extended to explain the behavior of more complex gates such as NAND, NOR, or XOR, which in turn form the building blocks for modules such as multipliers and processors.

The complementary MOSFET scheme (or CMOS) started the second revolution in computational machines. The limits of speed and density were conquered by moving to semiconductors and Very Large Scale Integration, but the power consumption and circuit cooling demands of bipolar transistors packed at extreme densities were formidable problems. The problem is that the transistor was always "on" (in other words drawing current and dissipating energy). CMOS circumvents this problem and allows bits to be stored without constant power consumption. A schematic of the CMOS inverter is given in the Figure 1 below.

This device dissipates energy only when it is switched from high to low or back. Quiescent operation in either the high or the low state dissipates essentially no power. So cooling the circuit is much easier, and supplying power is much less of a problem. If you don't believe me, just ask your calculator, digital watch or your laptop.

CMOS inverters are made of PMOS and NMOS transistors. PMOS and NMOS complement each other during regular operation of the inverter. The PMOS transistor conducts when logic zero is applied to its gate terminal and the NMOS transistor is off. The NMOS transistor conducts when logic one is applied to its gate terminal and the PMOS transistor is off.

In CMOS one transistor acts as a large resistance when the other is on. The PMOS transistor pulls the output up and the NMOS transistor pulls it down.

PSPICE

1. Circuit specifications and setup

Implement the circuit of a standard TTL inverter (shown in Figure 1) into a PSPICE circuit file or a Schematics file. The input signal to the inverter is a continuous symmetric square pulse of maximum amplitude of 5V and minimum amplitude of 0V. The period of the pulse is 400ns. (Note: to define such an input uses the *PULSE* source definition; refer to PSPICE handout. For Schematics users, the source *VPULSE* can be used. In this case make sure to change the source attributes to: V1=0, V2=5V, TD=100ns, TR=0s, TF=0s and PW=800ns). Use p-channel enhancement MOS number MbreakP and n-channel enhancement MOS number MbreakN. In the attributes of both transistor define L=2µm and W=10µm. Record all your results in the table.

2. Input/Output waveforms

Perform transient analysis of the circuit over 900ns interval with an increment of 10ns and observe the input and output waveforms on the same plot at the points marked V1, and V_{out}

3. Propagation delay

Using the results of part 2, estimate the propagation delay of the inverter. The propagation delay is defined as the difference in time between the 50% marks of the input pulse and the corresponding (inverted) output pulse (V_{out}).

4. Switching time (Speed)

Again using the results of part 2, focus on the output waveform and estimate the time that the output pulse takes to switch from the HIGH to LOW states and from the LOW to HIGH states. The switching time is defined as the difference in time between the 10% and the 90% marks on the output pulse for the LOW-HIGH case and the time between 90% and the 10% marks for the HIGH-LOW case (V_{out}). See Figure 2 for definitions

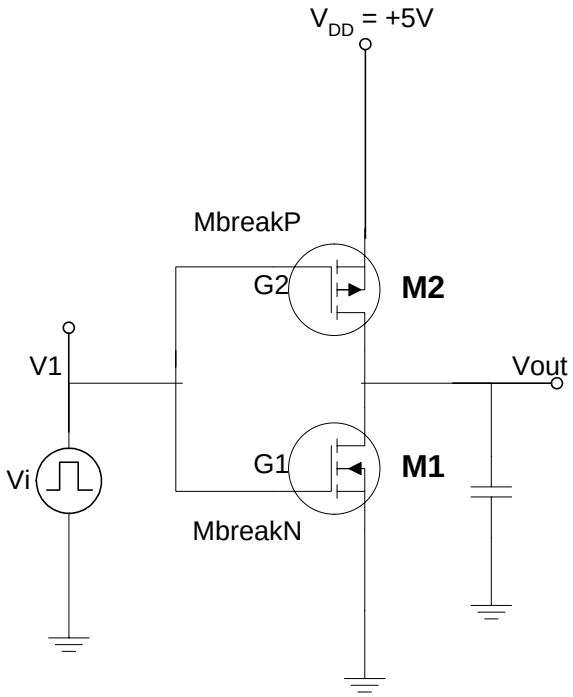


Figure 1. CMOS Inverter

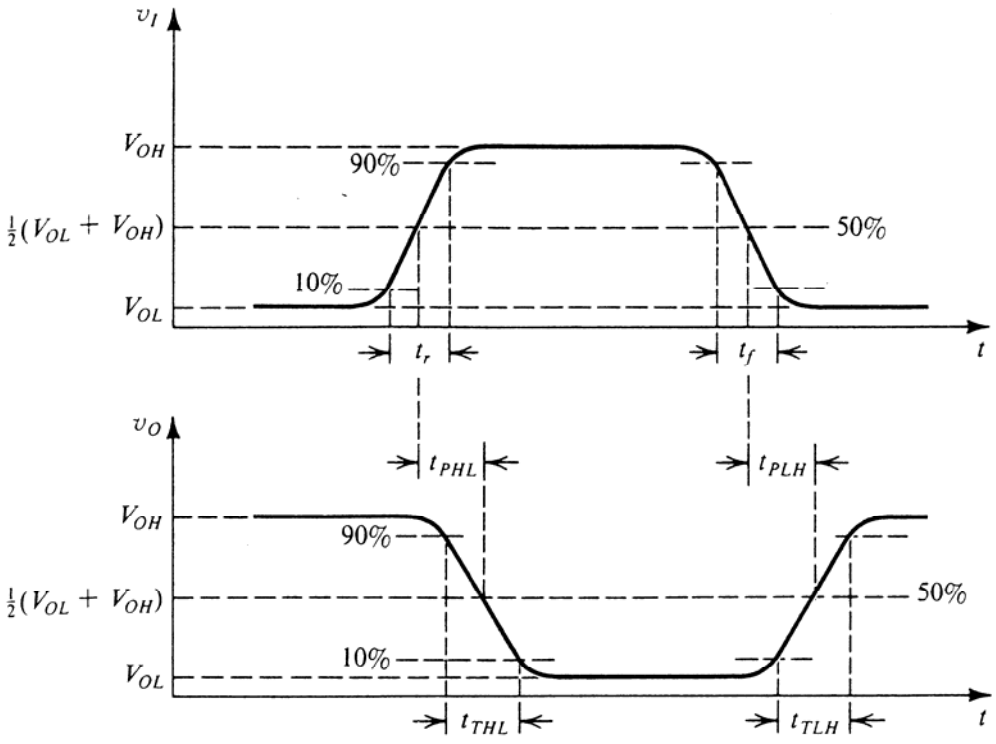


Figure 2

5. Voltage levels and noise margins

Remove the pulse source from the input terminal and connect a variable DC source. To study voltage levels and noise margins of the inverter, the input source is allowed to vary from 0 to 5V. At each input value the output voltage is recorded. A plot of output voltage versus input voltage is usually called the VTC (Voltage Transfer Characteristics). The above procedure is easily done using the *DC Sweep* analysis. (Note: The voltage increment of the input voltage should be fine enough to follow the sharp transition from HIGH to LOW in the output voltage).

From the VTC, estimate the values V_{IL}, V_{IH}, V_{OL}, V_{OH} and calculate NM_L and NM_H. Remember that V_{IL} and V_{IH} are defined at the "slope = -1" points on the VTC.

EXPERIMENTAL WORK

A. Transfer Characteristic

1. Connect the circuit shown in Figure 3. Apply a triangular wave of frequency about 1000Hz and of 10V peak-to-peak to the circuit supplied from a dc supply of 5V.
2. Use the oscilloscope to display the transfer characteristic with output applied to the Y input and the input applied to the X input. Sketch the result, noting particularly the logic levels (V_{OH}, V_{OL}, V_{IH}, V_{IL}). Note to observe the transfer characteristics use the XY format or the dual trace format on the oscilloscope (put Channel 1 on the input and Channel 2 on the output).
3. Now lower the supply voltage and note the display. Note the effect of changing the dc supply voltage on the performance of the circuit.

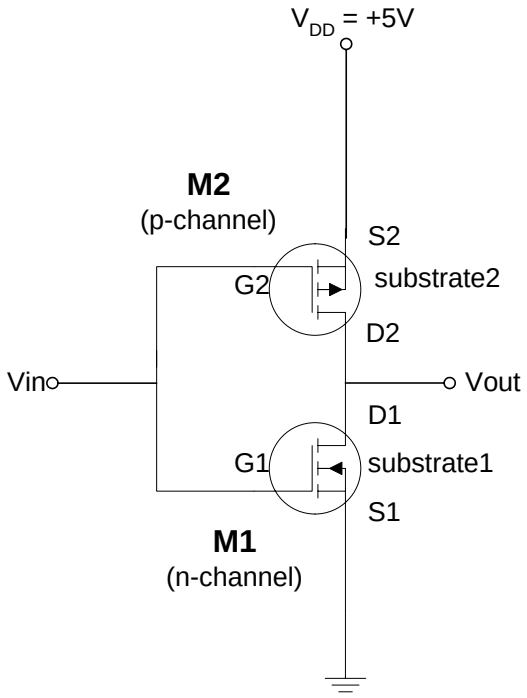


Figure 3 CMOS Inverter

B. Output Drive Capabilities

1. With the circuit supplied from 5V dc, ground the input. Now apply (to ground) resistors of 1k, 2k, 5k and 10k. Measure the output voltage in each case. Plot the output voltage versus load current.
2. Repeat step 1 but now with input voltage = 5V and the load resistors connected between the output terminal and the dc supply. Plot the output voltage versus load current.

COMPARE THE RESULTS OBTAINED IN STEPS 1 AND 2. COMMENT ON THE RESULTS.