KING FAHD UNIVERSITY OF PETROLEUM AND MINERALS
DEPARTMENT OF ELECTRICAL ENGINEERING
Electronic Circuits I - EE203

Experiment # 9

Transistor-Transistor Logic

OBJECTIVE

To study the circuit characteristics of Transistor-Transistor Logic (TTL) and to familiarize the student with the basic properties of logic circuits based on saturated bipolar junction transistors.

COMPONENTS REQUIRED

- Transistors - D2N2222 (4 No's)
- Resistors - 1KΩ, 4KΩ, 1.6KΩ, 0.13KΩ

PRELAB WORK

Using hand calculation, find the current in each branch and the voltage at each node in the circuit of Figure (1) when the input voltage is 5V. Assume β_F=100, β_R=0.01 V_{BE} =0.7 V. Keep these results in your notebook, in the laboratory you will measure these currents and voltages and compare them with your calculations.

Perform Pspice before coming to the Lab

SUMMARY OF THEORY

TTL has been the most popular circuit technology for implementing digital systems using SSI, MSI, LSI packages. At the present time, TTL continues to be used although it has certainly lost a lot of application grounds to its chief rival, CMOS.

Figure 2, shows the complete TTL gate circuit. It consists of three stages: the first transistor *Q1*, operating in the **inverse active mode**—that is, in the active mode but with the roles of emitter and collector interchanged. The driver stage *Q2*, whose function is to generate the two complementary voltage signals required to drive the totem-pole circuit, which is the third (output) stage of the gate. The totem-pole circuit in the TTL gate has two additional components: the 130Ω, resistance in the collector circuit of *Q4* and the diode D in the emitter circuit of *Q4*. The reason of including the 130Ω resistance is simply to limit the current that flows through *Q4*, especially in the event that the output terminal is accidentally short circuited to ground. This resistance also limits the supply current in another circumstances, namely, when *Q4* turns on while *Q3* is still in saturation.

Transfer characteristics

Figure 1, below shows the sketch of voltage transfer characteristics drawn in a piecewise linear fashion. The actual characteristics, is offcourse is smooth curve. We shall now explain the transfer characteristics.

Segment AB is obtained when transistor Q_1 is saturated, Q_2 and Q_3 are off, and Q_4 and D are on. The output voltage is approximately two diode drops below V_{CC}. At point B the phase slitter (Q_2) begins to turn on because the voltage at its base reaches 0.6V ($0.5+V_{CEsat}$ of Q_1).

Over segment BC, transistor Q_1 remains saturated, but more and more of its base current get diverted to its base-collector junction and into the base of Q_2, which operates as a linear amplifier. Transistor Q_4 and diode D remain on, with Q_4 acting as an emitter follower. Meanwhile the voltage at the base of Q_3, although increasing remains insufficient to turn Q_3 on (less than 0.6)

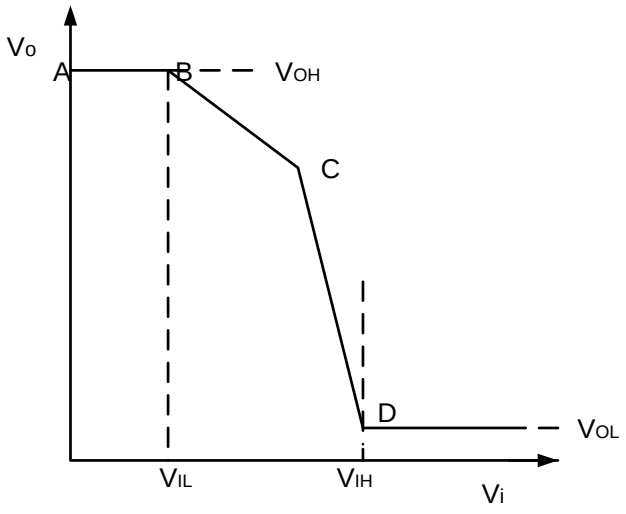

Figure 1 Voltage Transfer Characteristics

At breakpoint C Q_3 start to conduct, Q_2 & Q_4 remains in active mode and Q_1 remains saturated. The circuit behaves as an amplifier until Q_2 and Q_3 saturate and Q_4 cuts off. This occurs at point D on the transfer characteristics, which corresponds to an input voltage V_{IH}.

From the transfer characteristics curve Figure 1, (refer also Figure 2) we can determine the critical points and the noise margin as follows V_{OH} = 3.7V; V_{IL} is somewhere in the range of 0.5 V to 1.2 V, and thus a conservative estimate would be 0.5 V; V_{OL} =0.1 V; V_{IH} =1.4 V; $NM_H = V_{OH} - V_{IH}$ =2.3 V; and $NM_L = V_{IL} - V_{OL}$ =0.4 V. It should be noted that these values are computed assuming that the gate is not loaded and without taking into account power supply or temperature variations

PSPICE

1. **Circuit specifications and setup**

Implement the circuit of a standard TTL inverter (shown in Figure 2) into a PSPICE circuit file or a Schematics file. The input signal to the inverter is a continuous symmetric square pulse of maximum amplitude of 5V and minimum amplitude of 0V. The period of the pulse is 500μs. (Note: to define such an input use the *PULSE* source definition; refer to PSPICE handout. For Schematics users, the source *VPULSE* can be used. In this case make sure to change the source attributes to match the given specifications). Use transistor type *Q2N2222* for all transistors and diode type *D1N4148*. Record all your results in the table given.

2. **Input/Output waveforms**

Perform transient analysis of the circuit and observe the input and output waveforms on the same plot. Convince yourself that the inverter action is established. In the analysis, allow a number of periods to be plotted by setting appropriate parameters relative to the period of the input signal.

3. **Voltage levels and noise margins**

Remove the pulse source from the input terminal and connect a variable DC source. To study voltage levels and noise margins of the inverter, the input source is allowed to vary from 0 to 5V. At each input value the output voltage is recorded. A plot of output voltage versus input voltage is usually called the VTC (Voltage Transfer Characteristics). The above procedure is easily done using the *DC Sweep* analysis. (Note: The voltage increment of the input voltage should be fine enough to follow the sharp transition from HIGH to LOW in the output voltage).

From the VTC, estimate the values V_{IL}, V_{IH}, V_{OL}, V_{OH} and calculate NM_L and NM_H. Remember that V_{IL} and V_{IH} are defined at the "slope = -1" points on the VTC.

Results

V_{IL}	
V_{IH}	
V_{OL}	
V_{OH}	
NM_L	
NM_H	

EXPERIMENTAL WORK

A. Transfer Characteristic

1. Connect the circuit shown in Figure 2. Apply a triangular wave of 10V peak-to-peak to terminal A. Its frequency should be 1 kHz.
2. Use the oscilloscope to display the transfer characteristic with output V_0 vertically and input A horizontally. Alternately, and briefly, connect input A to +5V and then to ground to establish axes conveniently near the lower left of your screen. Sketch the result, noting particularly the logic levels (V_{OH}, V_{OL}, V_{IH}, V_{IL}). Note to observe the transfer characteristics use the XY format or the dual trace format on the oscilloscope (put Channel 1 on the input and Channel 2 on the output).
3. Now connect a 330 ohms resistor from the output to ground and then from +5V supply to output. Note briefly the changes in output transition, particularly its position on the input axis and maximum level. Remove this load.
4. Now with no load, lower the supply voltage towards ground and note the effect on the display. What is the lowest useable power supply voltage?
5. Return to the standard supply voltage of +5V, apply 5V to the input and measure the current in each branch and the voltage at each node. You will compare these measurements with your hand calculations.

Note: You may need to know β of the transistor used in the laboratory. This can be done by using the transistor curve tracer.

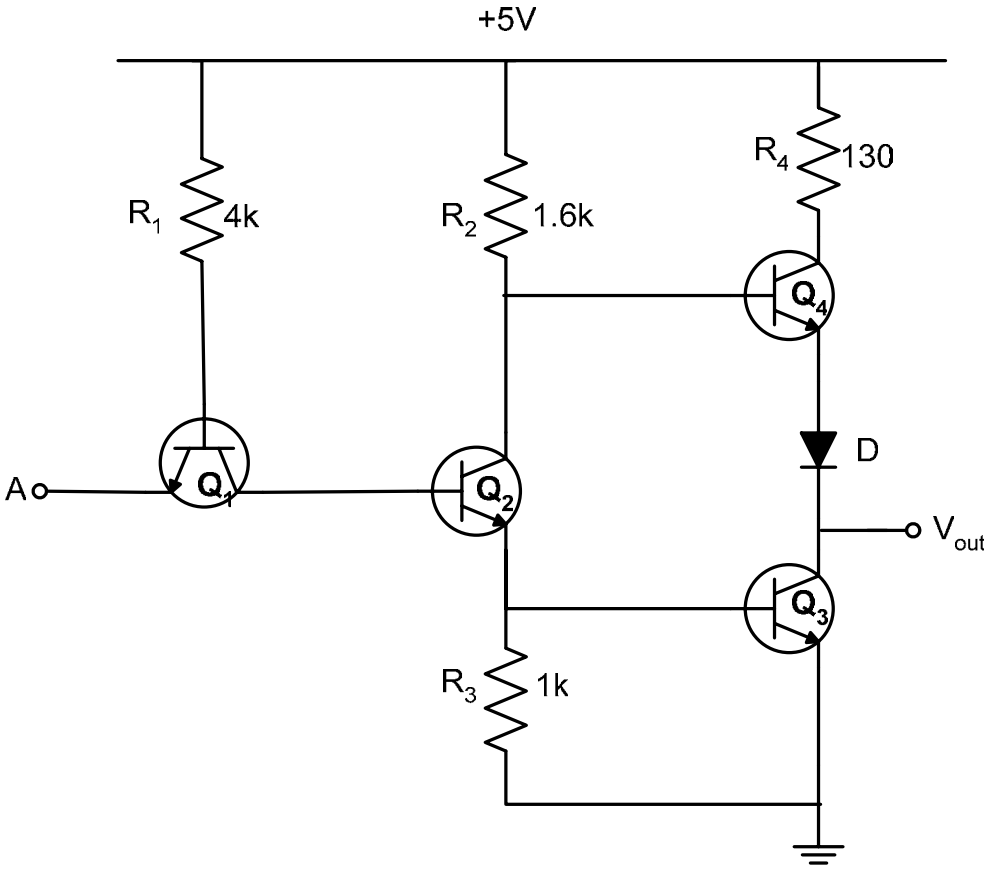

Figure 2 TTL Inverter

B. Output Drive Capabilities

1. With the circuit supplied from the standard +5V supply voltage ground the input. Now apply resistors of 2k, 1k, 500 ohms to the output. Note the output in each case. Plot the output voltage versus load resistance.
2. Repeat step 1 but now with the load connected between the output and the +5V supply. Compare the results of steps 1 and 2 and comment.

DATA SHEET

The 2N2222 is BJT, the data sheet of this can be analyzed same as 2N3904 except few facts which will be clarified below.

2N3904 and 2N2222 are intended for rather different purposes. The 2N2222 has an I_C max of 800mA (metal case, the PN2222 has less current capabilities), while the 2N3904 has something like 300mA I_C max. The 2N3904 is a higher speed and generally lower noise device. The 2N2222 is a medium-low power switch with higher input and output capacitances. The 2N3904 is a low power switch with lower noise .h_{FE} is about the same for both.

Philips Semiconductors — Product specification

NPN switching transistors — **2N2222; 2N2222A**

FEATURES

- High current (max. 800 mA)
- Low voltage (max. 40 V).

APPLICATIONS

- Linear amplification and switching.

DESCRIPTION

NPN switching transistor in a TO-18 metal package.
PNP complement: 2N2907A.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector, connected to case

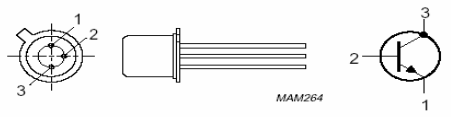

Fig.1 Simplified outline (TO-18) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	2N2222		–	60	V
	2N2222A		–	75	V
V_{CEO}	collector-emitter voltage	open base			
	2N2222		–	30	V
	2N2222A		–	40	V
I_C	collector current (DC)		–	800	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	500	mW
h_{FE}	DC current gain	I_C = 10 mA; V_{CE} = 10 V	75	–	
f_T	transition frequency	I_C = 20 mA; V_{CE} = 20 V; f = 100 MHz			
	2N2222		250	–	MHz
	2N2222A		300	–	MHz
t_{off}	turn-off time	I_{Con} = 150 mA; I_{Bon} = 15 mA; I_{Boff} = –15 mA	–	250	ns