KING FAHD UNIVERSITY OF PETROLEUM AND MINERALS
DEPARTMENT OF ELECTRICAL ENGINEERING
Electronic Circuits I - EE203

Experiment # 7

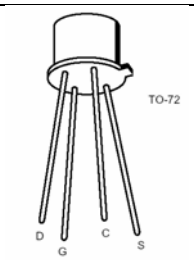
The MOSFET Small Signal Amplifier

OBJECTIVE

To study the properties of the common source MOSFET amplifier. The voltage gain, input and output resistance will be calculated both theoretically and experimentally.

COMPONENTS REQUIRED

- N-channel MOSFET 2N4351 (1)
- Resistors 5.6KΩ, 10kΩ, 100kΩ, 1Meg
- Capacitor 22 μF, (2)



MOSFET pin Configuration

PRELAB WORK

1. For the MOSFET CS amplifier circuit shown in Figure 1, assume V_t = 1.5V, K=0.5mA/V^2 and calculate the drain current I_D, and all DC voltages (V_D, V_G, V_S). Check for saturation mode operation.
2. Draw the small signal equivalent circuit and drive expressions for the amplifier voltage gain, input and output resistances.

SUMMARY OF THEORY

The MOSFET structure has become the most important device structure in the electronics industry. It dominates the integrated circuit technology in Very Large Scale Integrated (VLSI) digital circuits based on n-channel MOSFETs and Complementary n-channel and p-channel MOSFETs (CMOS). The technical importance of the MOSFET results from its low power consumption, simple geometry, and small size, resulting in very high packing densities and compatibility with VLSI manufacturing technology.

Two of the most popular configurations of small-signal MOSFET amplifiers are the common source and common drain configurations. The common source circuit is shown in Figure 1. The common sources, like all MOSFET amplifiers, have the characteristic of high input impedance. High input impedance is desirable to keep the amplifier from loading the signal source. This high input impedance is controlled by

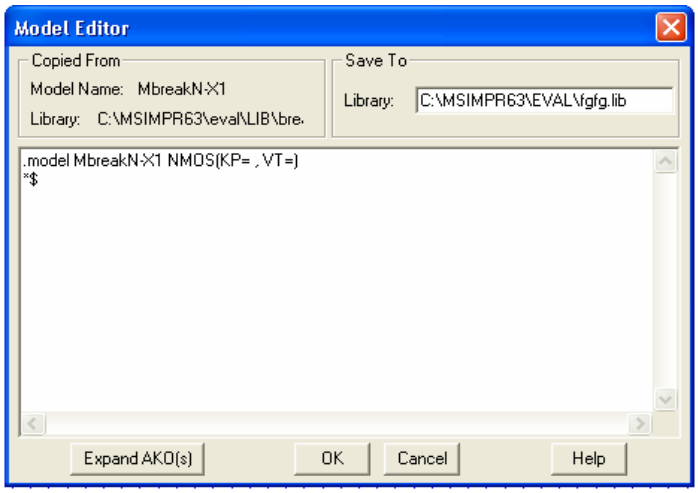
the bias resistor R_G (or bias resistors R_{G1} and R_{G2}). Normally the value of the bias resistor(s) is chosen as high as possible. However too big a value can cause a significant voltage drop due to the gate leakage current. A large voltage drop is undesirable because it can disturb the bias point. For amplifier operation the MOSFET should be biased in the saturated region of the characteristics.

The CS and CD MOSFET amplifiers can be compared to the CE and CC BJT amplifiers respectively. Like the CE amplifier, the CS amplifier has a negative voltage gain and an output impedance approximately equal to the drain resistor (collector resistor for the CE amplifier). The CD amplifier is comparable to the CC amplifier with the characteristics of high input impedance, low output impedance, and less than unity voltage gain.

PSPICE

1. Verify all Prelab calculations using SPICE. Assume $V_t = 1.5V$, $K_p = 0.05mA/V^2$, $W = 30\mu m$ and $L = 3\mu m$.

Note: To change V_t and K_p select the MOSFET (MbreaKN),. This is done by single-clicking on the transistor with the right mouse button. If it has been selected, it will turn red. Then, select "Model" from the Edit Menu. The Edit Model dialog box will appear. This box states the name of the part to be edited, along with three different methods to edit. We will select "Edit Model Instance (Model Editor)", since we want to use the Model Editor. Click that button, and you should get this error. This is just to inform us that if we change any of the parameters of the MOSFET, the model will behave differently. This is exactly what we want, so click "Okay". You should see the following:



2. Use SPICE TRAN analysis to find the maximum input voltage that can be amplified without distortion. Vary the value of R_D and notice the effect on the output. Can you find the optimum value for R_D that results in maximum symmetric output swing (clipping occurs on both sides).

You must have your SPICE output file with your hand calculations ready before you come to the lab.

EXPERIMENTAL WORK

Before you connect the circuit test the MOSFET using curve Tracer, instructor will examine you procedure

1. **DC ANALYSIS:** Connect the MOSFET CS amplifier circuit shown in Figure 1. Use a voltmeter to measure the transistor voltages (VD, VG, VS) and drain current (ID). Make sure your transistor is biased in the saturation mode for amplifier application. Compare all DC results to your prelab calculations.
2. **AC ANALYSIS:** Apply a sine wave (20mV, 10 kHz). Display both input and output signals on the oscilloscope and observe the phase shift. Measure the output voltage and compute the voltage gain.
3. Increase the input amplitude until you observe clipping in the output. Plot and label the clipped output. What is the maximum input that can be amplified without distortion (clipping)?
4. Connect a 100kΩ resistor between the voltage source and the coupling capacitor C_1. Measure the voltage gain and use the results from step 2 to deduce the amplifier input resistance R_{in}.
5. Remove the load resistor R_L, and measure the voltage gain, then deduce the amplifier output resistance R_o.

At the end of this experiment:

a) Compare all experimental results to the theoretical calculations and SPICE simulation.
b) Discuss the differences between theory and experiment.
c) Recall the BJT amplifier results and compare with the MOSFET. Which amplifier gives higher voltage gain (hint: compare g_m) and higher input resistance?

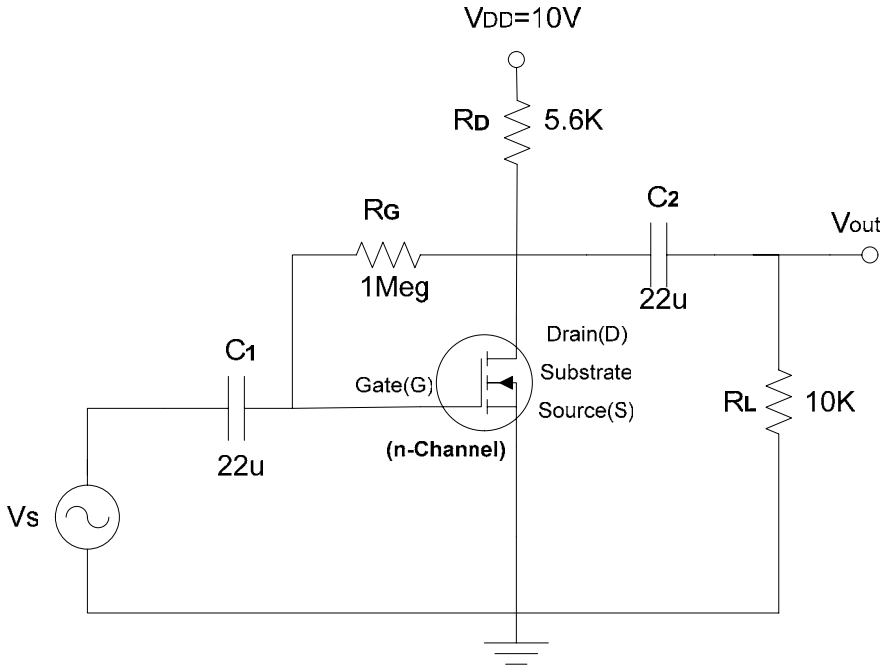


Figure 1 MOSFET Amplifier

DATA SHEET

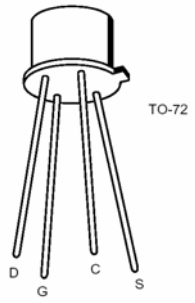
The 2N2351 MOSFET used in this Experiment is an 25 V (drain-source breakdown voltage), N-Channel enhancement mode MOSFET general purpose amplifier/switch MOSFET. For the enhancement-type MOSFET, the gate to source voltage must be positive and no drain current will flow until V_{GS} exceeds the positive threshold voltage V_T. V_T is a parameter of each particular MOSFET and is temperature sensitive. This parameter sensitivity to temperature is one reason for establishing a stable dc bias. The 2N4351 MOSFET data sheet lists the minimum and maximum values of V_T as 1 V and 5 V respectively (Refer Partial data sheet). y_{fs} is g_m which is a very important parameter to determine minimum and maximum voltage gain. Other parameters are very clear from the data sheet.

2N4351

FEATURES

- **Low ON Resistance**
- **Low Capacitance**
- **High Gain**
- **High Gate Breakdown Voltage**
- **Low Threshold Voltage**

PIN CONFIGURATION



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ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-Source Voltage or Drain-Body Voltage 25V
Peak Gate-Source Voltage (Note 1) . . . . . ±125V
Drain Current 100mA
Storage Temperature Range . . . . . -65°C to +200°C
Operating Temperature Range . . . . . -55°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Power Dissipation 375mW
Derate above 25°C . . . . . 3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
2N4351	Hermetic TO-72	-55°C to +150°C
X2N4351	Sorted Chips in Carriers	-55°C to +150°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
BV_{DSS}	Drain-Source Breakdown Voltage	25		V	I_D = 10µA, V_{GS} = 0
I_{GSS}	Gate Leakage Current		10	pA	V_{GS} = ±30V, V_{DS} = 0
I_{DSS}	Zero-Gate-Voltage Drain Current		10	nA	V_{DS} = 10V, V_{GS} = 0
$V_{GS(th)}$	Gate-Source Threshold Voltage	1	5	V	V_{DS} = 10V, I_D = 10µA
$I_{D(on)}$	"ON" Drain Current	3		mA	V_{GS} = 10V, V_{DS} = 10V
$V_{DS(on)}$	Drain-Source "ON" Voltage		1	V	I_D = 2mA, V_{GS} = 10V
$r_{DS(on)}$	Drain-Source Resistance		300	ohms	V_{GS} = 10V, I_D = 0, f = 1kHz
$\lvert y_{fs} \rvert$	Forward Transfer Admittance	1000		µS	V_{DS} = 10V, I_D = 2mA, f = 1kHz
C_{rss}	Reverse Transfer Capacitance (Note 2)		1.3	pF	V_{DS} = 0, V_{GS} = 0, f = 1MHz
C_{iss}	Input Capacitance (Note 2)		5.0		V_{DS} = 10V, V_{GS} = 0, f = 1MHz
$C_{d(sub)}$	Drain-Substrate Capacitance (Note 2)		5.0		$V_{D(SUB)}$ = 10V, f = 1MHz
$t_{d(on)}$	Turn-On Delay (Note 2)		45	ns	
t_r	Rise Time (Note 2)		65		
$t_{d(off)}$	Turn-Off Delay (Note 2)		60		
t_f	Fall Time (Note 2)		100		