

Experiment 4

Kirchhoff's Laws

Introduction

Kirchhoff's voltage law (KVL) states that the algebraic sum of all voltages around any closed path equals zero. The Kirchhoff's current law (KCL) states that the algebraic sum of all the currents at a node is zero (current entering a node has opposite sign to the current leaving the node). This experiment studies these two laws using *Multisim Electronics Workbench*, then with actual hardwired circuit.

Objectives

1. Voltage current measurement in a dc circuit
2. Verification of Kirchhoff's voltage and current laws.

Materials

One dc power supply
One multimeter
Assorted carbon resistors

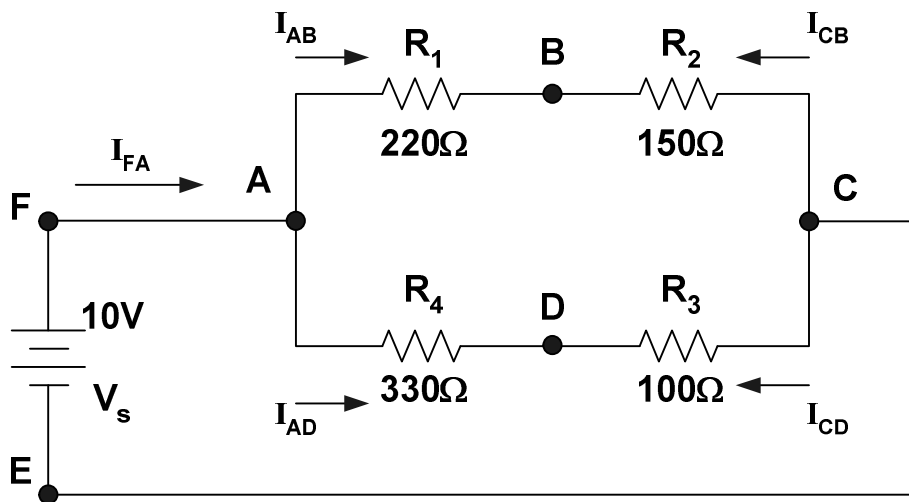


Figure 1: Resistive circuit

Procedure

1. Construct the circuit shown in Figure 1 using *Multisim Electronics Workbench*.
2. Measure the voltages V_{AB} , V_{BC} , V_{AD} , V_{DC} , V_{BD} , and V_{AC} . Enter the values in Table 1. Note the polarities of the voltages.
3. Measure the currents I_{AB} , I_{CB} , I_{AD} , I_{CD} and I_{FA} and enter the values in Table 2. Note the polarity (sign) of the currents.

4. Calculate the voltages around the following loops and record them in Table 4.

ABCEFA, ABDA, BDCB, ABCDA

5. Verify KCL by adding the currents at nodes A, B, C, D. Enter your results in Table 3.

6. Construct the circuit in Figure 1 with hardware components. Repeat steps 2-5. Enter your results in Tables 1-4. Considering the Workbench results as the base compute the percentage errors.

Table 1: Voltage measurement

| | V_{AB} | V_{BC} | V_{AD} | V_{DC} | V_{BD} | V_{AC} |
|------------------|----------|----------|----------|----------|----------|----------|
| Workbench | | | | | | |
| Hardwired | | | | | | |
| % Error | | | | | | |

Table 2: Current measurement

| | I_{AB} | I_{CB} | I_{AD} | I_{CD} | I_{FA} |
|------------------|----------|----------|----------|----------|----------|
| Workbench | | | | | |
| Hardwired | | | | | |
| % Error | | | | | |

Table 3: Sum of currents at nodes

| | A | B | C | D |
|-------------------|----------|----------|----------|----------|
| Workbench | | | | |
| Experiment | | | | |
| % Error | | | | |

Table 4: Voltages around loop

| | ABCEFA | ABDA | BDCB | ABCDA |
|-------------------|--------|------|------|-------|
| Workbench | | | | |
| Experiment | | | | |
| % Error | | | | |

Answer the following Questions:

1. Do the experimental and theoretical values of voltages and currents agree?
2. Give possible reasons for any discrepancies.
3. Are KVL and KCL verified?
4. Give reasons for any discrepancies.

Any other observations or comments