EXPERIMENT #10: FLIP-FLOPS AND THEIR APPLICATIONS

OBJECTIVES:

- Investigate the operation of various latches and flip-flops
- Implement and test two important applications of flip-flops

Equipment and ICs:

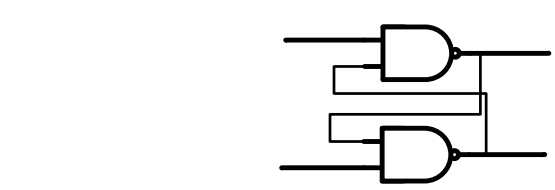
- Mini-Lab ML-2001 lab station
- 2 - IC 7474 Dual D-type flip-flops
- 2 - IC 7476 Dual J K-type flip-flops
- 1 – IC 7400 Quad NAND gates

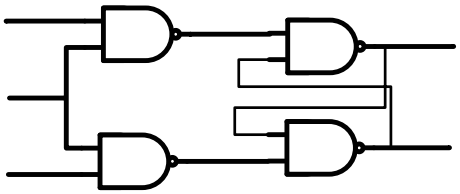
Introduction:

A flip-flop is a binary storage device capable of storing one bit of information. It is a basic building block for counters, registers, and other sequential control logic.

A flip-flop circuit can maintain a binary state indefinitely until directed by an input signal to switch state. The major differences among various types of flip-flops are in the number of inputs they possess and in the manner in which the inputs affect the binary state. The most basic types of flip-flops operate with signal levels and are referred to as ***latches***. The latches are the basic circuits from which all flip-flops are constructed but they are not practical for use in synchronous sequential circuits. Basic latches are shown in Figure 1.

The problem with a latch circuit is that it responds to a change in the level of a clock pulse. As long as the pulse remains in this level, any changes in the data input will change the output and the state of the latch. The result is an unpredictable situation since the state of latches may keep changing for as long as the clock pulse stays in the active level. Flip-flop circuits are constructed in such a way as to make them operate properly when they are part of a sequential circuit that employs a common clock. The key to the proper operation of a flip-flop is to trigger it only during a signal transition. A clock pulse goes through two transitions from 0 to 1 (positive-edge transition) and from 1 to 0 (negative-edge transition). See Figure 2.





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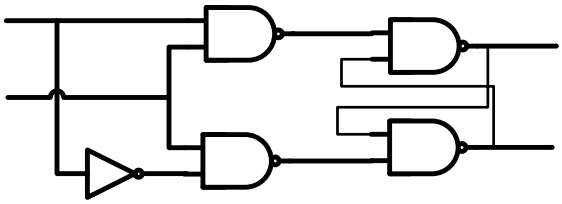

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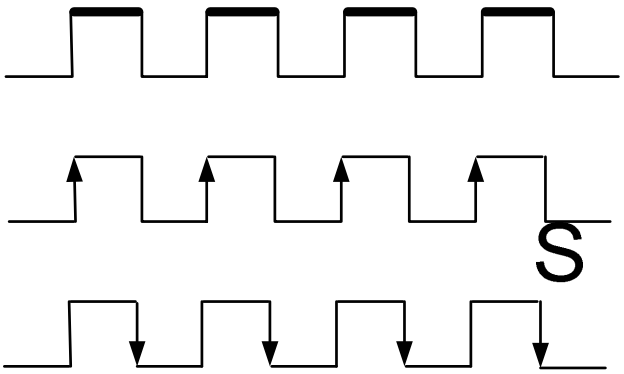
A clock pulse goes through two transitions from 0 to 1 (positive-edge transition) and from 1 to 0 (negative-edge transition).



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The two most widely flip-flops used in the design of sequential circuits are the D-Type flip-flop and the JK-Type flip-flop. The D-type flip-flop finds applications in registers and certain types of memories and the JK-type flip-flop is used in building counter circuits.

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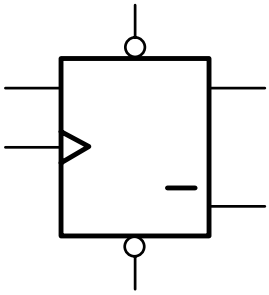
Part 1: Basic Flip-flops

Investigate the operation of D FF and JK FF. The graphic symbol with direct inputs Preset and Clear and the function table of each flip-flop is given in Figure 3.



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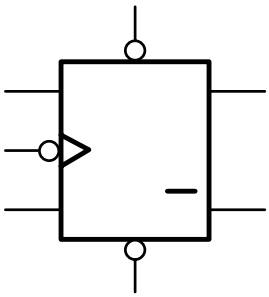

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Pre-lab Work:

1. Read sections related to Flip-flops and latches from your text book.
2. Read from the section **Introduction** of this lab.

D SET Q

CLR Q

- positive-edge re

Lab Work:

1. Connect one D FF on the proto-board from IC 7474 which has two D-type Flip-flops.
    a. Connect input D to a DIP switch.
    b. Connect PRESET and CLEAR inputs to two DIP switches.
    c. Connect CLK input to a pulser-button.
    d. Connect outputs Q and Q' to two indicator lamps.

2. Verify the operation of the D FF as shown in the function table in Figure 3 for the D FF.
    a. Apply clock pulses to the FF by pushing the pulser-button.
    b. Verify that output Q changes only when a clock pulse is applied while PRESET and CLEAR inputs are held at logic-1.
    c. Verify that the PRESET and CLEAR inputs can directly change the output at any time regardless of input D and clock. (PRESET is used to set Q to logic-1 and CLEAR is used to clear Q to logic-0).
    d. Verify that for normal operation of the flip-flop PRESET and CLEAR inputs must be at logic-1.
    e. Verify that output Q = D for all values of D.

3. Connect one JK FF on the proto-board from IC 7476 which has two JK-type Flip-flops.
    a. Connect input J and K to two DIP switches.
    b. Connect PRESET and CLEAR inputs to two DIP switches.
    c. Connect CLK input to a pulser-button.
    d. Connect outputs Q and Q' to two indicator lamps.

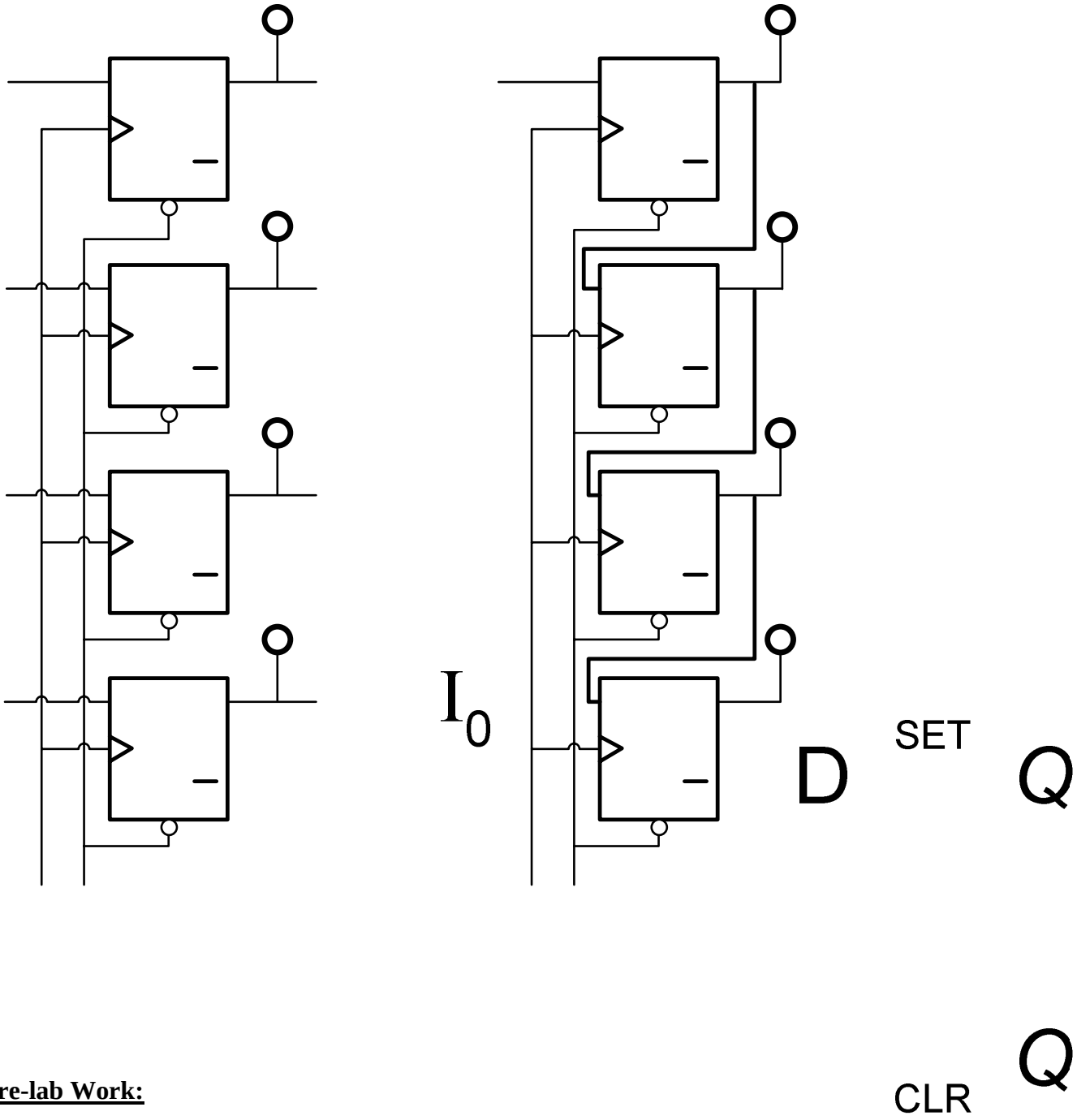
4. Verify the operation of the JK FF as shown in the function table in Figure 3 for the JK FF.
    a. Apply clock pulses to the FF by pushing the pulser-button.
    b. Verify that output Q changes only when a clock pulse is applied while PRESET and CLEAR inputs are held at logic-1.
    c. Verify that the PRESET and CLEAR inputs can directly change the output at any time regardless of inputs J and K, and clock. (PRESET is used to set Q to logic-1 and CLEAR is used to clear Q to logic-0).
    d. Verify that for normal operation of the flip-flop PRESET and CLEAR inputs must be held at logic-1.
    e. Verify that JK = 0 1 clears Q to 0, JK = 1 0 sets Q to 1, JK = 1 1 complements Q, and JK = 0 0 does not change Q.

5. Record your results and observations for the lab report.

OBSERVATIONS:

Part 2: D FF Applications

Construct a 4-bit register and a 4-bit shift register using D FFs. A 4-bit register with parallel load and a 4-bit serial shift register are shown in Figure 4.



Pre-lab Work:

1. Draw and simulate the circuits shown in Figure 4 in LogicWorks. Include your LogicWorks drawing in the pre-lab report.

2. Connect the PRE-SET input of each flip-flop to +5V in LogicWorks

Lab Work:

4-bit Register

1. Connect the 4-bit register (as shown in Figure 4) on the proto-board using two 7474 ICs.
    a. Connect the D inputs (I_0, I_1, I_2, and I_3) of the four D FFs to four DIP switches.
    b. Connect PRESET inputs of all flip-flops together.
    c. Connect CLEAR inputs of all flip-flops together.
    d. Connect Clock inputs of all flip-flops together.
    e. Connect PRESET and CLEAR inputs to two DIP switches.
    f. Connect Clock input to a pulser-button.
    g. Connect the Q outputs (A_0, A_1, A_2, and A_3) of the four D FFs to four indicator lamps.

2. Verify the operation of the 4-bit register.
    a. Clear the 4-bit register first by toggling CLEAR input to 0 and back to 1.
    b. Apply clock pulses to the FF by pushing the pulser-button.
    c. Verify that outputs of the four FFs change only when a clock pulse is applied while PRESET and CLEAR inputs are held at logic-1.
    d. Verify that for normal operation of the register PRESET and CLEAR inputs must be at logic-1.
    e. Observe the indicator lamps and verify that output A = input I.

4-bit Shift Register

3. Now connect the output of the first flip-flop to the input of the second, output of the second flip-flop to the input of the third, and output of the third flip-flop to the input of the fourth (as shown for the 4-bit Shift Register in Figure 4).

4. Keeping only the input of the first FF connected to a DIP switch; remove the wires connecting the inputs of the other flip-flops to other DIP switches.

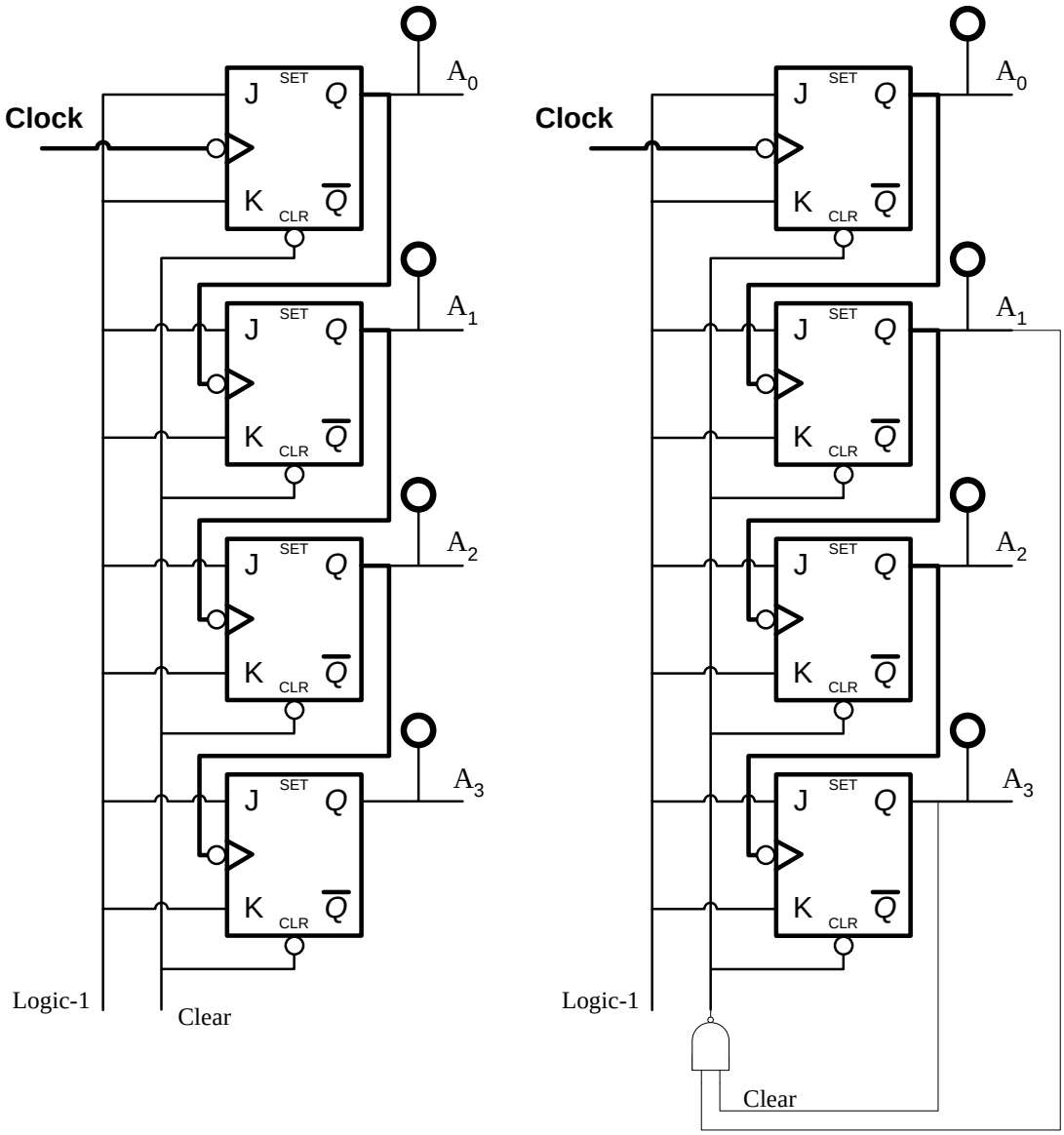
5. Do not change any other connections.

6. Verify the operation of the 4-bit shift register.
    a. Clear the 4-bit shift register first by toggling CLEAR input to 0 and back to 1. Set serial input SI to logic-1.
    b. Apply clock pulses to the FF by pushing the pulser-button.
    c. Verify that outputs of the four FFs change only when a clock pulse is applied while PRESET and CLEAR inputs are held at logic-1.
    d. Verify that for normal operation of the register PRESET and CLEAR inputs must be at logic-1.
    e. Observe the indicator lamps and verify that the input SI shifts through the first flip-flop to the last flip-flop in four clock cycles.

7. Record your results and observations for the lab report.

Part 3: JK FF Applications

Construct a 4-bit ripple counter and a BCD counter as shown in Figure 5.



4-bit Ripple Counter **BCD Counter**

Figure 5: JK FF used in counters

Pre-lab Work:

1. Draw and simulate the circuits shown in Figure 4 in LogicWorks. Include your LogicWorks drawing in the pre-lab report.

2. Connect the PRE-SET input of each flip-flop to +5V in LogicWorks

Lab Work:

4-bit Ripple Counter

1. Connect the 4-bit ripple counter (as shown in Figure 5) on the proto-board using two 7476 ICs.
    a. Connect the JK inputs of the four D FFs to 5v (logic-1).
    b. Connect PRESET inputs of all flip-flops together.
    c. Connect CLEAR inputs of all flip-flops together.
    d. Connect PRESET and CLEAR inputs to two DIP switches.
    e. Connect the Q outputs (A_0, A_1, A_2, and A_3) of the four JK FFs to four indicator lamps.
    f. Connect Clock input of the first FF to a pulser-button.
    g. Connect the output of the first flip-flop to the **Clock** input of the second, the output of the second flip-flop to the **Clock** input of the third, and the output of the third flip-flop to the **Clock** input of the fourth (as shown for the 4-bit ripple counter in Figure 5).

2. Verify the operation of the 4-bit register.
    a. Clear the 4-bit counter first by toggling CLEAR input to 0 and back to 1.
    b. Apply clock pulses to the FF by pushing the pulser-button.
    c. Verify that outputs of the four FFs change only when a clock pulse is applied while PRESET and CLEAR inputs are held at logic-1.
    d. Observe the indicator lamps and verify that the counter value increments by 1 for every clock pulse applied. Verify that the counter counts from 0 to F.

BCD Counter

3. Now disconnect the CLEAR input from the DIP switch.

4. Connect the output of the second and fourth flip-flop to the inputs of a 2-inout NAND gate as shown in Figure 5.

5. Connect the output of the above NAND gate to the CLEAR input removed in Step 3 above.

6. Do not change any other connections.

7. Verify the operation of the BCD counter.
    a. Apply clock pulses to the FF by pushing the pulser-button.
    b. Verify that outputs of the four FFs change only when a clock pulse is applied while PRESET input is held at logic-1.
    c. Observe the indicator lamps and verify that the counter value increments by 1 for every clock pulse applied. Verify that the counter counts only from 0 to 9.

8. Record your results and observations for the lab report.