Analysis of Harmonic Reduction for Synchronized Phase-shifted Parallel PWM Inverters with Current Sharing Reactors

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***Abstract*--Renewable energy sources are quickly becoming incorporated into increasingly distributed electrical utility grids. An ever present issue when interfacing these sources is that of harmonic distortion reduction at the inter-tie point. One very interesting approach to reduce harmonic distortion is to synchronize power transistor operation for inverters operating in parallel.**

In this paper, a rarely employed technique for harmonic reduction using synchronized phase shifted parallel PWM inverters with current-sharing reactors is presented and analyzed. Using the technique presented inverter output distortion can be reduced significantly, for example total harmonic reduction can be reduced typically in half using just two synchronized phase-shifted parallel inverters (our simulation and experimental studies indicate that even smaller distortion reduction factors can be achieved).

We present analyses for two and three phase-shifted inverters operated in parallel employing current sharing reactors. Our analyses consider the impact of a wide range of phase-shift delays on net output total harmonic distortion, with the phase-shift delay from zero to one entire cycle of the fundamental component. Some results are expected, such as a dramatic increase in distortion when the fundamental components between multiple inverters tend to cancel out, on the other hand it is interesting to observe a leveling-off, and gradual, smooth increase in the distortion reduction factor over a significant portion of the phase-shift delay variable.

***Index Terms*--multiple inverters, pulse width modulation, distortion reduction.**

I. Nomenclature

fs	frequency of the modulating sine wave
fc	frequency of carrier wave form
Tc	the period of carrier signal
N	number of parallel inverters
Ts	period of the modulating sine wave
M	modulation index

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II. Introduction

THE operation of two or more inverters in parallel is possible in situations where two or more DC sources are available (e.g. fuel cells, solar cells, some wind based sources, microturbine or other sources with a DC link). Parallel operation of multiple inverters has been identified as means to reduce both relative and net harmonic distortion of an inverter system [1, 2]. In more recent years, this idea has received renewed interest as alternative energy sources are being connected to electric utility grid systems. Many approaches employ an output reactor so that a voltage source inverter can be connected to the grid and at the same time provide current waveform control. Techniques have been suggested on how to minimize such reactors [3]. Another set of researchers have suggested randomizing the operation of the power transistor gating functions so as to obtain uncorrelated harmonic spectra among the parallel inverters [4].

With the increasing interest in renewable energy sources, we expect increased attention on parallel operation of multiple inverters. Indeed paralleling inverters is useful in itself for a number of reasons; where modularity and redundancy are some of the key points, paralleling may lead to other benefits such as ease of maintenance through operation of identical units, scalable designs, increased reliability through redundancy, etc, without over sizing the single inverter. One shortcoming is that many of these paralleling techniques depend on relatively large inter-tie inductors applied between inverter and the point of common coupling, to suppress the possible circulating currents and provide current control. It has also been pointed out that the need for communication between the inverter control systems is not desirable [4]. These issues will need to be addressed in the future. At the present time we are hopeful that parallel operation of inverters will be employed more in the near future. We offer here analyses where we explore the impact of the phase-shift delay parameter on the total harmonic distortion of a parallel multiple inverter system.

In this paper, a computer-aided design and analysis using PSpice and Simulink/Matlab as well as the experimental results for a single inverter, two synchronized shifted parallel inverters with an optimum phase delay of Tc/4, and three synchronized shifted parallel inverters with an optimum phase delay of Tc/6 is presented, where Tc is the carrier period.

Fig. 1 illustrates a typical full-bridge single-phase H-bridge inverter. In this paper, we operate such an inverter employing fixed-frequency open-loop double-edge naturally sampled pulse width modulation (NSPWM), in which the triangular high frequency carrier waveform is compared against the reference low frequency sine waveform (60 Hz). With this type of carrier, both phase-legs of the H-bridge are modulated which considerably improves the harmonic performance of the pulse train [5]. In this paper we set the carrier to sine reference frequency ratio, fc/fs, to be 15 and set the modulation index M to be 0.9 with two and three parallel inverters using 3-level NSPWM. Fig. 2 depicts this technique to generate the unfiltered voltage waveform for the single-full bridge. In this technique, both phase legs use a common carrier but they are modulated with inverted sine reference waveforms.

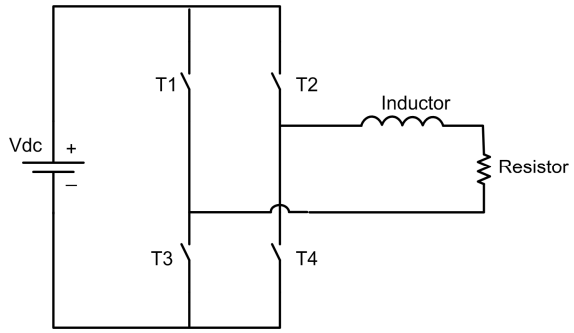


Fig. 1 Typical single-phase full-bridge (H-bridge) inverter.

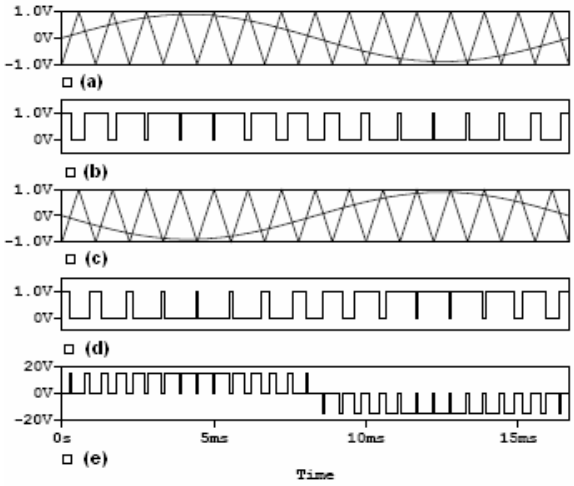


Fig. 2 Three-level NSPWM process for one single-phase inverter
(a), (c) Identical carriers with inverted references
(b), (d) Gating signals for the phase legs
(e) Unfiltered voltage waveform at the output of one inverter

III. Optimum Phase Delay

Fig. 3 demonstrates the proposed implementation of full-bridge inverters operated in parallel. Shown are three inverters but any number of inverters can be used. Note that the DC sources are isolated and output reactors are employed. The inverter reactors together with the grid inductance act as a summing network for the current outputs of the multiple inverters.

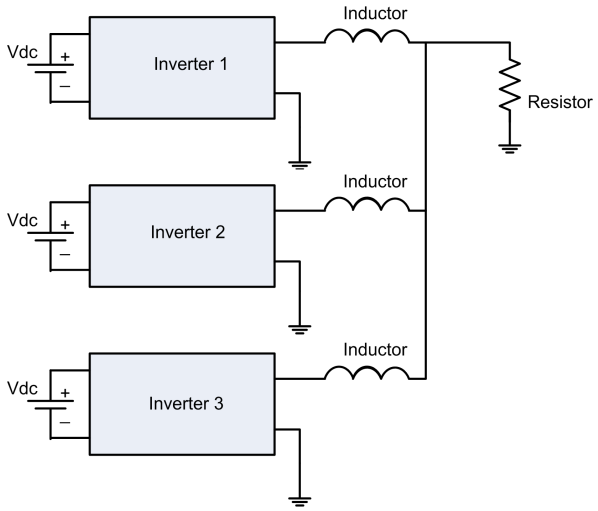


Fig. 3 Typical Schematic diagram of multiple full-bridge PWM invertors in parallel

A main contribution of this paper is finding the optimum phase shift between parallel inverters with 3-level PWM that yields minimum total harmonic distortion (THD). In this paper, a phase-shift delay sweep has been carried out, involving two and three parallel inverters with varying phase-shift delays. Fig. 3 shows the THD obtained when the second inverter is operated with a phase-shift delay swept from 0 to Ts (where Ts is the modulating reference period, ie, 1/60 s = 16.67 ms) relative to the first inverter in a two parallel inverters configuration. The optimum phase-shift delay that yields the lowest total harmonic distortion is found to be Tc/4 where Tc is the carrier period, in this case 1.11ms (ie, the second inverter lags the first one by Tc/4), as can be seen in the inset illustrating how no delay produces a THD of 15.74% but at the optimal phase-shift delay of Tc/4 = 0.278ms, the THD is 4.58% for one set of operation parameters and reactor and load parameters (c.f. Table 1 below).

Fig. 4 shows the THD obtained when the second and third inverters phase-shift delays are swept simultaneously between 0 and Ts in a three parallel inverters configuration. The optimum phase shift that yields lowest total harmonic distortion in this case is found to be Tc/6 (ie, the second inverter lags first one by Tc/6, and third inverter lags first by 2*(Tc/6)).

The symmetries in the plots are readily understood from the paralleling of the converters, and the peak distortion (greater than 100% THD) occurs for a 60Hz fundamental that is approaching zero amplitude.

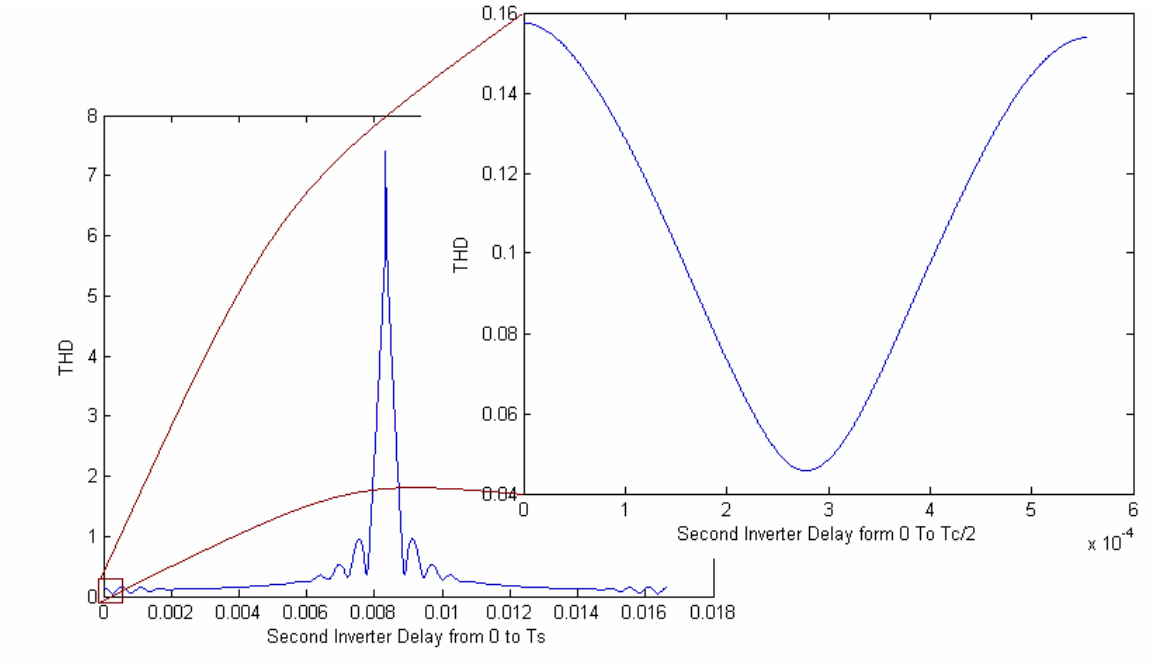


Fig. 4 THD versus phase-shift delay for 2-parallel inverters, with M=0.9 and fs/fc=15.

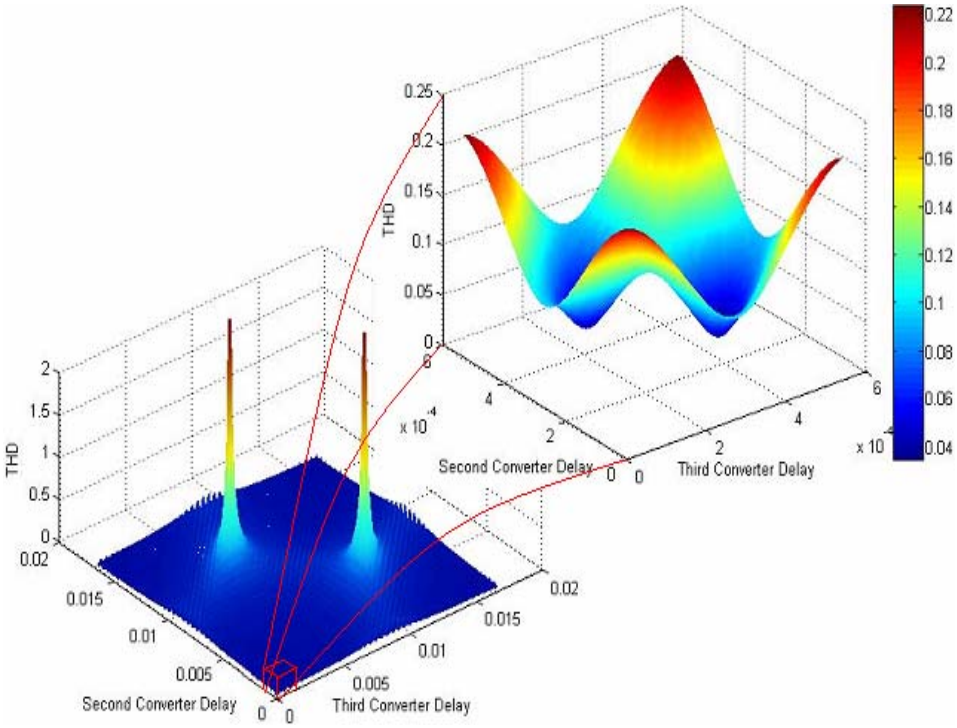


Fig. 5 THD versus phase-shift delay for 3-parallel inverters with M=0.9 and fs/fc=15.

IV. Simulation Results

To understand the harmonic reduction effect of

parallel synchronized inverter operation, we considered the switching strategy for two phase-shifted full-bridge inverters as illustrated in Fig. 6. In Fig. 6 (a and b) we see the output pulses of each NSPWM 3-level operated inverter. The second inverter is operated with the same set of pulses as the first inverter but delayed by Tc/4 as can be seen on the figure. Using current sharing filter inductors, the unfiltered effective resultant Vre at the common point of all parallel inverters, can be expressed for the general case of N parallel inverters as:

$$V_{re} = [V_{out(1)} + V_{out(2)} + V_{out(3)} + \quad + V_{out(N)}] / N \qquad (1)$$

With $V_{out(i)}$ being the unfiltered output of the i^{th} inverter (between the inverter legs of Fig. 1). Note, we refer, Vre in eqn. (1) as the effective resultant for the N parallel inverters since this voltage does not exist in the system (ie, there is no voltage waveform such as shown in Fig. 6 (c) in the parallel inverter system). Still, it is insightful to define effective resultant waveform as in eqn. (1).

Fig. 6 (c) shows this unfiltered effective resultant for the case of two parallel inverters. Note that there are five voltage levels in the effective unfiltered load voltage waveform for each cycle of the fundamental (0V, 1/2 Vdc, Vdc, -1/2 Vdc, - Vdc) compared to three in the case of one inverter. In the case of three synchronized parallel inverters (see Fig. 5), the unfiltered effective resultant output voltage waveform will have seven voltage levels per cycle of the fundamental waveform (0V, 1/3 Vdc, 2/3 Vdc, Vdc, –1/3 Vdc, –2/3 Vdc, – Vdc) as shown in Fig. 7. As more inverters are employed, the unfiltered effective resultant load voltage waveform becomes more sinusoidal-like with an effectively higher carrier frequency (ie, N x fc) and with the number of levels equal 2N+1.

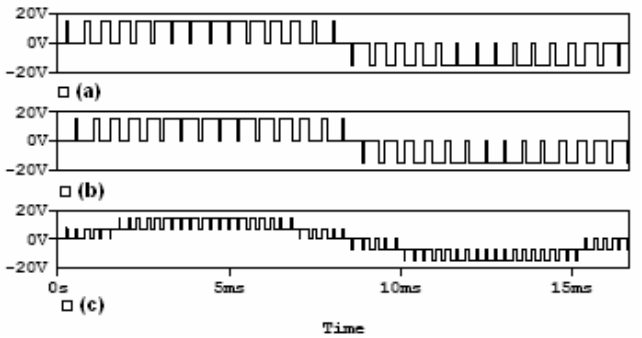


Fig 6 Two parallel inverters operation:
(a) Unfiltered effective voltage at the output of the first inverter
(b) Unfiltered effective voltage at the output of the second inverter
(c) The effective resultant output voltage waveform for two parallel inverters

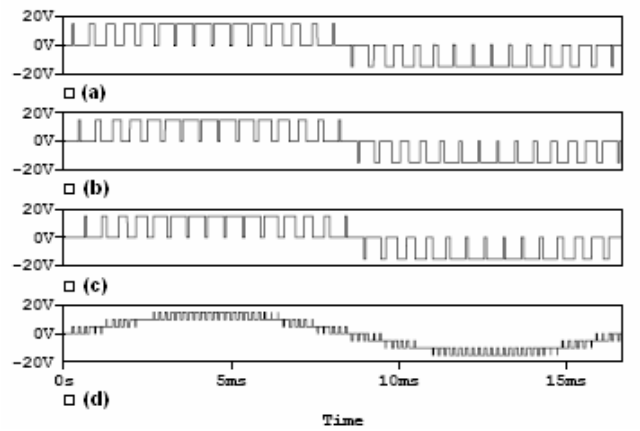


Fig 7 Three parallel inverters operation:
(a) Unfiltered effective voltage at the output of the first inverter
(b) Unfiltered effective voltage at the output of the second inverter
(c) Unfiltered effective voltage at the output of the third inverter
(d) The effective resultant output voltage waveform for three parallel inverters.

Fig. 8 shows the filtered output voltage waveform for the three cases being investigated, and Table 2 shows the corresponding THD, we can see that the THD decreases as N increases.

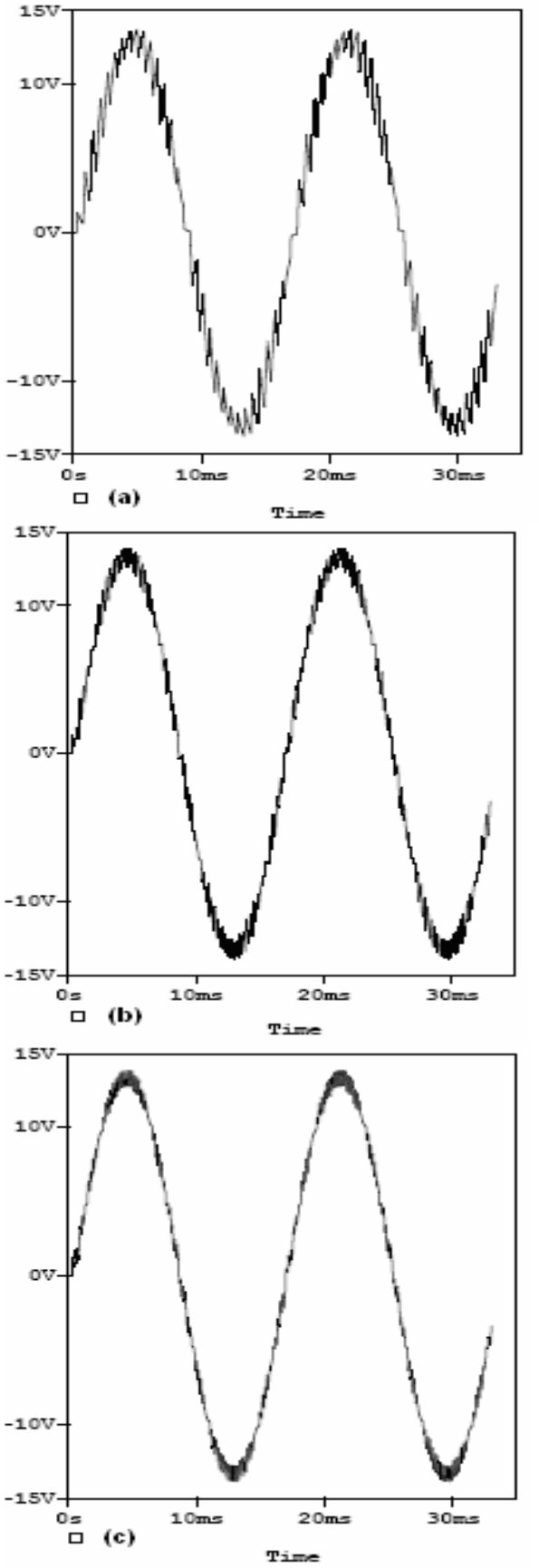


Fig. 8 (a) Filtered output voltage of single inverter
(b) Filtered output voltage of two parallel inverters
(c) Filtered output voltage of three parallel inverters

V. Experimental Results

A low voltage laboratory prototype was built to validate the simulation results. Fig. 9 illustrates the block diagram of the implemented scheme. Table 1 lists the parameters used in the experiment. The PWM gating signals were generated using the Microchip Technology's PIC 16F877. The synchronization unit consists of an external clock source to drive the OSC1/CLKIN pin, and a master Reset connected to the MCLR pin.

Fig. 10 shows the experimental wave shapes obtained, and Table 2 shows the corresponding THD results obtained which support our numerical simulation results.

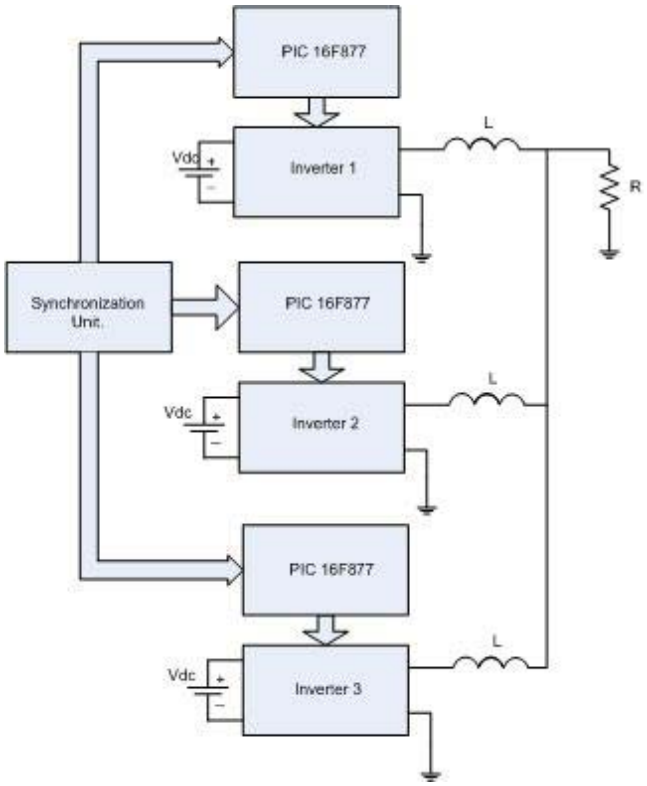
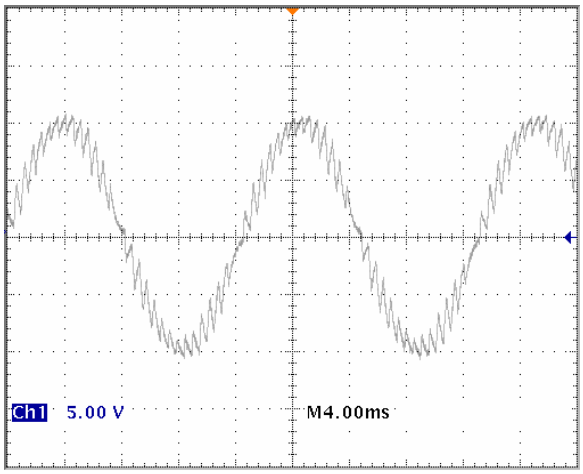


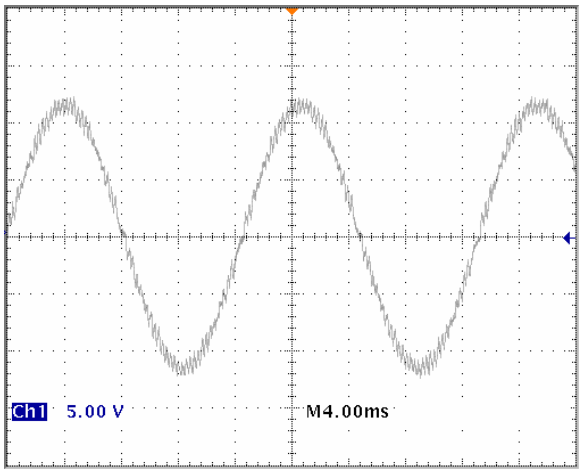
Fig. 9 Block diagram implementation of the proposed technique

Table 1
Parameters used in the Experiment

Parameter	Value
fs/fc	15
M	0.9
Vdc	15 V
L	100 mH
R	180 Ω



(a)



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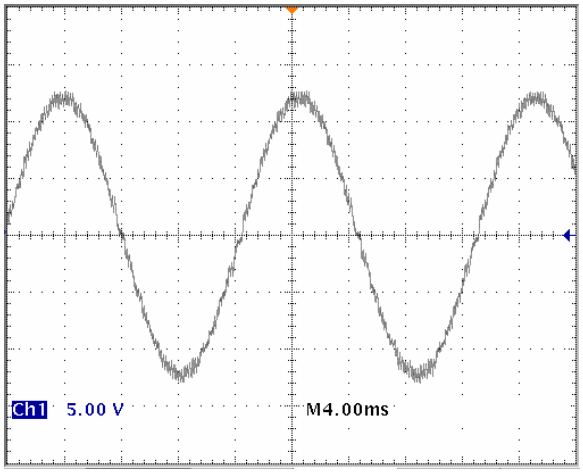

(c)

Fig. 10 Experimental load voltage waveforms
(a) case of only one inverter
(b) case of two synchronized inverters
(c) case of three synchronized inverters

Table 2
THD Result Obtained[1].

	One Converter	Two Converters	Three Converters
Matlab Results	8.28%	4.58%	3.45%
Pspice Results	8.32%	4.44%	3.32%
Experimental Results	10.91%	5.17%	3.84%

VI. Conclusions

In this paper, a new technique for harmonic reduction using synchronized phase shifted parallel PWM inverters with current-sharing reactors was presented. The optimum phase shift was introduced that results in a considerable THD reduction. Experimental results verified and validated our simulation results. Therefore, the proposed technique is a potential candidate for the power electronics interface of renewable energy systems.

VII. References

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[1] The difference in results between Matlab and PSpice are due to the fact that in calculating the THD PSpice uses only the first 100 harmonics while Matlab includes all the harmonics up to the Nyquist frequency (half the sampling frequency).