Increased Number of Voltage Steps for Cascaded H-bridge Multilevel Inverters using 3-level Operation in each Half-cycle

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***Abstract*-- Some renewable energy sources provide dc electrical energy. For example, photovoltaic sources, fuel cells, and the rectified output of some turbine driven sources, produce dc voltages. If the outputs of these devices are to be fed to the ac power grid, a power interface is required. The cascaded H-bridge multilevel inverter is an electronic interface that can connect multiple dc energy sources to an ac power system. In this paper we present an analysis to demonstrate the degree to which the total harmonic distortion of a cascaded H-bridge can be reduced by having some H-bridges provide 3-level voltage contributions in each half-cycle of the stepped output voltage waveform. Such 3-level operation produces a very significant distortion reduction, the result of an increase in the number of steps.**

***Index Terms*—multilevel inverters, cascaded H-bridge, distortion reduction.**

I. Nomenclature

V_i dc input voltage of the i^{th} H-bridge
Va_i voltage output function of time for the i^{th} H-bridge
v(t) voltage output function of time for cascaded H-bridge
m the number of H-bridges in the cascaded circuit
θ_k cascaded H-bridge step angle for the k^{th} transition
ω_o angular frequency of fundamental output voltage
n index number for the harmonic components

II. Introduction

THERE has been increased interest in recent years in methods that can be used to reduce harmonics produced by inverters supplied by renewable energy sources. For those renewable sources where a dc link is available, such as solar, fuel cell or some turbine based sources, it may be of value to employ a multilevel inverter. Some background on these converters is given in [1,2] with renewable issues discussed in [3]. Some methods to increase the number of voltage steps in the output waveform of a cascaded H-bridge topology are addressed in [4,5]. We discuss here, one technique where the number of voltage levels of the output waveform can be increased significantly using 3-level H-bridge operation during each half-cycle of the output voltage waveform [5].

The block diagram of a cascaded H-bridge multilevel inverter is shown in Fig. 1. An H-bridge switching circuit is associated with each dc voltage source to produce three possible voltage levels at each H-bridge output: zero volts, positive and negative polarity of the source voltage associated with that H-bridge. That is to say, if the an H-bridge has a voltage input for the i^{th} H-bridge of V_i, the switches in the H-bridge can be controlled to produce a voltage Va_i whose value can be 0, V_i or $-V_i$. The output voltages of the H-bridges are added subsequently to generate the output waveform v(t). Due to the nature of the output voltage generating process, the addition of the voltages produces a stepped waveform. This waveform is close to a sine wave in shape but will have harmonics that are inherent in a stepped waveform. The total harmonic distortion (THD) in this case is a measure of how far the resultant output is from a pure sine wave.

In this paper a rarely used technique is discussed to enhance the performance of the conventional multilevel H-ridge inverter by increasing the number of steps of this waveform without increasing the number of contributing dc sources. This is achieved by using both positive and negative voltage polarities of the contributing voltages in each half-cycle of the output voltage [5]. In the case of two voltage sources used in the present approach, the resultant output has the same harmonic components as the waveform generated by the conventional cascaded H-bridge approach having four dc voltage sources. Increasing the number of steps of the generated waveform will also improve switching performance of the circuit by decreasing the off-voltage imposed on the power switching devices.

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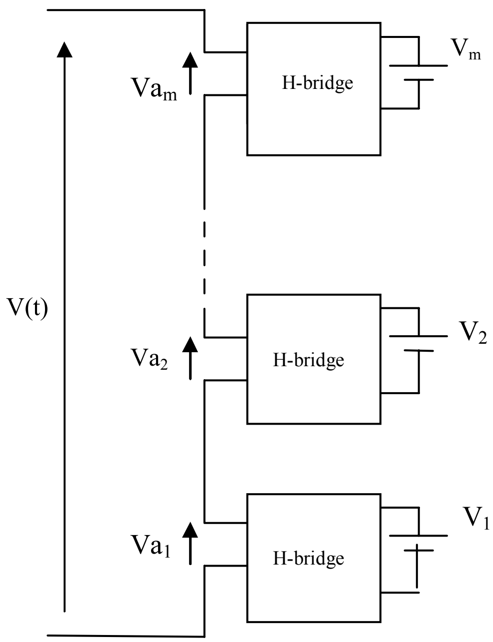

Fig. 1 Block diagram of a cascaded H-bridge inverter

III. Basic Equations and Simulation Example

Consider a cascaded H-bridge inverter system having *m* dc voltage sources with voltages V_i, i=1, 2, .., *m*, where each has a distinct voltage value:

$$V_i \neq V_j \quad \text{for all i and j.} \quad (1)$$

The voltage V_1 designates the lowest voltage; V_2 is the next higher one, and so forth. V_m is the highest value of the dc voltage sources in the system. This means:

$$V_i < V_{i+1} \quad \text{for all i} \quad (2)$$

Another assumption imposed on the values of the dc voltages is:

$$V_1+V_2+..+V_{i-1} < V_i \quad \text{for all i.} \quad (3)$$

Another assumption requires that the difference between voltages does not equal any of the voltages of the DC sources. For example,

$$V2\text{-}V1 > V1$$

Also,

$$V_3\text{-}V_2\text{-}V_1 > V_2+V_1$$

In general this idea can be formulated as follows

$$V_j\text{-}(V_1+V_2+...+V_{j-1})>V_1+V_2+...+V_{j-1} \text{ for all j} \quad (4)$$

The conventional multilevel cascaded H-bridge adds the voltages of the different dc sources one after the other at subsequent time intervals to approximate the shape of the sine wave. The total number of levels achieved is *2m+1*. To increase the number of levels in the conventional approach, *m* has to be increased. For the presented scheme [5] the number of levels is increased without the need for increasing the number of dc voltage sources. This is achieved by switching on and off the appropriate voltage sources with the appropriate polarity at the proper time to increase the number of steps of the stepped waveform as much as possible. The number of levels possible with the presented approach is 3^m. To illustrate how the technique works, the case of two voltage sources is presented here. In this case there are two dc voltage sources V_1 and V_2 used to produce the output ac waveform. Each voltage source is connected via an H-bridge switching circuit to be a component of the resultant ac output voltage waveform (sometimes currents circulate in an H-bridge to contribute zero volts). The output of the H-bridge connected to V_1 for instance will give at its output $+V_1$, $–V_1$ or 0v. The outputs of the two H-bridges are added together to produce the resultant output ac waveform. As shown in Fig. 2, the conventional approach will generate the output waveform by adding successively the voltages coming from the H-bridges with the same polarity in each half-cycle. This procedure will result in having a total of 5 levels (2*m*+1=5 for *m*=2) in the output waveform for the two voltage sources of the example. It is noted that V_1 is equal to V_2 in this specific (ie, conventional) case of Fig. 2.

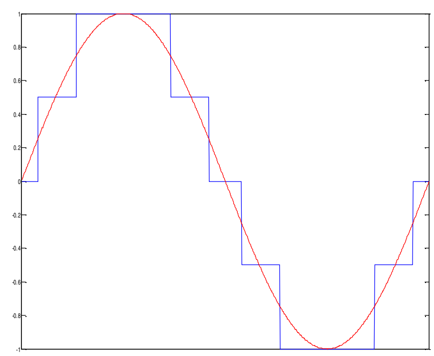

Fig. 2 Output waveform for the conventional approach with two equal dc voltage sources.

Fig. 3 depicts the condition for the approach discussed here. By applying equations (1) to (4), the half-cycle of the output staircase waveform can be composed of four steps in each quarter cycle. The values of V_1 and V_1+V_2 are already used in the conventional approach and they are used here also. The two new voltage values of the output waveform are V_2-V_1 and V_2. These two newly added values will make the total number of levels in one complete cycle of the output waveform equal to 9 (3^m=9 for *m*=2). This is equivalent to having four dc voltage sources in the conventional approach (2*m*+1=9 for *m*=4). The value of V_2 was chosen in this case to be $3V_1$ to make the voltage steps equal in magnitude, but this is not a requirement. In fact, it would be worthwhile investigating non-equal step values.

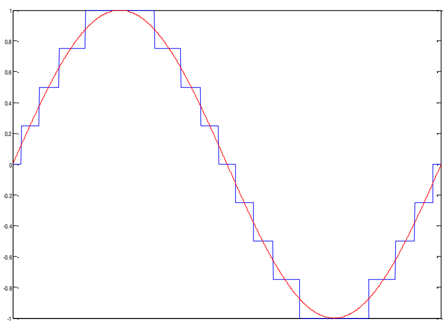

Fig. 3. Output waveform for the presented approach having only two voltage sources.

IV. Fourier Analysis

Consider Fig. 2 where there are two transitions of the output voltage waveform in the first quarter cycle. The angles at which these two transitions take place can be denoted as θ_1 and θ_2. The equation for the Fourier series expansion of the output voltage waveform given two dc sources, V_1 and V_2, is given as,

$$v(t)=\Sigma\{V_1[\cos(n\theta_1)]+V_2[\cos(n\theta_2)]\}\{4\sin(n\omega_0 t)/n\pi\},\quad n=1, 3, 5, 7, \ldots \qquad (5)$$

where the even harmonics are zero.

The corresponding Fourier coefficients are,

$$H(n)=\{4/n\pi\}\{V_1[\cos(n\theta_1)]+V_2[\cos(n\theta_2)]\},\quad n = 1, 3, 5, 7, \ldots \qquad (6)$$

This equation will be similar for the case of more than two voltage sources, ie, V_1, V_2, V_3, etc. The voltage source values will be multiplied by the cosine terms whose arguments are the angles of transition step, namely,

$$H(n)=\{4/n\pi\}\{V_1[\cos(n\theta_1)]+V_2[\cos(n\theta_2)]+V_3[\cos(n\theta_3)]+..\},\quad n=1, 3, 5.. \qquad (7)$$

In the waveform of Fig. 3 the four transitions at which the step takes place in the first quarter cycle can be denoted as θ1, θ2, θ3 and θ4. By comparing the shape of the waveforms in Fig. 2 and Fig. 3 and the value of H(n) given by equation (7) one can deduce a strategy for calculating the spectrum of such waveforms. In equation (7) the cosine term is multiplied by the value of the 'step' in the waveform, and the argument of the cosine term is *n* multiplied by the angle at which this 'step' takes place. According to this argument the harmonics of the waveform of Fig. 3 can be written as follows,

$$H(n)= \{4/n\pi\}\{(V1)[\cos n\theta 1]+ ((V2-V1)-V1)[\cos n\theta 2]+ (V2-(V2-V1))[\cos n\theta 3]+((V1+V2)-V2)[\cos n\theta 4]\},\quad n=1, 3, 5\ldots$$

In this equation the values between small brackets (.) represent the values of the step voltage at the specified transition angles. Simplifying the above equation one obtains,

$$H(n)=\{4/n\pi\}\{V_1[\cos(n\theta_1)-2\cos(n\theta_2)+\cos(n\theta_3)+\cos(n\theta_4)]+V_2[\cos(n\theta_2)]\},\quad n=1, 3, 5.. \qquad (8)$$

The spectra of both approaches are shown in Fig. 4 and Fig. 5 respectively for the case of two voltage sources. In the conventional approach of Fig. 4 the total harmonic distortion (THD) is 17.56%. The THD for the presented approach shown in Fig. 5 is 9.37%. As seen, considerable reduction in THD is achieved with this approach.

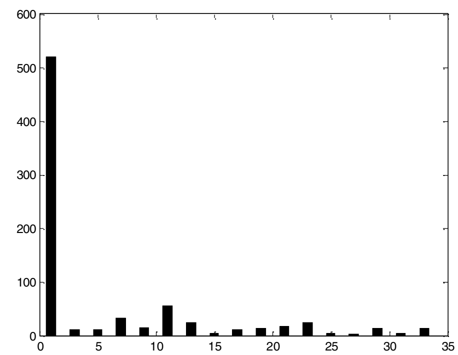

Fig. 4 Fourier coefficient magnitudes of the output waveform for the conventional approach given two dc sources (5 levels in the waveform)

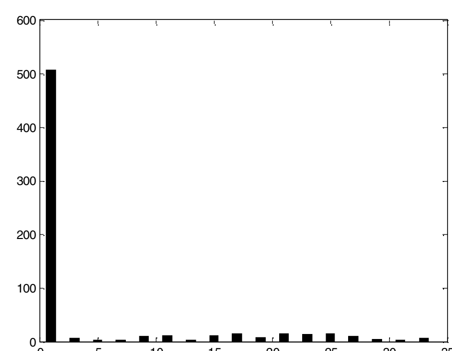

Fig. 5 Fourier coefficient magnitudes of the output waveform for the presented technique given two dc sources (9 levels in the waveform)

V. Experimental Results

The output waveform and its spectrum of a practical implementation for the presented technique using two dc voltage sources are shown in Fig. 6 and Fig. 7 respectively. The values of the dc sources were chosen to be 6V and 18V. To generate the same waveform using the conventional approach, one would need four dc voltage sources of 6V each.

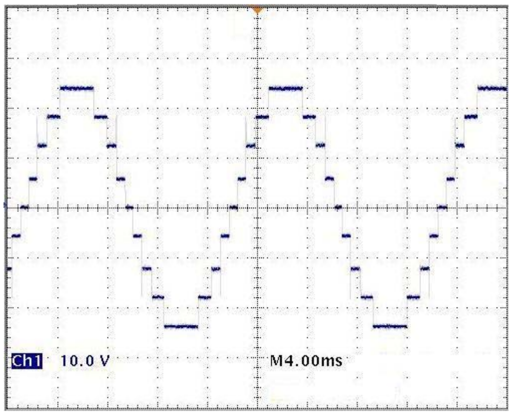

Fig. 6 Practical output waveform for multilevel inverter using the presented approach with only two voltage sources (9 levels in the waveform)

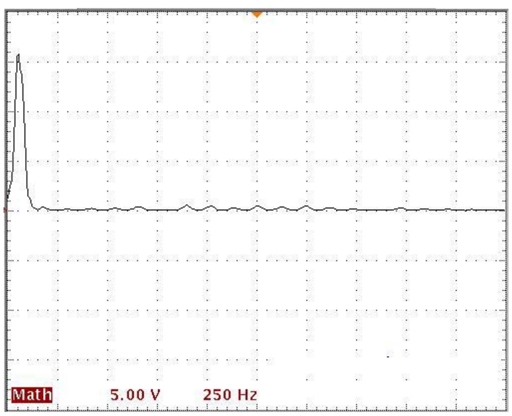

Fig. 7 Spectrum of the practical nine level stepped waveform of Fig. 6

VI. Discussion

We note, as others have observed as well, that in the case of two voltage sources half the number of dc sources are required for the presented technique compared to conventional cascaded H-bridge operation to obtain the same number of levels in the ac output voltage waveform. This translates into 3^m levels in the ac output voltage waveform compared to $2m+1$ levels for conventional operation, where m is the number of dc sources.

For the example given in this paper, we have chosen equal step values in the resultant ac output voltage waveform by selecting $V_2 = 3V_1$ but this is not a requirement. It may be worthwhile in the future to investigate the effect of non-equal step sizes on harmonic reduction.

Note also that the dc sources must permit current reversal for significant periods of time unlike the conventional approach, an issue that also should be further investigated in the future.

VII. Conclusions

In this paper we have formalized the requirements of cascaded H-bridge operation with 3-level H-bridge output voltage in each half-cycle to reduce harmonics dramatically in the output ac waveform. These requirements are given in equations (1) to (4). For equal step sizes, we derived the optimal firing angles to produce minimum total harmonic distortion. The approach is demonstrated with Matlab simulations and verified experimentally in the case of a cascaded H-bridge with two dc sources. For the examples presented, where there are two dc sources, the total harmonic distortion is reduced approximately in half (ie, from 17.6% to 9.4%) corresponding interestingly to an increase in the number of ac levels by roughly a factor of two, ie, increasing from five levels for conventional cascaded H-bridge control, to nine levels for the technique analyzed in this paper.

VIII. References

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