**COE 444 - Internetwork Design and Management**
**Fall 2004 (Term 041)**

# Homework 4
# - Solution -

Date: Thursday, November 4, 2004

**Q1.**

**a.** If full meshing is required among n nodes, then how many circuits are needed?

**n(n-1)/2**

**b.** A collection of five X.25 Packet switch exchanges (PSEs) are to be connected. Between every two PSEs the designer may assign a 64 Kbps line or no line. If it takes 100 ms to generate and evaluate each topology, how much time would be required to inspect all of them and select the one that best matches the expected load and delay requirements?

**Number of circuits in a full meshed topology of 5 nodes is: (5*4)/2 = 10**

**There are two options for each circuit (a 64 Kbps line or no line) → There are $2^{10}$ different possible topologies.**

**Therefore $2^{10}$ * 0.1 sec = 102.4 sec is required to inspect all topologies.**

**Q2.** Answer the following review questions from the "Cisco Internetwork Design" handout:

- Chapter 2 (1→ 7)
- Chapter 3 (1, 2, 3, 6)
- Chapter 4 (4)

**4.4. A key characteristic of a VLAN is that every VLAN represents a separate broadcast domain.**

**(Check the lecture notes and reading material for Solution of the other problems)**

**Q3.** A good enterprise network should follow a structured hierarchical design model consisting of three tiers (i.e., layers). Name these 3 tiers, and state the main design rule for each one.

**Q4.** Hierarchical design guidelines state that chains and backdoors must be avoided. Draw an example of each type.