Experiment 2

Designing the Bus System

2.1 Background

The 8086 CPU has 16 data lines and 20 address lines. The CPU uses time multiplexing for the address, data, and some status lines. The CPU generates the addresses A0-A15 on lines AD0- AD15 and A16-A19 on lines AS16-AS19 during clock T1. This event is indicated by a bus control signal ALE. During T2, T3, and T4 the CPU uses the AD0-AD15 to transfer data, i.e. as data bus. Demultiplexing of the AD lines requires latching of the addresses by using some integrated latches (e.g. 74LS373 octal latches). The latched addresses will then be used as address bus during clocks T2, T3, and T4.

The 74LS373 octal latch is a simple level-triggered D flip-flops with two control lines: *Output Control* (OC) and *Latch Enable* (G). As long as the Latch Enable (G) is high, the outputs of the D flip-flops follow their inputs. When G goes low, the flip-flops latch (save) the input signals. The output control line (OC) can be used to place the eight latches in either a normal logic state (high or low logic levels), or a high-impedance state.

2.2 Objective

To provide a demultiplexed data and address buses for the 8086 CPU through the use of the 74LS373 octal latches

2.3 Equipment

- The prototype-board that already includes an 8086 microprocessor with clock generator,
- TTL 74LS373 octal latches, and
- Multimeter

2.4 Procedure

1. Review the function of the 74LS373 octal latch (Appendix). Identify its input and output lines as well as the control signals available on this chip.

2. Each group discuss and give solutions to the following issues:

    a. What are the AD and AS lines that must be demultiplexed?

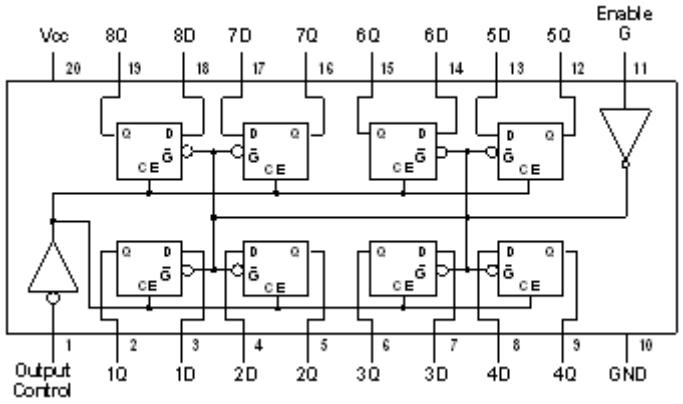
    b. The number of needed octal latches.

    c. What should be connected to control lines of the 74LS373 octal latch (i.e. G and OC).

3. Each group present their design of the demultiplexed bus to the lab instructor for validation. The proposed design must be completely defined on a working map, and the same map must be used in the wiring and debugging. The design must show what should be connected to the Latch Enable (G) and Output Control (OC) lines.

4. Once the design is validated, the group can start wiring based on the working map.

5. After completing the wiring, each group must carry out visual and electrical testing of the connections (e.g. using multimeters) as well as doing necessary corrections.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Enable G
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Output Control
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2Q
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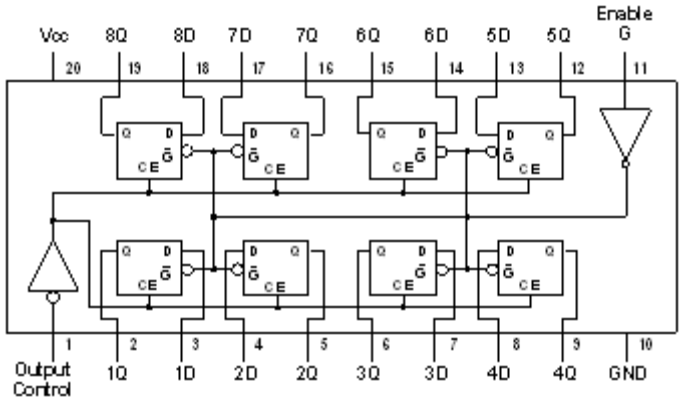
3D
4D
4Q
GND


Vcc
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Output Control
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2Q
3Q
3D
4D
4Q
GND