COE 200, Term 041

Fundamentals of Computer Engineering

HW# 8

Q.1. The following equations give the average propagation delay (in pico-seconds, i.e. 1E-12 seconds) of logic gates as a function of their Fan_{in} (i.e. the number of inputs, e.g. an AND gate with a Fan_{in} of 3 is a 3-input AND gate):

AND gate delay = $100 + 100*Fan_{in}$ pico-seconds,
OR gate delay = $200 + 200*Fan_{in}$ pico-seconds,
XOR gate delay = $250 + 250*Fan_{in}$ pico-seconds;

1. Find the worst case delay of an 8-bit Ripple Carry Adder (RCA)
2. Find the worst case delay of a 4-bit Carry Look-ahead Adder (CLA)
3. Find the adder size where the RCA becomes faster than the CLA (i.e. has less delay)

Q.2. Using ***minimum*** number of gates and Full-Adders design a circuit that multiplies an 8-bit number (X) by 10.
(Hint: 10*X = 8*X + 2*X)

Q.3. Implement a 4-to-16 Decoder using the minimum number of 2-to-4 decoders with enable inputs. If the resulting 4-to-16 Decoder is to be provided with an enable input En, show the modified circuit.

Q.4. Implement the following functions using minimum-sized Decoders and minimum number of extra gates:

a. F(X,Y,Z) = XY + Z
b. F(A,B,C,D) = D(A` + B)
c. F(X,Y,Z) = X`(Y` + Z`) + YZ`
d. F(X,Y,Z) = X`(Y` + Z`) + XZ
e. F(A,B,C) = A`
f. F(A,B,C,D,E) = 1
g. F(A,B,C,D,E,G,H) = 0
h. $F(X,Y,Z) = \sum (0,3,5,6)$, $d(X,Y,Z) = \sum (1,2,4,7)$
i. $F(A,B,C,D) = \Pi(1,7,9,13,15)$

Q.5. Construct a 5-to-32 line decoder with four 3-to-8 line decoders with enable input and one 2-to-4 line decoder.

Q.6. A Combinational circuit is defined by the following three Boolean functions:

$F_1(X, Y, Z) = X`Y` + XYZ`$
$F_2(X, Y, Z) = X` + Z$
$F_3(X, Y, Z) = XY + X`Y`$

Design the circuit with a 3x8 decoder, four 2-input OR gates, and an inverter.