EXPERIMENT 8

8. Time Multiplexing

8.1 Objectives

- Application on multiplexers
- Time multiplexing four different digits on the four seven-segment displays.

8.2 Overview

In the previous lab we used four seven-segment displays to display a single digit. If two or more distinct digits are to be displayed, then *time-multiplexing* is employed. In the context of this experiment, time multiplexing simply means that every one of the four seven-segment displays is enabled for a fixed amount of time, then disabled and another one is enabled for the same amount of time, and this process continues in a circular manner.

8.3 Design Specifications

You need to design a quad four-to-one multiplexer. This multiplexer has four input buses, each bus has four lines (D, C, B, and A), and one output (four line bus). It should have two select lines S1 and S0. The multiplexer function as follows:

If *S1S0=00* ***then***

Output=A

Elseif *S1S0=01* ***then***

Output=B

Elseif *S1S0=10* ***then***

Output=C

Elseif *S1S0=11* ***then***

Output=D

End

After that, you are going to design a full time multiplexing circuit that allows you to display four different digits on the four seven-segment displays using the quad four-to-one multiplexer

8.4 Pre-Lab

- You are required to bring the schematic of the previous experiment completed and error free.

8.5 In-Lab

8.5.1 Quad Four-to-One Multiplexer

1. On a new sheet design a macro for a quad four-to-one multiplexer, call it Q4-1MUX. You can utilize the quad two-to-one multiplexer available in the Spartan library (X74_157) see Figure 8.1. .
2. Show your schematic to the lab instructor.

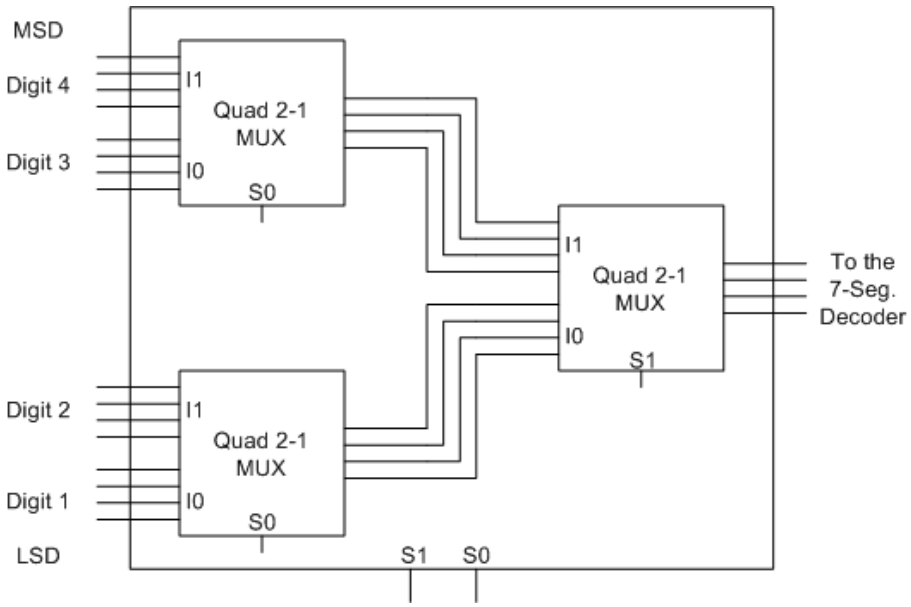

Figure 8.1: Quad 4-1 Multiplexer.

8.5.2 Time Multiplexing the Four Seven-Segment Displays.

3. Import the time multiplexing design of the previous experiment. You are going to build a macro of it in the following steps.
4. Replace the four switches with the quad four-to-one multiplexer macro you just built.
5. Select lines of the multiplexer should be connected such that if the two-to-one decoder enables the least significant seven-segment display, multiplexer output should be ***Digit 1***, and if the decoder enables the most significant seven-segment display, multiplexer output should be ***Digit 4***.
6. Add four AND gates between the four decoder outputs and the four enabling pads of the four seven-segment displays. The second input of these four AND gates is to be connected to four enabling signal to allow the user to selectively enable/disable any of the four seven-segment displays. See Figure 8.2.
7. To save power you need to add a global enable signal that allows the user to disable all the internal components of your design (multiplexer, two-to-one decoder, and two bit counter).

8. Create a macro of the design. It should look similar to MUXED7SEG macro given in Figure 8.3. The CLK input should provide the macro with the pre-calculated REF_RATE.
9. To test your MUXED7SEG macro, build a schematic similar to Figure 8.3. The least significant display should show zero as its input bus is connected to GND. On the other hand, the most significant display should show F as its input bus is connected to Vcc. The second and third lest significant displays should show the value of switches (SW5 to SW8) and (SW1 to SW4) respectively. Buffers are added because you can not give two names to the same line.
10. Download your design.
11. Verify its functionality. Make sure that when you press on any of the push buttons its corresponding display is turned OFF.
12. Demonstrate your work to the lab instructor.

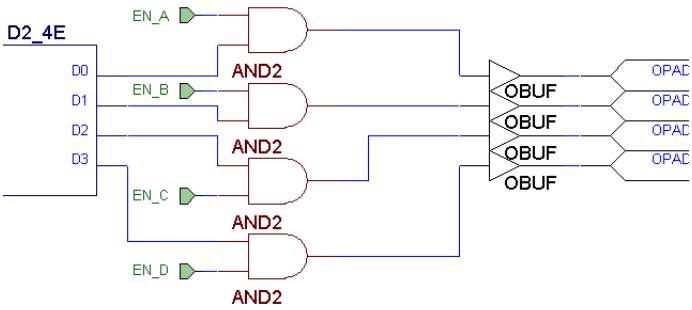

Figure 8.2: Selectively Enable/Disable Any of the Four Seven-Segment Displays.

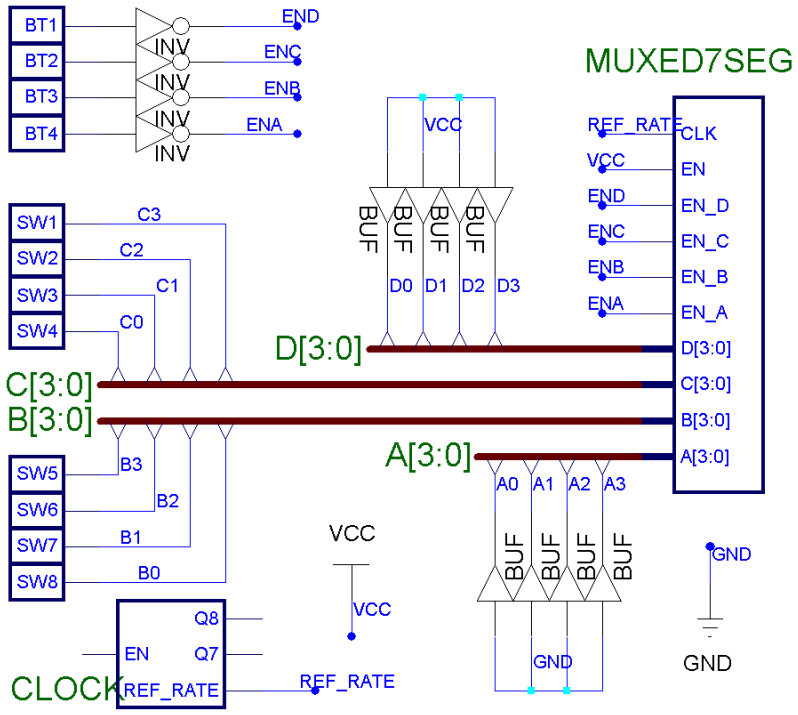

Figure 8.3: Testing Multiplexed Four Seven-Segment Displays Macro.