Non-Deterministic Iterative Solve VLSI CAD Problems

- CAD Problems such as Floorplanning, Placement, Routing, Scheduling, etc., require an enormous amount of computation time.
- Iterative Heuristics such as Genetic Algorithms, Tabu Search, Simulated Evolution, and others have been found effective in solving several NP-hard optimization problems.
- **Objective:** To use a cluster of PCs to solve multi-objective VLSI CAD problems in order to improve quality and reduce run-time

Distribute Computationally Intensive Tasks

- Clusters of low end PCs are easy to build.
- Tools such as MPI and PVM are available for message passing.
- Tools such as gprof, Intel's VTUNE Performance Analyzer, etc., are used for generating profiles for serial codes and determining the part of the code that has the bottlenecks.
- Iterative algorithms are non-deterministic, and dividing work load, i.e. partitioning the search space, is a challenge.
- The parallelizing model (i.e., Partitioning, Communication, Agglomeration and Mapping) is very well-defined for numerical problems, which are mostly deterministic. This is not the case for Iterative heuristics, which are non-deterministic.

cations from this Project

- Sadiq M. Sait, Mustafa I. Ali, Ali Mustafa Zaidi, ñMultiobjective VLSI Cell Placement Using Distributed Simulated Evolution Algorithmò, IEEE International Symposium on Circuits and Systems, ISCAS, Kobe, Japan, May 2005.
- Mahmood R. Minhas, Sadiq M. Sait, ñA Parallel Tabu Search Algorithm for Optimizing Multiobjective VLSI Placementò, Intôl Conf. on Computational Science and itôs Application, May 2005, Singapore, Proceedings published by Springer-Verlag in Lecture Notes in Computer Science, LNCS 3483, pp. 587-595.
- Sadiq M. Sait, Mohammed Faheemuddin, Mahmood R. Minhas, Syed Sanaullah, ñMultiobjective VLSI Cell Placement using Distributed Genetic Algorithmò, ACM Genetic and Evolutionary Computation Conference, GECCO, June 2005, Washington DC, USA.
- Sadiq M. Sait, Syed Sanaullah, Ali Mustafa Zaidi, Mustafa I. Ali, ñComparative Evaluation of Parallelization Strategies for Evolutionary and Stochastic Heuristicsò, ACM Genetic and Evolutionary Computation Conference, GECCO, June 2005, Washington DC, USA.

tionship to Intel's R&D

- COE Department has faculty experienced in VLSI Design.
- A book in the area of iterative algorithms has been authored by the department faculty.
- The Technology Center being proposed in RI will have the state-of-art tools and equipment.
- Faculty and students currently interested in HPC and parallelization of heuristics can work together to address industrial and real-world problems.

in our Current Cluster

- **MPICH Library** provides a flexible implementation of MPI for easier message-passing interface development on multiple network architectures.
- **Intel® Trace Collector 5.0** applies event-based tracing in cluster applications with a low-overhead library. Offers performance data, recording of statistics, multi-threaded traces, and automatic instrumentation of binaries on IA-32.
- **Intel® Trace Analyzer 4.0** provides visual analysis of application activities gathered by the Intel Trace Collector.
- TotalView (MPICH) is also used for observing communication between processors.
- Also used in Condor (for scheduling jobs on the cluster).