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Timing influenced general-cell genetic floorplanner

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Abstract

In this paper we present a timing-influenced floorplanner for general cell IC design. The floorplanner works in two phases. In the first phase we use the genetic algorithm and restrict the modules to be rigid and the floorplan to have slicing structure. This restriction results in a simple and elegant encoding, as well as large savings in run time. In this phase the search is directed toward floorplans that better satisfy timing constraints on the critical paths and delay bounds on all the nets. The objective function also incorporates area and wirelength. The second phase allows modification to the aspect ratios of individual modules to reduce further the area of the overall bounding box. This phase is constraint graph based. The approach combines the robustness of genetic algorithm with run time efficiency and elegance of constraint graph based method. Experimental results are presented.