MINIMISING LATENCY OVER FRAME RELAY ASYNCHRONOUS TRANSFER MODE INTERWORKING

A. Hellany   H. Achi   A. Rizk   M. Nagrial

University of Western Sydney, School of Electrical Engineering & Industrial Design
Locked Bag 1797, Penrith South DC, NSW, Australia
Phone: 61-2-47-360-126, Fax: +61-2-47-360-833
Email: a.hellany@uws.edu.au,

Abstract -The implementation of FR-ATM network is presenting challenging service interworking issues. This paper describes the process of build-up delay in a FR ATM interworking, and proposes a new approach to reduce the latency by increasing the PIR/SIR ratio. Furthermore, A case study is introduces in order to validate the proposed method. Finally, the burstiness, virtual bandwidth and buffer overflow affecting the network performance are discussed.

I Introduction

For a FR service to be carried over ATM backbone, there are several issues of concern to carriers and customers. Customers generally connect to ATM network using Frame Relay access. The switch interface terminating the customer access link performs a translation from Frame to ATM as per Frame Relay interworking Function standard FRF.8. This data is then delivered to the particular customer Core router ATM interface as shown in Fig. 1.

Frame Relay and ATM inherent certain characteristics, some of which tend to be problematic in FR-ATM interworking:
At the FR interface customers are able to burst above the Frame Relay CIR and up to the Access Rate for extended periods. Frame Relay nodes use BECNs to signal the upstream device to throttle traffic when congestion occurs.

ATM has no equivalence for BECNs [1] and thus cannot notify upstream devices to throttle back and enforces compliance to PCR, SCR and MBS parameters. Both Frame Relay and ATM specific terminology to describe the rate of user traffic are provided: *Access Rate* (AR) and *Committed Information Rate* (CIR) are Frame Relay parameters, which describe the maximum allowed data rate, and the rate, which the network commits to deliver, respectively. Similarly the terms *Peak Information Rate* (PIR) and *Sustained Information Rate* (SIR) are the corresponding ATM parameters describing the maximum allowed data rate and the average data rate, which the network commits to deliver, respectively [2].

The customer Frame Relay CIR is mapped to the equivalent ATM SIR (allowing for ATM overhead) and the Frame Access Rate is also mapped to the ATM PIR. SLAs have been drafted to provide FR equivalent behaviour when carrying it over ATM. However this expected behaviour might not be totally met under this scenario for some inherent interworking limitations. Inability to measure bursts above the Frame CIR bandwidth [3]. This results from carriers using ATM interfaces in the ATM core routers. When ATM PVCs are loaded, the transfer rate will average to the ATM SCR bandwidth and consequently to the Frame CIR (not the access speed like Frame Relay).
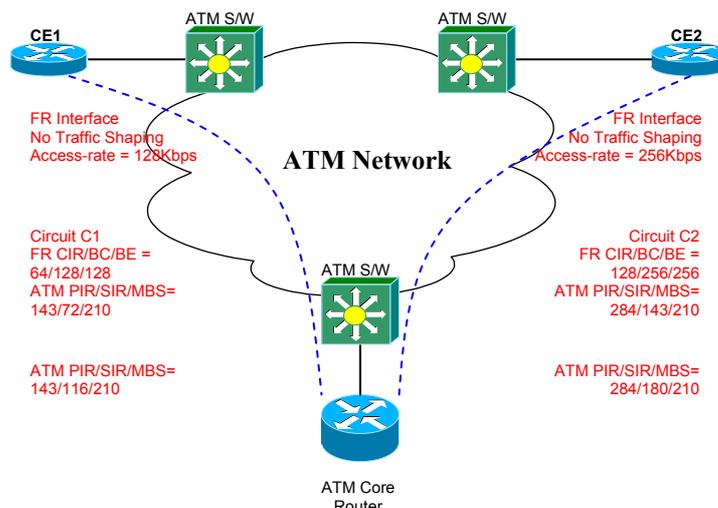

Fig. 1. FR service over ATM network

Latency is increased to values higher than what the customer believes they should experience for their link size and traffic profile [4]. This is due to the longer than expected serialisation delay from the core router ATM interface. Under load data is clocked out of the interface at the SCR rate rather than the PCR rate (Frame Relay sends data at the access rate unless BECNs are received). [5,6,7,8].

The latency improvement in this proposed solution is attained with a tradeoff on network. There is the possibility of overflowing the egress buffer at the FR interface, when the core ATM router sends non-conforming traffic i.e. flat lining at PIR or for large MBS. This will result in increasing the delays in the egress buffer. To guard against long buffer delays, the buffer threshold should be made small or at an optimised level depending on the frame size, PIR and MBS [9].

In this paper we present a parameter configuration for FR-ATM interworking to reduce latency and obtain a FR network like behaviour over ATM. The optimisation of the buffer setting is discussed. This solution can be applied to Multi-Protocol Label Switching (MPLS) routers communicating over ATM backbone.

II. Delay Calculations.

The End-to-End delay can be calculated as follows:
Let D(ab) be the delay experienced by the traffic sent from the branch FR Router to the Core ATM router,

D(ab)= FR serialisation delay + ATM network delay + ATM switching delay   (1)

Let D(ba) be the delay experienced by the traffic sent from the ATM core router to the FR branch router,

D(ba)= core router serialisation delay + network delay + switching delay + FR serialisation + FR queuing delay + FR buffer delay   (2)

Roundtrip delay = D(ab) + D(ba)   (3)

The roundtrip delay experienced by the data sent from a branch router to another branch router or back to itself.

Where FR serialisation delay $= \dfrac{FrameSize * 8}{AR}$ (4)

Core router to ATM serialisation =

$$\begin{cases} \dfrac{FrameSize*8}{AR} \rightarrow \text{for packets sent at PIR} \\ \dfrac{FrameSize*8}{CIR} \rightarrow \text{for packets sent at SIR} \end{cases} \quad (5)$$

Switching delay =250 μ s/cell for CDVT of 250us.
Network delay = 5ms, it usually depends on the number of hops and distances between the nodes.

FR queuing delay = 5 ms, this depends on the switch fabric and packet processing.
FR buffer delay depends on the amount of data held in the FR egress buffer when congestion occurs. The total delay of this buffer is equal the buffer threshold setting in ms, under no congestion the buffer delay is nil.

The existing parameter settings, as shown in Fig. 1, are: Access link = 128K, CIR=64K, PIR/SIR = 144/72 Kbps. It is assumed that the router can transmit at either AR or PIR. Hence,

$$D(ab)= \frac{1500*8}{128} +5+0.25=99 \text{ ms}$$

$$D(ba)= \frac{1500*8}{128} +5+.25+ \frac{1500*8}{128} +5+0=197.75 \text{ ms}$$

Worst case

$$D(ba)= \frac{1500*8}{64} +5+.25+ \frac{1500*8}{128} +5+0=291.5 \text{ ms}$$

Roundtrip delay is then 296.75 ms or at worst case = 390.5 ms. this round trip delay is large for certain applications and services which are delay sensitive.

III. Proposed Solution

To reduce the latency, we propose to increase the PIR to a larger value in order to decrease the serialisation from the core router to ATM interface. It is also possible to increase SIR to a value equivalent to the AR plus overheads as shown in Fig. 2. However, there are several effects on the network, which need to be addressed and guarded against such as network burstiness, virtual bandwidth and buffer overflow. The proposed settings are provided in Table 1.

The PVC specifications are listed below:
FR service category: Low Delay;
ATM service category: nrt-VBR;
Interworking: service FRF.8
ATM Traffic Policing: Tagging
Frame Discard: Enabled {Partial Packet Discard PPD}

$$D(ab)= \frac{1500*8}{128} +5+0.25=99 \text{ ms}$$

$$D(ba)= \frac{1500*8}{1024} +5+.25+ \frac{1500*8}{128} +5+0=115.72 \text{ ms}$$

Worst case

$$D(ba)= \frac{1500*8}{128} +5+.25+ \frac{1500*8}{128} +5+0=197.75 \text{ ms}$$

Under the proposed solution, the new delay becomes:
Roundtrip delay is 214.72 ms or at worst case = 296.75 ms. this leads to a delay improvement of 24% to 41% in ATM-FR direction, whereas the Roundtrip delay improvement is 24% to 27%.

ATM switch settings	ATM Core Router settings
PIR =1145 kbps *(fixed to match 1024 Kbps FR access)*	PIR=1145 kbps
SIR = 1.12625 * CIR kbps *(eg. for CIR = 64kbps, SIR= 72kbps)*	SIR = 1.12625*FR Access Rate kbps *(eg. for AR=128kbps, SIR=143kbps)*
MBS = 210 cells	MBS=48 to144 cells

IV. Egress Buffer Optimisation

The Frame egress buffer needs to be optimised to account for the increased burstiness. Increased MBS and PIR result in great probability of faster buffer fill under burst conditions.

In a frame relay Quality of Services (QoS) network, there are three congestion thresholds, (Absolute, Severe and Mild Congestion Thresholds: ACT, SCT, and MCT) which may be configured per service category in milliseconds. These congestion thresholds serve three main purposes:

- Frame loss management,
- Congestion notification to end-user equipment, and
- Prevent frames being stored in a queue for more than ACT.

The Egress queuing delay (EQD) encountered by a frame in FR ATM network is the delay accumulated after it has been switched by the node from the ingress Frame Relay Stream (FRS) to the egress (FRS) and before its transmission on the egress FRS.

The EQD is viewed as an average delay that does not change dynamically according to FRS congestion status, and it should be less than MCT for an FRS.
EQD is defined by the following expression:

$$EQD = \frac{ACT\,(in\,bytes)*8}{FRS\,speed\,(in\,bps)}$$

If FRS congestion threshold settings are set too low, it may lead to an increase in loss of DE=0 frames for a service category. On the other hand, if the congestion thresholds are set too high for a specific service category, then it may lead to an increase in egress queuing delay. To guard against long buffer delays, the buffer threshold should be made small or at an optimised level depending on the frame size, PIR and MBS as shown in Fig. 3 and 4.

V. Conclusion

This paper identified the FR-ATM network latency, and proposed a solution to reduce the delays by increasing the PIR/SIR ratio. The impact of the novel approach on the network performance: burstiness, virtual bandwidth and buffer overflow is analysed and discussed. Series of strategies are proposed in order to guard against the stated impacts.
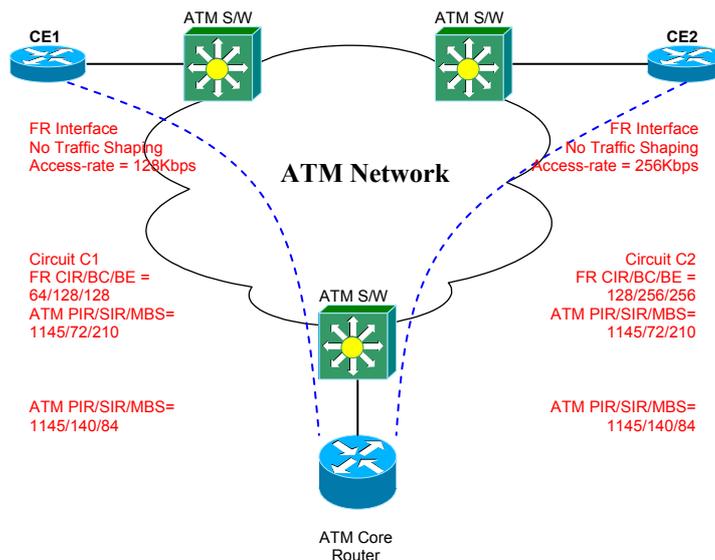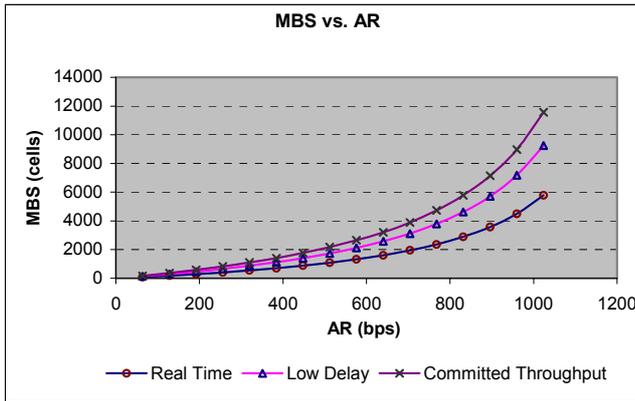

Fig. 2: FR service over ATM network

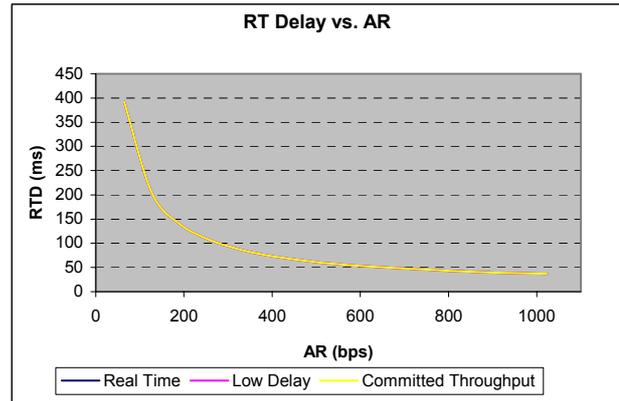Fig. 3. MBS optimised setting for minimum buffer delay.

Fig. 4. Roundtrip delay for optimised MBS

References

[1] Sudhir Dixit and Stuart Elby "Frame Relay and ATM interworking", IEEE Communications Magazine, June 1996.

[2] Sudhir s. Dixit, Senior Member, IEEE, and Sharad Kumar "Traffic Descriptor Mapping and Traffic Control for Frame Relay Over ATM Network", IEEE/ACM Transaction on Networking, VOL. 6, NO. 1, February 1998

[3] Jae-II Jung, "Translation of QoS parameters into ATM performance parameters in B-ISDN", IEEE Communications Magazine, August 1996.

[4] J.W. Paek, S.W. Lee, C.H Oh and K.S Kim "A Study on traffic Parameters Estimation of call Admission Control in ATM Networks", 1999 IEEE TELCON pages 836-839.

[5] "af-tm-0056.000, Traffic Management Specification", The ATM Forum Technical Committee, version 4.0, April 1996

[6] "af-bici-0013.003, B-ICI Specification", The ATM Forum Technical Committee, version 2.0, December 1995.

[7] "FRF.5, Frame Relay/ATM PVC Network Interworking Implementation Agreement", The Frame Relay Forum, December 1994.

[8] "FRF.8, Frame Relay/ATM PVC Service Interworking Implementation Agreement", The Frame Relay Forum, April 1995.

[9] H. Achi, A. Rizk, and A. Hellany, "Novel Approach to reduce Latency over FR ATM Interworking", 1st Workshop on the Internet Telecommunications and Signal Processing (WITSP'02) University of Wollongong. Vol 1. pp. 134-137, December, 2002, Wollongong, Australia