Effect of Glitches on the Efficiency of Components' Region-Constrained Placement as a Fast Approach to Reduce FPGA's Dynamic Power Consumption

Seyed E. Esmaeili[1], Nabil I. Khachab[1], Moustafa Y. Ghannam[2]

[1]*EE Department*
Kuwait University
P.O. Box 5969, Safat 13060, Kuwait
E-mail: khachab@eng.kuniv.edu.kw

[2]*Department of Physics*
The American University in Cairo
E-mail: mghannam@aucegypt.edu

Abstract

The increased flexibility offered by FPGAs implies that more transistors are needed which leads to higher power consumption per logic gate. FPGAs power consumption is fast becoming an essential design consideration especially for mobile systems with a limited power supply. The effect of components' region-constrained placement on reducing internal nets total capacitance and the corresponding change in internal nets' total dynamic power consumption is investigated. Two logic circuits were specified as components covering around 80% of total FPGA busy gates. These components are multiplexers and adders along with multipliers. Each of these components was implemented on two of Xilinx FPGA's families, namely; Spartan II and Virtex. Gate-level power estimation for different region-constrained placements of each logic circuit was carried out using the Xilinx hierarchal power distribution analyzer, XPower.

1. Introduction

Field Programmable Gate Arrays (FPGAs) have traditionally been used in environments where their energy consumption was not critical. However, current FPGAs play many important roles, ranging from small glue logic replacement to System-on-Chip designs. Present day portable devices have become more complex, and can take advantage of the programmability offered by the FPGA. Today's largest FPGAs implement complex systems with millions of gates that can consume several watts of power. In rising to the challenge to reduce power, the semi conductor industry has adopted a multifaceted approach, attacking the problem on three fronts [1]:

- Reducing chip capacitance through process scaling. This approach to reducing the power is very expensive.
- Reducing voltage. While this approach provides the maximum relative reduction in power it is complex, difficult to achieve and requires moving the systems industries to a new voltage standard.
- Employing better architectural and circuit design techniques. This approach promises to be the most successful because of its relatively small cost in comparison to the other two approaches.

1.1 Related Work

Several analysis of FPGAs power consumption have appeared in the literature. It was shown that power dissipation in FPGAs devices is predominantly in the programmable interconnection network. It was reported that as high as 50% to 70% of total power is dissipated in the interconnection network [2], with the remainder being dissipated in the clocking, logic, and I/O blocks. The dominant role of interconnect in total FPGA power consumption implies that characterization and management of net capacitance is a crucial part of a power–aware FPGA design [3]. Leakage power reduction in FPGAs was proven to be achievable through region-constrained placement where the FPGA fabric was divided into small regions and the power supply to each region was switched on/off using a sleep transistor [4].

In this paper, the effectiveness of region-constrained placement of different logic components as a fast approach to reduce dynamic power consumption is investigated.

2. Theory and Implementation

Placement is essentially assigning a unique position inside the FPGA to each of the configurable logic blocks of the logical circuit to be implemented. Placement has

essentially been used as a mean to reduce area and path delay. In the following, dynamic power reduction through region-constrained placement for different components is investigated. Table 1 below presents a brief comparative description of the Xilinx FPGAs device families used in the implementation process.

Table 1. Xilinx FPGAs

FPGA Family	Saprtan II	Virtex
Device	xc2s100	xcv100
Technology	0.18 um	.22 um
V_{CCO} (as reported in XPower)	3.3 v	3.3 v
V_{CCINT} (as reported in XPower)	2.5 v	2.5 v
Logic Cells	2,700	2,700
Slices	1200	1200
Flip-Flops	2400	2400
LUTs	2400	2400
Maximum Available User I/O	200	180
XPower Data Version	Preliminary	Production
Anticipated Error in Power Estimation	20%	10%

A VHDL code was written to implement a 32-to-1 line multiplexer using two 16-to-1 line multiplexers and one 2-to-1 line multiplexer as shown in Figure 1 below. In addition, a combination of a 16 by 16 bits add/shift multipliers and three carry look ahead adders were initialized as components to implement a simple function $F=2\times[(a\times b)+(a\times b)]$ as shown in Figure 2.

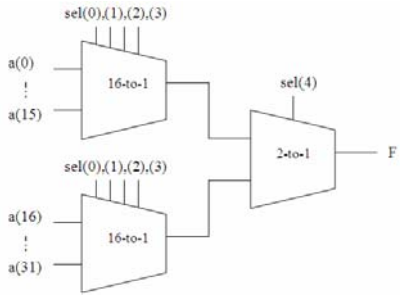

Figure 1. 32-to-1 Multiplexer

The logical circuits had to be repeated in order to increase the percentage of the FPGA's busy gates to around 80%. The multiplexer had to be repeated 90 times and the adder/multiplier 3 times. It should be noted that each of the repeated components shared the same input pins and that in some cases the outputs had to be combined using an AND gate in order to avoid exceeding the FPGA's available output pins.

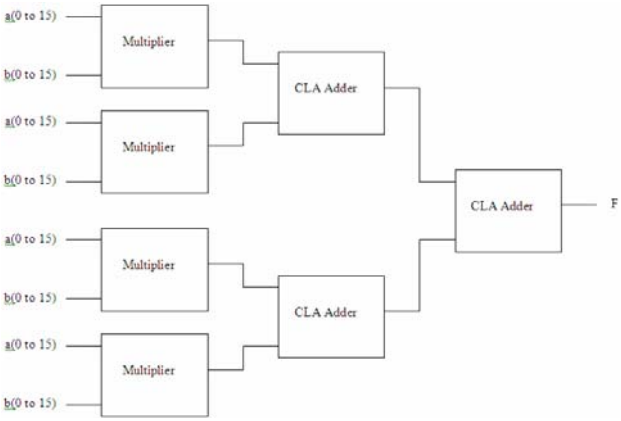

Figure 2. CLA Adder & Add-Shift Multiplier

Synthesis of the VHDL code was performed using the Xilinx Synthesis Technology (XST). The synthesis optimization goal was set to area, the optimization effort was set to normal, and the hierarchy of the design was preserved. Correct design functionality was verified by performing post synthesis simulation. Then, the location of each of the components and its respective I/O ports were assigned using the Xilinx Pinout and Area Constraints Editor (PACE). The location of the components and I/O ports was saved in a User Constrained File (UCF). For each of the logic circuits mentioned earlier, the components were randomly placed across the FPGA. A total of seven random placements were specified for each of these circuits' components. Though the percentage of FPGA occupation did not exceed the available FPGA resources, some problems were encountered in placing the components for certain logic circuits. The reason of this could be due to the way the components are being presented in the Xilinx Pinout and Area Constraints Editor (PACE). It was observed that all components were assigned rigid shapes (mostly the rectangular shape). Assigning more flexible shapes according to the component's resource occupation would certainly maximize placement flexibility. Following the specification of each component's location, place and route was performed using Xilinx FPGA Editor to route the components in the specified devices. The place and route effort was set to high, while the place and route mode set to normal. Finally, after ensuring that the design

components have been successfully placed and routed with no errors reported, a post place and route simulation was run. A Value Change Dump (VCD) file providing detailed design activity rates for all nets is generated by Modelsim in post place and route simulation. This file is required by XPower to have all the necessary information about the activity rates of all the ports and nets in the design. Figure 3 shows a simplified view of the power estimation flow in XPower.

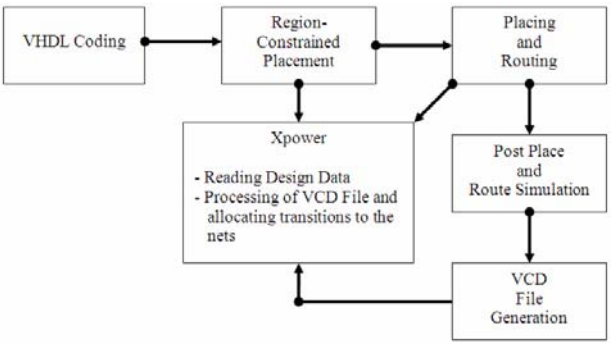

Figure 3. XPower Power Estimation Flow

3. Results Obtained

XPower divides the reported dynamic power consumption into the following five categories:

- **Clock Power:** is the power consumed by clocks in the design.
- **Inputs Power:** is the power consumed by the buffers configured as IBUFs.
- **Logic Power:** is the power consumed by the logic in the design.
- **Outputs Power:** is the power consumed by the buffers configured as OBUFs.
- **Signals Power:** is the power consumed by internal nets.

In the following, the effect of region-constrained placement on the capacitances reported by XPower for each of the above five categories will be presented followed by the relationship between capacitance change and the reported dynamic power estimation for different logic circuits implemented. It should be noted that glitches are translated in XPower as higher activity rates which means higher power. The results obtained for Spartan II- xc2s100 and Virtex- xcv100 will be presented respectively.

Plotting signals dynamic power consumption versus total signals capacitance has revealed that the relationship between internal nets capacitance and the corresponding dynamic power consumption changes with respect to the logic circuit being implemented. To further investigate this relationship, the highest reported capacitance for signals in the seven region-constrained placements for each of the logic circuits that were implemented was taken and the corresponding reduction of signals capacitance and its respective effect on dynamic power was calculated for both device families used in our design.

The correlation coefficient between the change in the capacitance and the corresponding change in power consumption was calculated. A correlation coefficient > 0.75 was considered to indicate strong positive relation, whereas a -0.75 < coefficient < 0.75 would suggest that they are unrelated, and a coefficient < -0.75 would indicate strong negative relationship.

Tables 2 and 3 show the correlation between the change in signals' capacitance and its dynamic power consumption. In all of these tables the percentage reduction in signals' capacitance was calculated with respect to the placement with the highest reported capacitance and hence there are only six placements reported in each table.

Table 2. Signals' Capacitance-Dynamic Power Relationship for the Multiplexer

	Spartan II			Virtex	
	Percentage Change in Signals'			Percentage Change in Signals'	
Placement	Capacitance	Dynamic Power	Placement	Capacitance	Dynamic Power
P#1	-1.14%	-1.52%	P#1	-3.90%	-2.53%
P#3	-1.06%	-1.74%	P#2	-2.22%	-0.73%
P#4	-0.67%	-0.02%	P#3	-1.72%	-3.05%
P#5	-0.67%	-0.02%	P#5	-0.03%	0.15%
P#6	-0.35%	1.56%	P#6	-0.37%	2.77%
P#7	-0.35%	-0.25%	P#7	-3.24%	-3.52%
Correlation Coefficient	0.86		Correlation Coefficient	0.76	
Indication	Strong Positive Relation		Indication	Strong Positive Relation	

Table 3. Signals' Capacitance-Dynamic Power Relationship for the Adders/Multipliers

	Spartan II			Virtex	
	Percentage Change in Signals'			Percentage Change in Signals'	
Placement	Capacitance	Dynamic Power	Placement	Capacitance	Dynamic Power
P#1	-42.09%	113.79%	P#1	-7.11%	0.78%
P#2	-6.99%	-8.58%	P#3	-50.68%	89.62%
P#3	-42.09%	113.15%	P#4	-22.57%	24.32%
P#4	-19.26%	6.66%	P#5	-28.11%	16.36%
P#5	-25.03%	2.25%	P#6	-19.85%	20.77%
P#6	-42.09%	109.94%	P#7	-27.38%	10.03%
Correlation Coefficient	-0.94		Correlation Coefficient	-0.90	
Indication	Strong Negative Relation		Indication	Strong Negative Relation	

4. Conclusion

Although substantial reduction in internal nets (signals) capacitance is achievable through careful region-constrained placements of components, the expected gain of reduced dynamic power consumption of these internal nets is dependent on the logic circuit being implemented. In the case of the multiplexer, there was an observable high correlation between signals' capacitance reduction and the corresponding reduction in their dynamic power consumption. However, the correlation between reducing signals' dynamic power through capacitance reduction was diminished in the case of the multipliers and adders; where it is a known fact that glitches are common in arithmetic circuits, especially in large multipliers where they often represent the major part of transitions [5] and where glitching power dissipation can amount to 20% of the total power dissipation [6]; there has been observable negative relationship between internal nets capacitance reduction and the anticipated reduction in their dynamic power. For instance, as high as 42% reduction in internal signals capacitance was achieved through region constrained placement but caused 113% increase in internal nets dynamic power dissipation for the Spartan II case. Also, in the Virtex case as high as 50% reduction in capacitance has caused around 90% increase in signals dynamic power.

Reducing the capacitance of internal nets through careful region-constrained placements of components is not an effective way for dynamic power reduction. The reduction of internal nets capacitance must be accompanied with balancing data paths delays in order to reduce glitches as much as possible and thus increase the correlation between capacitance and dynamic power reduction.

Unfortunately the effect of region-constrained placement on static power was not investigated since the only fully licensed software at the time of this research was the Xilinx Project Navigator and XPower. XPower has reported constant Quiescent (Static) power regardless of the running frequency, logic circuit implemented, number of components, or placements of these components.

More experiments need to be carried out to further investigate the effectiveness of region-constrained placement as a mean to reduce dynamic power consumption in other FPGAs architectures from other vendors such as Actel, Algotronix, and Altera. Also, more accurate transistor-level power estimating CAD tools are required to provide comprehensive calculations and accurately estimate the effect of region-constrained placement on dynamic power as well as on short-circuit and leakage power.

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