Coding for Minimizing Energy in VLSI Interconnects

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***Abstract*— In CMOS VLSI circuits, the dynamic power dissipation contributes a significant fraction in the overall power dissipation. Hence, the main target of VLSI designers is to minimize the switching activity on the on-chip bus lines. In this paper, the authors propose a novel bus encoding technique which minimizes both self and coupling transition activity to curtail the global power dissipation. The performance of the proposed coding scheme has been tested on various SPEC'95 benchmarks and found that with respect to unencoded data, an average reduction of 28% and 26% with respect to self and coupling energies in the total power dissipation is achieved. The hardware, used for encoding and decoding purposes, has been designed using Magma©tools.**

***Index Terms*— Low power, Interconnect, Crosstalk, VLSI**

I. Introduction

MOORE'S law says that the performance of an IC doubles every 18 months, the interconnect performance is expected to double only over the next decade [1]. This disparity, caused due to the various inductive and capacitive effects, poses a major challenge to VLSI system designers. Much of the power in a bus is dissipated in the process of charging and discharging the high nodal and inter-wire capacitances. Hence, majority of the works [2, 3, 4, 5], which exist in the literature focus on minimizing the bus transition activity. A very popular method among them is the Bus Invert method [3], which does a conditional inversion of the bus lines to minimize the self transitions and thereby reducing the self energy. As we approach Deep Submicron (DSM) and Ultra Deep Submicron (UDSM) technologies, the effect of inter-wire capacitance becomes significant due the high proximity of the bus lines carrying signals. As a result, many attempts [4-9] to reduce the coupling transition activity also exists. In this paper, the authors propose a new coding technique which minimizes both coupling and self transition activities in the bus lines.

The rest of the paper is organized as follows: Definitions of some of the important terms which are used in this paper are given in section II. The problem formulation is given in section III and a brief overview of the previous works related to bus coding is given in section IV. The energy model is shown in section V. The proposed coding scheme is explained in section VI and its hardware implementation is shown in section VII. While, illustration of the proposed coding scheme with an example is shown is section VIII, the results and discussions are provided in section IX. Finally, conclusions are made in section X.

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II. Definitions

1) *Coupling Transition (CT)*: A Coupling Transition is defined as a transition from $0 \rightarrow 1$ or $1 \rightarrow 0$, between two adjacent bus wires.
2) *Self Transition (ST)*: A Self Transition is defined as a transition from $0 \rightarrow 1$ or $1 \rightarrow 0$ on bus with reference to the previous data on it.
3) *Bus Width (BW)*: The number of bits in the data is called the Bus Width.

III. Problem Formulation

In general, four sources of power dissipation can be identified in any CMOS VLSI circuit and they are related to the global power dissipation [6] by (1).

$$P_{Dissipation} = P_{Static} + P_{Dynamic} + P_{Leakage} + P_{Shortckt} \quad (1)$$

The major share in the overall power dissipation is that of dynamic power dissipation. Hence, this paper concentrates on reducing $P_{Dynamic}$ using a novel encoding technique described in section VI. Furthermore, the dynamic power dissipation in a CMOS VLSI circuit is given by

$$P_{Dynamic} = \alpha * V_{DD}^2 * C_L * f \quad (2)$$

where, α is the transition activity factor, V_{DD} is the supply voltage, C_L is the load capacitance and f is the frequency of operation. It is clear from (2) that, in order to minimize the dynamic power dissipation, attempts must be made to reduce one or more factors on the right hand side. In this paper, the authors focus on lowering the activity factor , which is a promising way of reducing the power dissipation. The transition activity factor α is given by

$$\alpha = \alpha_s C_s + \alpha_c C_c \quad (3)$$

where, α_s is the self transition activity factor which arises from the changes in a particular bus line, C_s is the self capacitance i.e. the capacitance between the bus wire and the ground, α_c is the coupling transition activity factor which arises due to the difference in bits carried by adjacent bus lines and C_s is the coupling capacitance i.e. the capacitance between two adjacent bus wires.

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IV. Previous Work

The bus coding techniques existing in the literature, which attempt to reduce the power dissipation, can be classified into two major categories.

One set of methods aim at reducing the transitions in the address busses. Some of them are A^2BC [11], The Beach Solution [12] and Gray Coding [13]. These techniques exploit the redundancy to minimize the power dissipation.

The other set of methods aim at reducing the transitions in the data buses. Among them, Bus Invert [3] is an efficient method for reducing the power dissipation by minimizing the self transitions. According to this method, if the number of bits that change is more than half the width of the bus, then the entire bus is inverted and transmitted. For decoding purposes, an extra bit is transmitted with the data which shows if the data in the bus is inverted or not. The main disadvantage of this method is that the authors concentrated only on self transitions. For DSM technology, the coupling effects become more dominant and Samala et al. proposed [4], which aims at reducing the coupling capacitance. In this method, the power consumed by their huge circuit would surpass the power savings and hence is not suitable for low power applications. Some of the other works existing in this field are Shift Invert [8] method and Coupling Driven Bus Coding [15]. A majority of the encoding techniques currently existing in literature do not consider both the self and coupling effects, while this paper considers the effects of both self and coupling transitional activities to minimize the power dissipation.

V. Energy Model

The DSM model of n interconnects in parallel, driven by an inverter [2] is shown in Fig. 1. Here, C_s and C_c are the self and coupling capacitances, R represents the on-off resistance of the driver, V_j^i and V_j^f denote the initial and final voltages in the j^{th} interconnect.

The equation for calculating the total energy dissipation is given by (4) [2]. Equation (5) and Equation (6) describe the energy dissipation due to self transition, E_r^L, and coupling transitions, E_j^I, respectively. The subscript represents the node number and the superscript represents the initial or final value of voltage on the interconnect at that node. For example,V_{j+1}^f represents the final value of voltage at $(j+1)^{th}$ wire. α in (4) represents the technology parameter which is given by (7). The significance of α is that it's value becomes high when the technology shrinks.

$$E = \sum_{r=1}^{N} E_r^L + \alpha \sum_{r=1}^{N-1} E_r^I \tag{4}$$

where,

$$E_r^L = C_s V_r^f (V_r^f - V_r^i) \tag{5}$$

$$E_j^I = C_c (V_{j+1}^f - V_j^f)^2 + (V_{j+1}^f - V_j^f)(V_{j+1}^i - V_j^i) \tag{6}$$

$$\alpha = \frac{C_c}{C_s} \tag{7}$$

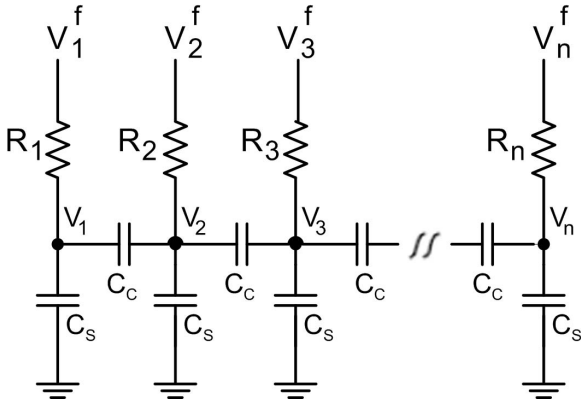

Fig. 1. Deep Submicron Model of N Interconnects in Parallel, Driven by an Inverter

VI. Proposed Coding Scheme

Let the data on an n bit wide bus, at time instant t be denoted as A^t =$\{a_{n-1}^t, a_{n-2}^t, ...a_1^t, a_0^t\}$. The data transmitted on the bus is denoted as $A^{(t)enc}$. The function **calculateST_n(data1,data2)** finds the number of self transitions between **(data1, data2)**. Here, **data1 and data2** should be n bits wide. The function **swapAdj_n (A^t)** swaps the adjacent bits in A_t and gives the output $A^{sw(t)}$ =$\{a_{n-1}^t, a_{n-2}^t, ...a_0^t, a_1^t\}$.

The proposed coding scheme is as follows:

1) Let $A^{(t-1)enc}$ be the previously coded data which was transmitted on the bus and let A^t be the present data which should be encoded and transmitted.
2) Invert the odd lines in A^t and affix it with 00, for decoding puposes. Let this new data be denoted as $A^{t(odd)}$.
   Evalute ***st_odd***=**calculateST_n(**$A^{t(odd)}$**,**$A^{(t-1)enc}$**)**.
3) Likewise, Invert the even lines in A^t and affix it with 01. Let this new data be denoted as $A^{t(eve)}$.
   Evalute ***st_eve***=**calculateST_n(**$A^{t(eve)}$**,**$A^{(t-1)enc}$**)**.
4) Let $A^{sw(t)}$=**swapAdj_n(**A^t**)**. Suffix $A^{sw(t)}$ with 10 and let this new data be denoted as $A^{t(swp)}$.
   Evalute ***st_swp***=**calculateST_n(**$A^{t(swp)}$**,**$A^{(t-1)enc}$**)**.
5) Suffix A^t with 11 and let this new data be denoted as $A^{t(unc)}$.
   Evalute ***st_unc***=**calculateST_n(**$A^{t(unc)}$**,**$A^{(t-1)enc}$**)**.
6) Find ***min(st_odd,st_eve,st_swp,st_unc)***
7) The coded pattern corresponding the minimum value in step **6** is transmitted.

VII. Hardware Implementation

The block diagram of the proposed encoder is given in Fig. 2. The encoder takes an n bit input. The **calculateST_n** functions in the steps **2, 3, 4, 5** in the coding scheme above are evaluated by the *Energy Estimator* block. The outputs of the *Energy Estimator* block, ***min(st_odd,st_eve,st_swp,st_unc)*** are compared among themselves and the minimum amongst them is found out. The encoded data pattern corresponding to the minimum value of self transitions is transmitted on the

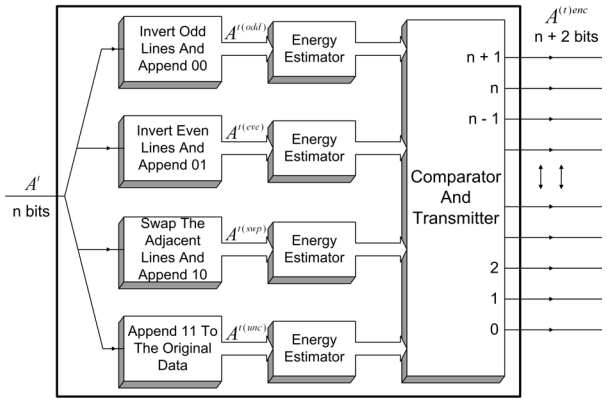

Fig. 2. Block Diagram of the Proposed Encoder

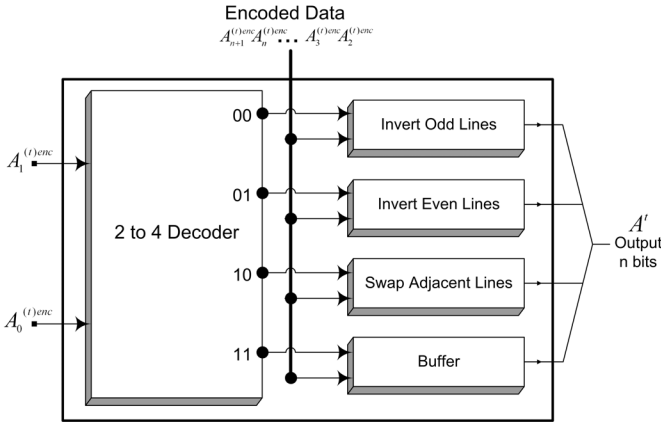

Fig. 3. Block Diagram of the Proposed Decoder

bus.

The decoder to be used at the receiving end is shown in Fig. 3. The two least significant bits in the transmitted pattern are given to a 2 to 4 decoder and depending on these two bits, the appropriate decoding procedure is done.

The internal diagram of a 10 bit of *Energy Estimator* block is shown in Fig. 4. One of the input binary vectors is $A^{(t-1)enc}$, which is the previous data on the bus at time (t-1) and other input is $\{A^{(t)enci}\} \in \{A^{t(odd)}, A^{t(eve)}, A^{t(swp)}, A^{t(unc)}\}$ in sequence. The array of the output binary vectors is $\{B_3B_2B_1B_0\}$. We have used the concept of parallel adders in order to minimize the critical delay. The array of EXOR gates is shown in Fig. 4 performs the action of a coincidence circuit. In this particular example, it can be seen that for a '10' bit Energy Estimation, we get a 4 bit output. In general, for a w bit wide connector, the output of the *Energy Estimator* will be $\lceil log_2(w) \rceil$ bit wide.

VIII. Illustation of the Proposed Coding Scheme

Let the coded data on the bus at time (k-1) be $A^{(k-1)enc}$=$\{\uparrow\downarrow\uparrow\downarrow\downarrow\downarrow\uparrow\downarrow\uparrow\}$ and let A^k=$\{\uparrow\uparrow\uparrow\uparrow\downarrow\uparrow\downarrow\uparrow\}$ be the current data that should be transmitted after encoding. In this case number of transitions without coding is 7 and with coding is given by,

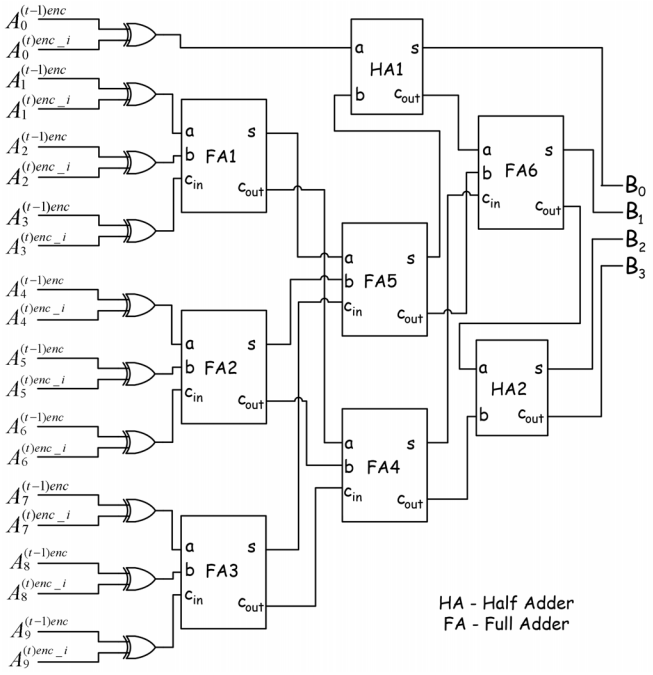

Fig. 4. Hardware Implementation of the Energy Estimator Block

$A^{t(odd)}$=$\{\uparrow\downarrow\uparrow\downarrow\downarrow\downarrow\downarrow\downarrow\downarrow\}$ with ***st_odd*=2**
$A^{t(eve)}$=$\{\downarrow\uparrow\downarrow\uparrow\uparrow\uparrow\uparrow\downarrow\uparrow\}$ with ***st_eve*=7**
$A^{t(swp)}$=$\{\uparrow\uparrow\uparrow\uparrow\uparrow\downarrow\uparrow\downarrow\uparrow\downarrow\}$ with ***st_swp*=7**
$A^{t(unc)}$=$\{\uparrow\uparrow\uparrow\uparrow\downarrow\uparrow\downarrow\uparrow\uparrow\uparrow\}$ with ***st_unc*=4**

Since ***min(st_odd,st_eve,st_swp,st_unc)=(st_odd)***, $A^{t(odd)}$ is transmitted. Hence $A^{(t)enc}$=$A^{t(odd)}$ and the number of transitions is reduced from **7** to **2** with respect to the transmission of uncoded data.

IX. Simulation Results and Discussions

The power dissipation of various coding schemes has been tested with 1,00,000 random vectors for 8 and 16 bit wide bus and the observations are tabulated in Table I. Partitioning of bus lines for buses of higher width (32, 64, 128 bit widths etc.) will give a better power saving than applying the coding directly for the entire bus width [15]. Partitioning of bus lines have not been considered in this paper. The value of the technology parameter, α, increases as the technology shrinks. Experiments have been conducted for various values of the technology parameter and the results are shown in Table I where, α=0 signifies the bus model without coupling effects, α=3.5 represents 130nm technology and α=5 represents 90nm technology. It can be inferred from Table I that the proposed method is efficient when compared to various methods proposed earlier in the literature in terms of reduction in power dissipation with respect to both self and coupling energies. The performance of the proposed coding scheme has been evaluated using SPEC'95 benchmark suite [16] considering the extra bits added for decoding purpose. The results obtained are shown in Table II. In general, any coding technique should consider power dissipation due to coding/decoding hardware (CODEC) also in order to estimate true power saved. Thus, the

TABLE I
PERFORMANCE OF THE PROPOSED CODING TECHNIQUE WITH OTHER CODING TECHNIQUES (EXPRESSED AS PERCENTAGE), CONSIDERING THE EXTRA BITS ADDED THE ENCODER

BCT	BW=8 bit			BW=16 bit		
	α=0	α=3.5	α=5.0	α=0	α=3.5	α=5.0
BI[3]	15.9	14.2	14.0	13.6	13.5	13.5
NBED[4]	9.5	8.98	9.31	8.5	9.0	8.32
DSM BI[9]	19.1	18.82	17.32	16.14	16.0	16.1
SHIV[7]	20.6	18.6	18.5	17.1	18.0	18.0
OE-BI[6]	23.1	22.45	23.0	20.12	19.98	20.02
GC[17]	22.0	21.32	22.0	19	18.12	18
DC[13]	17.32	18.12	17.14	16.4	16.6	16.1
NBC[8]	22.65	21.21	20.0	21.62	21.0	25.9
PM[1]	28.32	27.14	27.0	26.32	26.5	25.9

TABLE II
PERFORMANCE OF THE PROPOSED CODING TECHNIQUE ON SPEC'95 BENCHMARKS CONSIDERING THE TWO EXTRA BITS ADDED BY THE ENCODER

Benchmark	Power Saved	
	Coupling Energy	Self Energy
compress	26.5	25.9
go	24.12	22.9
gcc	28.10	25.45
vortex	25.12	24.38
mpeg	22.9	22.3

actual total power saved, P_{total} is given by (8), where P_s is the power saved due to encoding technique and P_{codec} is the power dissipated by the CODEC relative to the un-encoded bus.

$$P_{total} = P_s - P_{codec} \tag{8}$$

Since, power dissipation due to CODEC has not been considered by earlier coding techniques, CODECs have been designed by the authors for a few select coding techniques and the total power saved has been estimated using (8). The results are illustrated in Table III. It can be seen that the total power saved by the proposed method is much higher than the other methods. Low energy in NBED [4] method signifies that the power dissipated by the CODEC surpasses the power saved by the coding scheme.

TABLE III
THE TOTAL POWER SAVED OF VARIOUS CODING SCHEMES (EXPRESSED AS PERCENTAGE)

Bus Coding Technique	% Total Power Saved
BI[3]	13.2
NBED[4]	2.52
DSM BI[9]	14.5
SHIV[7]	15.5
OE-BI[6]	18.8
Generic Coding[16]	18.2
Dynamic Coding [13]	14.12
NBC[8]	16.55
Proposed Method	23.01

X. CONCLUSIONS

A new bus coding technique, which reduces the power dissipation with respect to both coupling and self energies, has been proposed. This technique achieves a reduction of 28% and 26% in self and coupling energies respectively. Experimental results have shown that the proposed method is suitable for the continually shrinking technology. The CODEC for the proposed coding scheme has been designed using Magma©tools. The total power saved considering the power overhead of the CODEC is found to be 23%. Hence the proposed coding scheme is suitable for low power VLSI applications.

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