CMOS Digitally Programmable Inductance

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***Abstract*—A CMOS digitally programmable active lossless inductor realization is proposed. The proposed inductor is based on current and voltage followers and uses R-2R ladder to provide digital tuning of the inductance value. The followers support the use of the simulated inductor for applications in few MHz range. Whereas the use of R-2R provide an additional advantage of realizing high inductance value suitable for very low frequency applications. The proposed inductor is used in synthesizing cascadable biquadratic filters. Simulation results are presented.**

***Index Terms*— *Analog signal processing*, Current mode circuits, Active filters.**

I. Introduction

Active simulation of inductor is a common design problem in analog integrated circuits. Various topologies based on op amps, nullors, current feedback amplifiers and current conveyors can be found in the literature, for example [1-2]. However, such active-RC realizations rely on the inaccurate RC time constant to determine the inductance value. On the other hand, inductance simulation based on the operational transconductance amplifier (OTA) provides electronic programmability such that of [3]. Unfortunately, transconductor-C (gm-C) based circuit suffers from linearity problems.

Recently, unity gain cells have been used in several applications such as filters and oscillators. This is attributed to their inherent wide bandwidth and low power consumption [4]. More recently, digitally programmable devices [5-8] have become attractive for mixed digital-analog applications. Digital tuning of analog devices not only provides wide programmability range but also allows direct interface with digital signal processing (DSP) controller.

In this paper, a new simulated inductance based on current followers, unity gain buffers, and digitally controlled R-2R ladder is proposed. The R-2R ladder which is conventionally used in data converters is used here to provide digital tuning of the inductance value. It is expected that the proposed inductor will provide the advantage of high frequency operation and programmability, like those of OTA based circuits, while offering improved linearity. Also, the proposed circuit can realize large inductance values in relatively small area which will permit the implementation of large time constant circuit in integrated circuit (IC) chips. Moreover, it will be seen that any filter built using the proposed inductor will be automatically cascadable. Furthermore, the proposed circuit and unlike other grounded inductors can realize lowpass filter function. As demonstrating applications, the proposed inductor is used in synthesizing a new voltage mode resonator filter that provides both bandpass and lowpass functions, simultaneously. Simulation results obtained from a 0.5μm CMOS technology are included.

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II. Basic Building Blocks

This section briefly describes the terminal characteristics and realizations of the basic building blocks of the proposed inductor circuit.

A. Current Follower

An ideal current follower (CF) has zero input impedance and infinite output impedance. Hence the terminal characteristics of an ideal CF, symbolically shown in Fig. 1, can be described by the following matrix equation.

$$\begin{bmatrix} I_z \\ V_x \end{bmatrix} = \begin{bmatrix} 0 & \pm 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_x \end{bmatrix} \quad (1)$$

where the plus and minus signs of the current transfer ratio denote the CF+ or CF- respectively. The X terminal is held at virtual ground, which results in a simple input stage that does not require rail-to-rail operation. A CMOS realization of the CF is shown in Fig. 2 [5].

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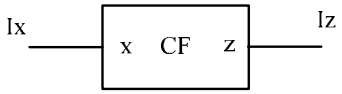

Fig. 1. Current follower symbol

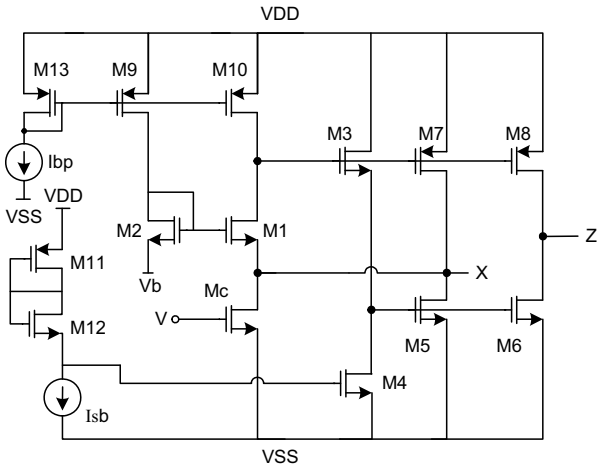

Fig. 2. A CMOS low power current follower

B. *Voltage Buffer*

Ideally, a voltage buffer exhibits infinite input resistance, zero output resistance, and unity gain voltage transfer characteristics. A CMOS class-AB realization of a voltage buffer is shown in Fig. 3 [5]. The circuit utilizes a class-AB loop to boost the transconductance of a MOS transistor operating in the saturation region. Hence, low output impedance can be achieved with low standby power consumption. The voltage tracking of the buffer is achieved by forcing a constant biasing current through transistor M1 and M2.

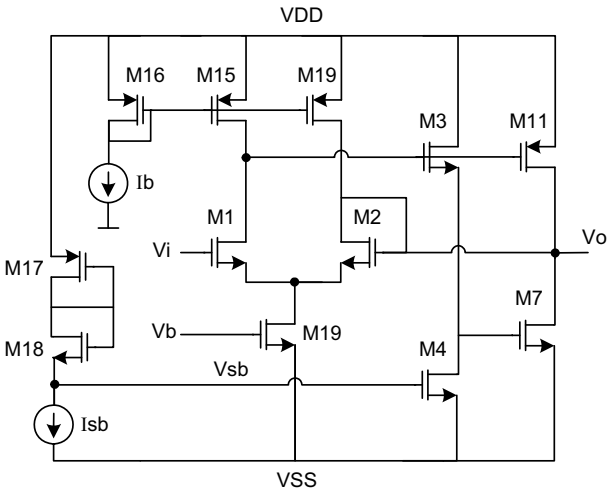

Fig. 3. A CMOS low power voltage buffer

C. *R-2R Ladder*

The R-2R ladder shown in Fig. 4 can be considered as a digitally programmable resistor. Incorporating the R-2R ladder as a circuit element into the circuit design will provide precise frequency characteristics that can be tuned over a wide range. Unlike the case of the g_m–C technique, the tuning feature of the proposed approach does not degrade the dynamic range of the circuit, since it is independent of the active element operating point. It can be seen that the output current (I) is given by:

$$I = \sum_{i=1}^{n} \frac{b_i I_r}{2^{i-1}} \quad \text{where} \quad I_r = \frac{V}{2R} \tag{2}$$

Therefore, the equivalent resistance, seen between the input and output nodes, is given by

$$R_{eq} = \frac{V}{I} = \beta R \quad \text{where} \quad \beta = \frac{1}{\sum_{i=1}^{n} b_i 2^{-i}} \tag{3}$$

where b_i, equaling 0 or 1, is the i^{th} bit in an n bit digital control word. This programmable resistance can be incorporated in inductor simulation designs to provide wide tuning of inductance value without component spreading. This can be applied as long as those resistors are connected to virtual ground, which simulates the proper operating condition of the R-2R ladder. This property is inherently provided by the CF.

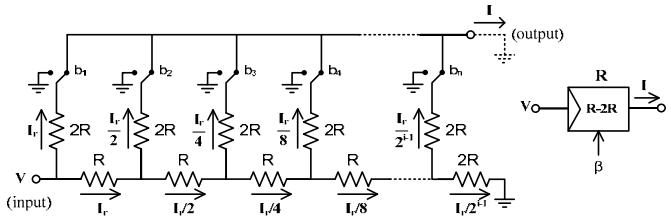

Fig. 4. Digitally controlled R-2R ladder.

III. Proposed Circuit

Using the building blocks of the pervious section, a digitally programmable active inductor can be implemented. The inductor is obtained from the basic circuit of Fig. 5 consisting of a voltage integrator with infinite input impedance followed by voltage to current converter with its output fed-back to the input node. The corresponding lossless inductor circuit is shown in Fig. 6. It can be shown that input impedance of the circuit of Fig. 6 is given by:

$$Z_i = sC_1\beta_1\beta_2 R_1 R_2 \tag{4}$$

where β_1 and β_2 can be digitally controlled. Obviously, the circuit simulates a lossless inductor and inductance is given by:

$$L = C_1\beta_1\beta_2 R_1 R_2 \tag{5}$$

Clearly, the inductance can be tuned digitally via β_1 and/or β_2. On the other hand, a negative lossless inductor can be obtained by changing the polarity of one of the CF.

It can be observed that a large R-2R ladder equivalent resistance can be achieved using a relatively small passive resistance. For example, when $b_i = 0$ for $n = 1, 2, \ldots\ldots (n-1)$ and $b_n = 1$, a n bit R-2R ladder exhibits a large equivalent resistance of $(2^n)R\Omega$ while actually requiring total resistance of only $(3n+1)R\Omega$. Thus, the circuit of Fig. 6 can simulate a very high inductance value and therefore can also be used for implementing very low frequency applications in ICs. For example, with C1=5pF, and 8-bit R-2R ladder with R=10kΩ, a 32H inductance can be achieved. On the other hand, the use of voltage buffer and current follower provides better linearity than OTA and therefore can inherently be used for high frequency applications.

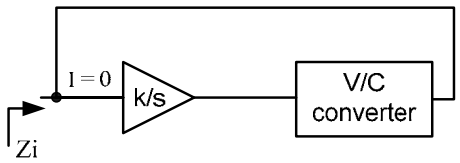

Fig. 5. Basic circuit for inductor realization.

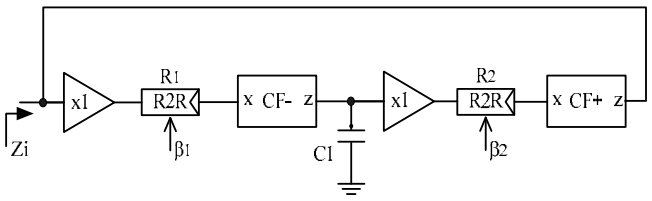

Fig. 6. Proposed inductor realization.

IV. Applications

Actively simulated inductors can be used in several applications such as active filters, oscillator designs and cancellation of parasitic inductances. This section demonstrates that the proposed inductor exhibits several attractive features when used in filter design. First, it provide cascadable voltage-mode biquad filters. Second, it can be used to realize a lowpass biquad which usually requires a floating inductor. It will be shown that when it is used to release a bandpass filter an additional lowpass function is automatically provided.. A second order voltage mode bandpass filter can be obtained by connecting a capacitor C in parallel with the simulated inductor as shown in Fig. 7(a). It is well known that the bandpass response is given by:

$$V_o / V_i = sL / D(s) \tag{6}$$

where $D(s) = s^2 CLR + sL + R$ (7)

and L is given by (5). Therefore, it can be shown that the circuit of Fig. 7(b) provides bandpass and lowpass responses that are given by:

$$V_{BP} / V_i = sL / D(s) \tag{8}$$

$$V_{LP} / V_i = (\frac{L}{R_1 C_1}) / D(s) \tag{9}$$

It can shown from (5) and (7) that the center frequency (ω_o) and the bandwidth (ω_o/Q_o) are given by:

$$\omega_o = 1/\sqrt{LC} = \sqrt{1/(CC_1\beta_1\beta_2 R_1 R_2)} \tag{10}$$

$$\omega_o / Q_o = 1/CR \tag{11}$$

Clearly, ω_o can be tuned digitally using β_1 and/or β_2 without disturbing ω_o/Q_o. Also, the filters are automatically cascadable since they are available at the output of the voltage buffers.

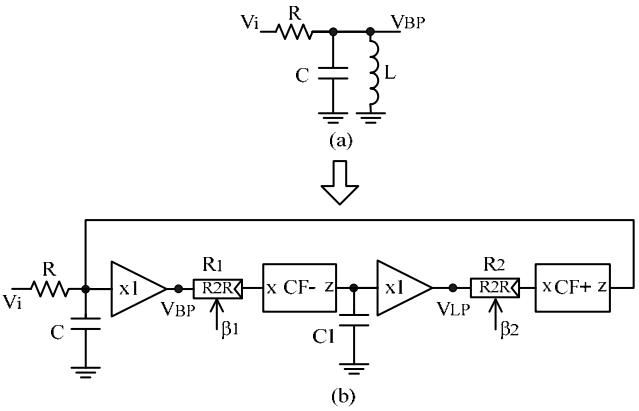

Fig. 7. (a) Passive filter realization (b) Bandpass and lowpass active filter realization using inductor simulation circuit.

V. Simulation Results

The proposed filter of Fig. 7(b) was simulated using SPICE. The 0.5μm BSIM3 CMOS models available through MOSIS were used. Supply voltages were V_{DD}=-V_{SS}=1.5V, Ibp=40μA, Ib=80μA and Isb=8μA. The component values are selected to be C=C1=6.5pF, and 6-bit R-2R ladder with R=10kΩ. Simulation results are shown in Fig. 8 and Fig. 9 for the bandpass and lowpass filters, respectively. Responses of

filters are varied for several different digital control word showing fine and coarse tuning.

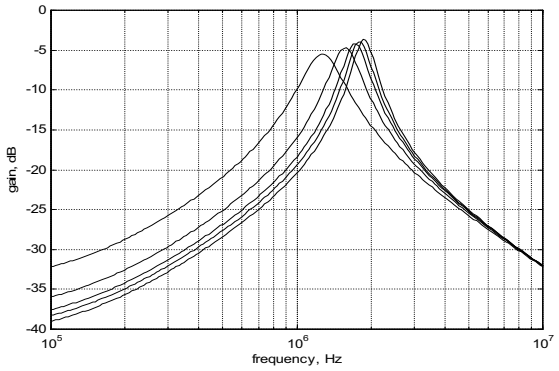

Fig. 8. Simulation results for V_{BP} with passive R=100kΩ

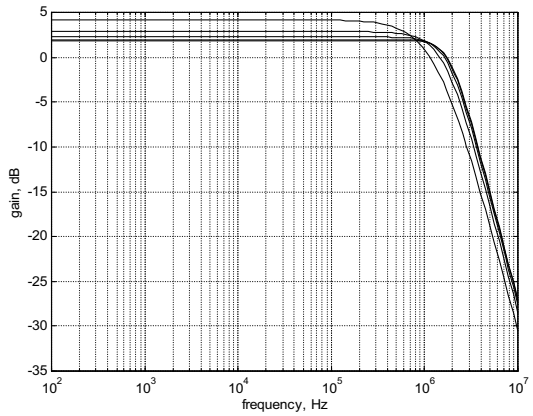

Fig. 9. Simulation results for V_{LP} with passive R=10kΩ

VI. Conclusion

A CMOS simulated inductor circuit based on current and voltage followers and incorporates R-2R ladders is presented. The proposed circuit exhibit several advantages: (a) its value can be digitally tuned (b) it can be used for high frequency application like the OTA based counterparts but with improved linearity (c) It can be used to realize a very high inductance value required for ICs low frequency applications (d) it provide cascadable voltage-mode biquad filters when used in filter design (e) it can be used to realize a lowpass biquad which usually requires a floating inductor. The proposed circuit is used to design a second order filter that simultaneously provides bandpass and lowpass functions. Simulation results based on manufacturer 0.5μm CMOS technology models are included

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