Modified Leakage-Biased Domino Circuit with Low-Power and Low-Delay Characteristics

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Abstract— In this paper, a new domino logic structure whose architecture is based on a leakage biased (LB) domino circuit is introduced. The proposed technique improves the performance and the dynamic power consumption of the circuits. In addition, the number of transistors is reduced leading to a lower silicon area. Simulations are done for various circuits. Compared to the LB method, in a full adder circuit, the delay is reduced more than 25%; also, the dynamic and the static powers have reduced slightly.

I. Introduction

Among the logic styles, the dynamic logic, especially the domino logic, can play an important role in the future integrated circuit because of their higher speed of operation. Among other advantages of the domino logic, one can mention its smaller number of transistors than that of the conventional CMOS. The disadvantage of this style, however, is its high power consumption due to its clock network [1-3].

Many low power design techniques have been proposed mainly targeting the minimization of the main sources of the power dissipation in conventional CMOS VLSI circuits. These sources are the capacitive and the short circuit dissipations which are the dynamic components of the power dissipation [4-6]. The capacitive dissipation, which is the major contributor in the total power dissipation, is caused by charging and discharging the circuit node capacitances. Many circuit realizations have been introduced to reduce this type of power. They focus to minimize the total circuit capacitance [7], the supply and internal voltages [8], and the switching frequency [9]. Most of these circuits require more silicon area.

By reducing the feature size of the technology the supply voltage is reduced to lower the dynamic switching energy per operation. This results in the power reduction at the cost of slowing down the circuit. However, to maintain the performance, the threshold voltages must also be scaled down with the supply voltage. Unfortunately, lowering the threshold voltage increases the static leakage current exponentially. If the feature size reduction continues in the future fabrication process generations, the predicted energy dissipation due to the static leakage current would be comparable to the energy dissipation due to the capacitance switching (dynamic). Some circuits have been proposed to reduce the static power but have increased the dynamic power [13-15]. As an example, one can mention the Leakage-Biased (LB) Domino circuit proposed in [14]. The increase of the dynamic power in this technique originates from the usage of an extra static CMOS inverter gate.

In this work, we propose a new circuit which reduces the power-delay product up to %25 compared to the LB method. The static power is equal to that of the LB technique. The structure of this paper is as follows. In Section II, we briefly review the LB technique while Section III describes the proposed circuit. The results and discussion are given in Sections IV. Finally, the summary and conclusion are given in Section V.

II. Previous Work

An LB-domino buffer is shown in Figure 1 [14]. In comparison with the conventional domino gate, two small sleep transistors are added to the gate: a high-V_{th} PMOS in series with the keeper transistor (and the PMOS inverter) and a high-V_{th} NMOS in series with the pull down branch of the static output logic. High-V_{th} transistors are shown in figure with thick lines for the gates.

To place the circuit into sleep mode, the *sleep* signal is set and *sleepb* signal is reset. If the input data *in* is low, node1 is high but the leakage through the pull down transistors of NMOS pull-down network (PDN) will slowly discharge the node1 to the ground and, hence, the data is lost in the sleep mode.

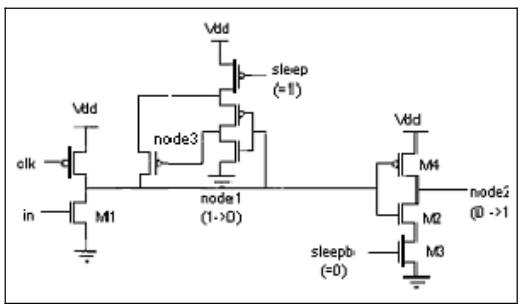

Fig. 1. A leakage-biased domino buffer [14]

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When the internal dynamic node is discharged, the main leakage is across the high-V_{th} PMOS clk transistor which is turned off when the clock signal is high. For the static node (node2), the leakage path includes at least two series NMOS transistors which one of them is a high-V_{th} device. Note that a conventional precharge cycle is used to move from sleep mode back to the active mode.

Using this technique, the LB-Domino gates bias themselves into a low leakage state where the internal dynamic nodes are discharged low and static nodes are charged high regardless of the input vector state. Although this circuit reduces the leakage power, it increases the dynamic power as well as the delay and area.

III. The Proposed Circuit

As discussed above, the main problem of the LB circuit is that it increases the dynamic power. It also adds some transistors and thus the total silicon area is increased. We propose a circuit which suppresses these undesirable effects. The new circuit is shown in Figure 2. The operation of the new circuit is similar to the previous one. Since node2 and node3 take the same values as those of the previous circuit for the same input signals, the signal in node2 can be applied to node3. This eliminates one the extra inverters in the circuit. When this circuit goes to the sleep mode, in the steady state node1 is discharged to ground and node 2 is charged to V_{dd}. The leakage path is through M2 and M3 for node2 and is through M1 for node 1. Since transistor M2 and M3 are connected in series, the stack effect reduces the leakage current. The clock transistor (M1) has high threshold voltage giving rise to a considerable reduction in the leakage.

Since a complete inverter gate is omitted in this circuit, the overall capacitance seen at nodes 1 and 2 is decreased. Subsequently, a reduction in dynamic power and delay in the proposed circuit is anticipated.

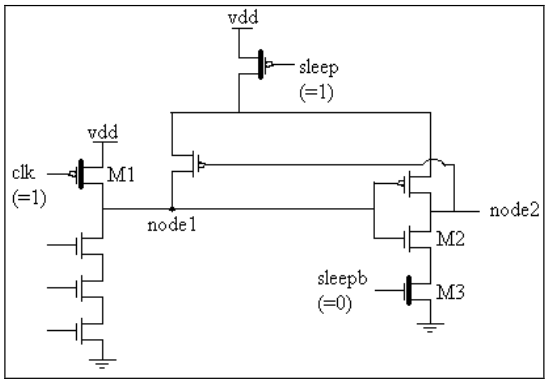

Fig. 2. The proposed circuit in a 3-input OR gate.

TABLE I. The parameters used in the simulations.

Process	65nm	45nm
High-V_{th}	0.22V	0.22V
Low-V_{th}	0.18V	0.18V
V_{dd}	0.9V	0.6V

TABLE II. Results for an Adder circuit in 65nm technology. (V_{DD}=0.9V)

Circuit	Pd [µw]	Ps [µw]	Tp [ps]
LB-Domino	29.09	53.06	330.8
Proposed Circuit	28.28	52.93	240.7

IV. Results and Discussion

To determine the improvements of the suggested technique, 3-input OR gate, AND gate, and a full adder circuits were simulated using HSPICE. The technologies used are two standard CMOS 65nm and 45nm dual threshold voltage [16]. In the simulations, the supply voltage was swept from 0.4V to 1V. The parameters used in the simulations are summarized in Table I. As is seen from this table, V_{th}'s are the same in the two technologies.

We have implemented the conventional adder with our proposed logic. The full adder circuit is shown in Figure 3. The simulation results for the dynamic power (Pd), the static power (Ps), and the delay (Tp) for the full adder are given in Table II. Compared to the LB method, the delay is reduced more than 25% while the dynamic and the static powers have reduced slightly.

In Figures 4-5, the power delay products for the OR and AND gates are shown. The power delay product of the ADDER as a function of the supply voltage is depicted in Figure 6. All these results show that the proposed circuit improves the dynamic power, the delay, and the power delay products for these circuits.

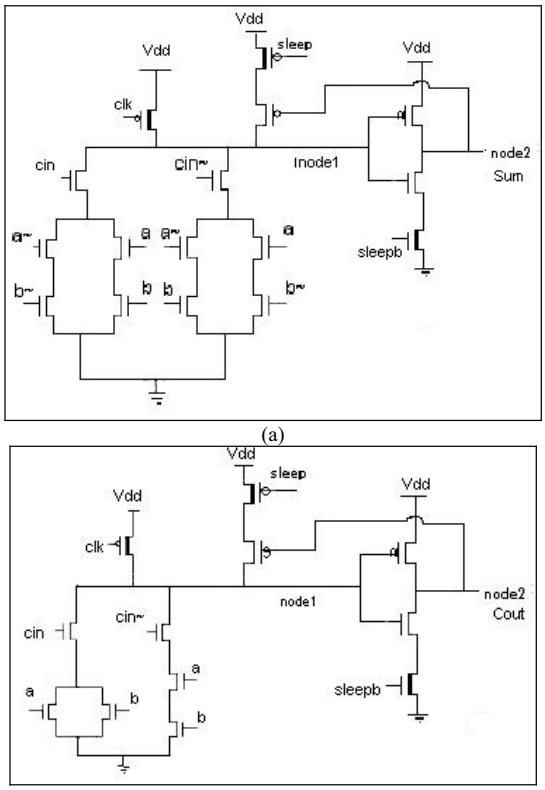

Fig. 3. Domino logic Adder. (a) Sum circuit, (b) Cout circuit.

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V. Summary and Conclusion

In this paper, a domino logic structure which has low static power consumption was proposed. Its architecture is based on a leakage bias domino circuits. Compared to the previous structure, the delay of circuits was reduced more than 25%, in addition; the dynamic power and the area were reduced. The proposed architecture could be used for modern applications where high performance and power-delay product are the main evaluation metrics.

References

[1] W. Wang, M. Anis, and S. Areibi, "Fast Techniques for Standby Leakage Reduction in MTCMOS Circuits," in *Proc. of the IEEE International SOC Conference*, pp. 21 – 24, 12-15 Sept. 2004.

[2] S. Shieh and J. S. Wang, "Design of Low-Power Domino Circuits Using Multiple Supply Voltages," in *Proc. of The 8th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2001)*, vol.2, pp. 711 - 714, 2-5 Sept. 2001.

[3] M. W. Allam, M. H. Anis, and M. Elmasry, "High-speed Dynamic Logic Styles for Scaled-Down CMOS and MTCMOS Technologies," in *Proc. of the International Symposium on Low Power Electronics and Design (ISLPED '00)*, pp.155 – 160, 2000.

[4] P. Chadrakasan and R. W. Brodersen, *Low Power Digital CMOS Design*, Kluwer Academic Publishers, 1995.

[5] J. M. Rabaey, M. Pedram, *Low Power Design Methodologies*, Kluwer Academic Publishers, 1996.

[6] L. Bisdounis, S. Nikolaidis, O. Koufopavlou, G. Goutis, "Accurate Evaluation of CMOS Short-circuit Power Dissipation for Short-Channel Devices", in *Proc. IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, Monterey, California, USA, pp. 184-192, August 12-14, 1996.

[7] M. Hahm, "Modest Power Savings for Applications Dominates by Switching for Large Capacitive Loads," in *Proc. IEEE Symposium on Low Power Electronics*, pp. 60-61, 1994.

[8] S. Lee, and M. Ismail, "1.5 V Full-Swing BiCMOS Dynamic Logic Circuits," *IEEE Trans. on Circuits and Systems*, vol. 43, no. 9, *IEEE Trans. on Circuits and Systems* vol. 43, no. 9, pp. 760 – 768, Sept. 1996.

[9] J. R. Yuan, C. Svensson, and P. Larsson, "New Domino Logic Precharged by Clock and Data", *IEE Electronic Letters*, vol. 29, no. 25, pp. 2188 – 2189, Dec. 1993.

[10] A. Rjoub and O. Koufopavlou, "Low-Power Domino Logic Multiplier Using Low-Swing Technique," in *Proc. of the IEEE International Conference on Electronics, Circuits and Systems*, pp. 45 – 48, vol.2, 7-10 Sept. 1998.

[11] S. O. Jung, S. M. Yoo, K. W. Kimt and S.M. (Steve) Kangi, "Skew-Tolerant High-Speed (STHS) Domino Logic", in *Proc. of the IEEE International Symposium on Circuits and Systems* pp. 154 - 157 vol. 4, 6-9 May 2001.

[12] A. Rjoub, O. Koufopavlou, S. Nikolaidis, "Low-Power Low-Swing Domino CMOS Logic", in *Proc. of the 1998 IEEE International Symposium on Circuits and Systems*, pp.13 – 16 vol.2, 31 May-3 June 1998.

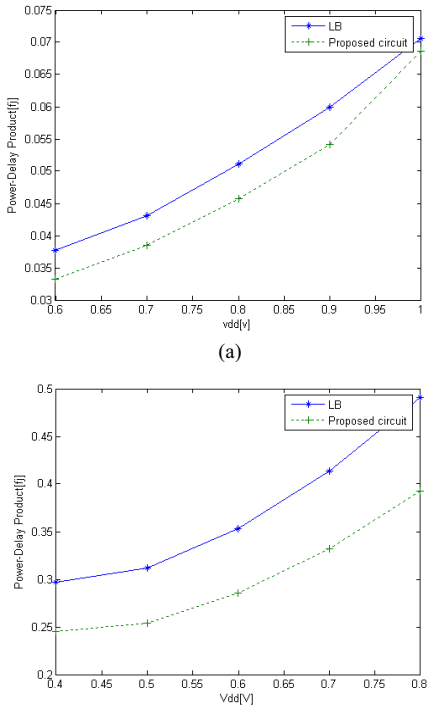
[13] P. Patra, U. Narayanan, and T. Kim, "Phase Assignment for Synthesis of Low Power Domino Circuits," *IEE Electronics Letters*, vol. 37, no. 13, pp.814 – 816, 21 June 2001.

[14] S. Heo and K. Asanovic, "Leakage-Biased Domino Circuits for Dynamic Fine-Grain Leakage Reduction," in *Proc. of the Symposium on VLSI Circuits*, June 2002.

[15] A. Abdollahi, F. Fallah, and M. Pedram, "Runtime Mechanisms for Leakage Current Reduction in CMOS VLSI Circuits," in *Proc. of the 2002 International Symposium on Low Power Electronics and Design (ISLPED '02)*, pp.213 – 218, 2002.

[16] http://www-devices.eecs.berkeley.edu/~ptm/.

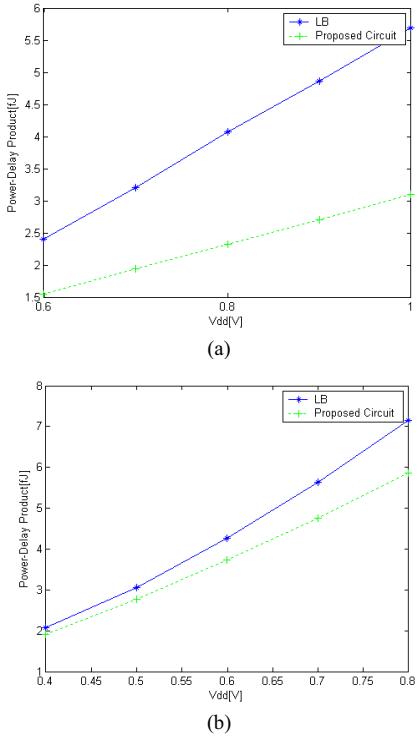
Appendix



(a)

(b)

Fig. 4. Power delay product in 3-input OR gate versus V_{dd} in (a) 65nm (b) 45nm process.



(a)

(b)

Fig. 5. Power delay Product in 3-input AND gate versus Vdd in (a) 65nm (b) 45nm process.

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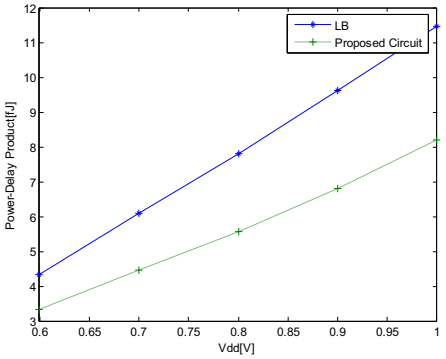
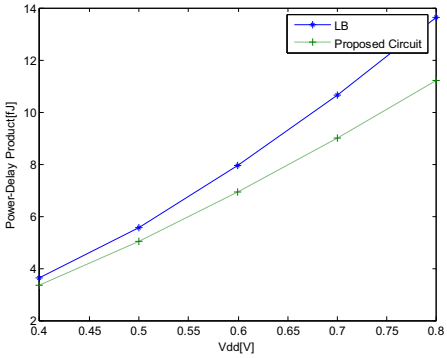


(a)



(b)

Fig. 6. Power delay product in an ADDER circuit versus V_{dd} in (a) 65nm (b) 45nm process.

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