A Low Power Base-Band Circuit for Low-IF Wireless PAN Receivers

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***Abstract*- A fully integrated CMOS base-band part of a low-IF WPAN receiver is presented, which consists of an active complex filter, an automatic gain control unit, and a 10-Bit Pipe-Line ADC. The highlights of the receiver include a low-power active complex filter with a nonconventional Gm-C structure and a high-resolution, low power pipe line ADC using averaging and double sampling techniques. The chip was designed on a small die using 0.18-um standard CMOS process. The filter provides more than 55 db image rejection ratio and IM3 of -50 dB for 1.9 & 2.1 MHz signals with 0.2Vpp. The converter has a peak SFDR of 61 dB, maximum DNL of 0.5 LSB, and INL of 0.9 LSB. The all parts of the scheme consume an active current about 4mA from a 1.8-V power supply.**

Index Terms- **ADC, Complex filter, CMOS , WPAN, Low-IF**

I. INTRODUCTION

A wireless communication with higher density of nodes and simple protocol is emerging for low-data-rate distributed sensor network applications such as those in home automation and industrial control. A low-power Bluetooth radio [1] is standardized as IEEE802.15.1 but it is relatively expensive and consumes too much power for this purpose. In 2000, IEEE started to standardize IEEE 802.15.4 exclusively for these kinds of low-rate wireless personal area network (LR-WPAN) applications.

Due to the application environment of the WPAN system, the specification has made emphasis on intermodulation performance. Low cost, low power consumption and small form factor are essential requirements for a WPAN transceiver. In this paper, we present a fully integrated base-band part of a low-IF WPAN receiver. The receiver was designed using a low-cost 0.18-um standard CMOS process while uses a low-IF architecture with 2-MHz IF. An on-chip automatically tuned OTA-C complex filter achieves more than 55 db of image rejection ratio and suppresses strong adjacent channel interference.

In Section II, the receiver architecture and high-level design issues are addressed. Section III explains the circuit design of each building block in detail. The results are reported in Section IV. Conclusions are provided in Section V.

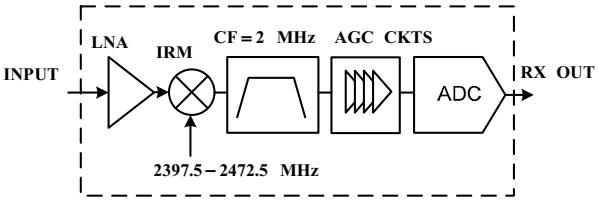

Fig.1. Topology of a low-IF WPAN receiver.

II. RECEIVER ARCHITECTURE

Three different architectures are commonly used in current receiver designs: high-IF, low-IF, and direct-conversion architectures. The selection of different IFs results in different circuit implementation tradeoffs. A high-IF receiver, which uses an IF much larger than the signal channel bandwidth, requires off-chip components with high quality factors (Q); hence, the system integration level is reduced, and extra power on the I/O driving circuits is demanded. In addition, the high-IF choice also increases the complexity of the IF band circuits and causes more power dissipation in the IF stage. Thus, high-IF architecture is not adopted in the proposed design. In a baseband WPAN signal, the most of the signal power is contained within the dc to bandwidth. If direct-conversion architecture is used, the flicker noise and dc offset will significantly degrade the signal-to-noise ratio (SNR). Hence, a low-IF architecture is more appropriate in this proposed design, especially when considering the relaxed image rejection requirement in WPAN. The modulation selected for ZigBee is Offset Quadrature Phase Shift Keying (O-QPSK) with half-sine pulse shaping [2]. The benefit of this constant envelope modulation is the flexibility to use simple, low-cost, and less linear power amplifiers in the transmit chain. Binary data is coded into 4-bit symbols (16-ary) where each symbol contains a nearly orthogonal 32-bit pseudo-noise (PN) sequence transmitted at a 2.0 Mchips/s rate. Fig. 1 shows the block diagram of the low-IF receiver. The RF signal is amplified and downconverted to an IF by the RF front end (LNA-Mixer); then the channel selection and image signal suppression are

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performed by an active complex filter, and after filtering signals are passed through to the automatic gain control to relax the dynamic range. The last analog component of the receiver is ADC which converts the analog signals to digital's as inputs of the DSP section.

III. CIRCUIT IMPLEMENTATIONS

A. Filter Architecture

System level simulations show that a complex filter based on a sixth-order Butterworth LPF may be sufficient to achieve the required selectivity. A low-pass filter (LPF) prototype can be converted to a band-pass complex filter by applying a linear frequency transformation $(s \rightarrow s - j\omega_{IF})$ [3]. This is equivalent to replace each pair of grounded capacitors in I and Q branches according to the equation (1) as depicted in Fig.2.

$$sC \rightarrow sC - j\omega_{IF}C \quad (1)$$

This transformation is equal to shift the LPF frequency response to $+\omega_{IF}$. Therefore, the image signal at $-\omega_{IF}$ will be outside of the filter pass-band and will be rejected. Using the mentioned method, it is possible to convert a typical real biquadratic Gm-C filter to a complex biquadratic Gm-C filter. Fig. 3 shows the fully differential structure of the proposed filter as the real part of the complex filter.
The transfer function of the complex biquadratic Gm-C filter is described by the equations (2).

$$H(s) = \frac{{\omega_p}^2}{(s - j\omega_{IF})^2 + (s - j\omega_{IF})\omega_p / Q + {\omega_p}^2} \quad (2)$$

Where,

$$\omega_p^2 = \frac{g_{m1}g_{m5}}{C_m C_o} \ , \ Q = \sqrt{\frac{C_o}{C_m}.\frac{g_{m1}}{g_{m5}}}$$

The circuits introduced in Fig. 4 are the required cross coupled connectors to realize the linear frequency transformation which are calculated by the equations below:

$$g_{mc} = C_m.\omega_{IF} \quad (3)$$

$$g_{md} = C_o.\omega_{IF} \quad (4)$$

An active-RC structure is used as an automatic gain control with the single stage folded cascade opamp to relax the dynamic range of the signal after filtering.

B. Proposed Pipeline Structure

Fig. 5 shows the common structure of the 1.5-Bit pipeline ADC stage that all capacitors during its sampling cycle are set to the input voltage; hence, the stage amplifier is in the rest mode but consumes power. Double sampling technique, by adding another set of capacitors and switches, moderates this problem and allows the stage to utilize amplifier during both cycles. A double sampling method intended in Fig. 6(a) consists two set of capacitors which are replaced with each other during averaging approach.
For analyzing the desired SHA, the timing diagram depicted in Fig. 6(b) is used. C_{f1} & C_{s1} sample V_i while φ_8, φ_2 are high. At the same time, C_{s2} is connected to the reference voltage, and C_{f2} is connected to the opamp in the feedback configuration. The stage gain in this cycle is equal to G1, and like this approach the gain stages for other cycles are calculated as shown in equation (5).

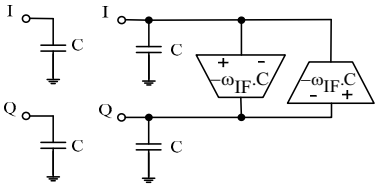


Fig. 2. Linear frequency translation to convert LPF to complex BPF.

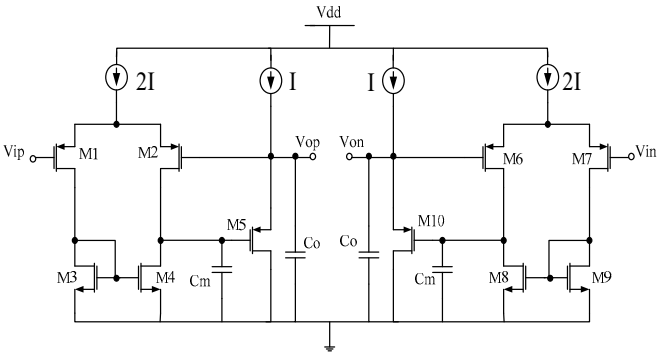


Fig. 3. Single ended Gm-C biquadratic real filter.

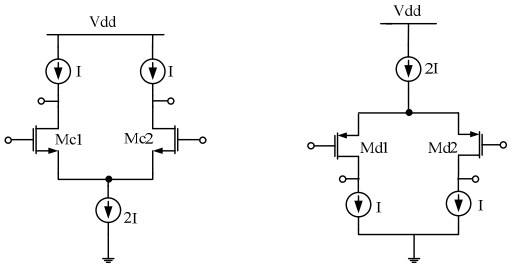


Fig. 4. Required connectors for linear frequency transformation.

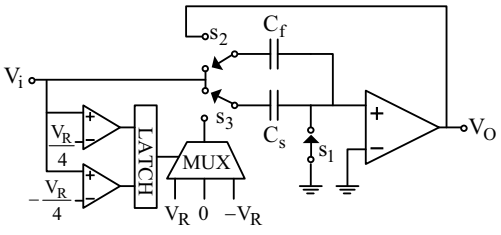


Fig. 5. Common 1.5-Bit pipeline ADC stage.

$$G_1 = 1 + \frac{C_{s2}}{C_{f2}}, G2 = 1 + \frac{C_{s1}}{C_{f1}}, G_3 = 1 + \frac{C_{f2}}{C_{s2}}, G_4 = 1 + \frac{C_{f1}}{C_{s1}} \quad (5)$$

One of the restrictions limiting the unit capacitance is noise constraint. "Multiply by two" block is shown in Fig. 5. As seen in this figure,

$$Cl = C_{ns} + C_{out} + C_{other} + \frac{C_f (C_s + C_{opamp})}{C_s + C_f + C_{opamp}} \quad (6)$$

Where C_{ns} is the next stage capacitive load, C_{out} is opamp output capacitance. Since the total input-referred noise due to opamp noise is calculated by dividing V_{no}^2 by residue-amplifier gain squared, so in a fully-differential circuit [4]:

$$V_{ni,total}^2 = 2.kT.\frac{2}{3}.\frac{1}{f}.\frac{1}{C_l}.F.(\frac{C_f}{C_s + C_f})^2 \quad (7)$$

Where k is Boltzman constant, T is absolute temperature, F is noise factor usually equal to *"6"* for two-stage or folded-cascode configurations and *"3"* for telescopic-cascode opamps and f is the feedback factor. Considering that in an m-Bit residue stage with gain 2^m (or an m+l-Bit stage with one redundant bit), the total input-referred noise is calculated from [4]:

$$\frac{C_s}{C_f} = 2^m - 1 \quad (8)$$

$$V_{ni,opamp}^2 = 2.kT.\frac{2}{3}.\frac{1}{f}.\frac{1}{C_l}.F.(\frac{C_f}{C_f + C_S})^2 + 2kT.\frac{(C_s + C_f + C_{opamp})}{(C_s + C_f)^2} \quad (9)$$

The capacitance mismatch is the other important factor to determine the unit capacitor. This factor is appeared as a ratio of the capacitors in the stage gain. The dominant unit capacitor of the 10-Bit pipeline ADC is fixed by the capacitance mismatch, but using averaging technique can alleviate this problem by exchanging the priority of these two factors (input-referred noise and capacitance mismatch). Equations (10), (11) show the variance of the stage gain in the common stage and the stage using averaging technique respectively. As a result of the mentioned equations, Fig. 7 has been plotted to describe the variance of the stage gain with and without the averaging method versus the variance of the capacitance mismatch.

$$\sigma_{Gi} = \sqrt{2}.\sigma_C \quad (10)$$

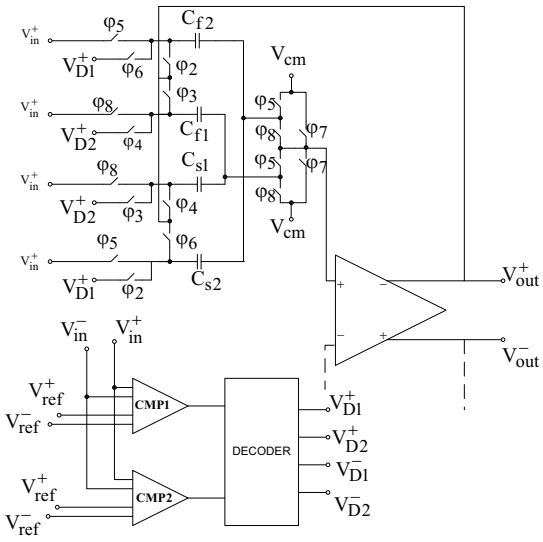
$$\sigma_{Gj} = \sigma_C^2 \quad (11)$$

Where σ_C is the variance of the capacitance mismatch.

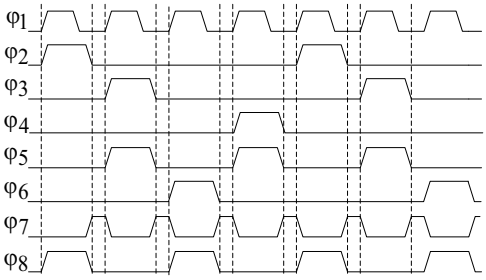
The operational amplifier used in the converter is one stage folded cascade structure, and also the dynamic type of the comparator is utilized to consume less power in whole system.

IV. SIMULATION RESULTS

All the circuits have been designed and tested with precise simulations. Table I, II summarize the simulated performances of the complex filter and A/D respectively. A sinusoidal source with frequency of 3 MHz and full scale amplitude was used as an input to the ADC system to test SNR. Fig. 8 shows FFT plot of output stream.



(a)



(b)

Fig. 6. (a) Proposed 1.5-Bit double sampling pipeline ADC stage (b) Clock timing diagram for proposed structure.

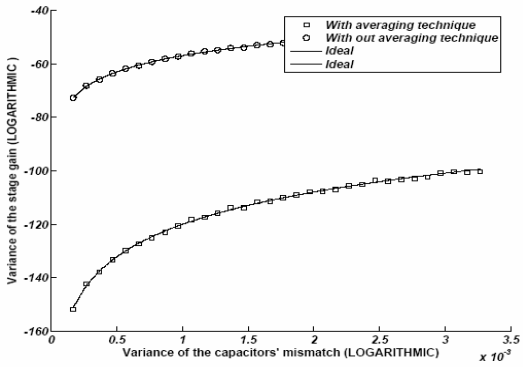


Fig. 7. Variance of the stage gain with and without the averaging method versus the variance of the capacitance mismatch.

The peak SFDR is 61 dB which shows the ADC can achieve 10-Bit performance at sampling rate of 40 MS/s, and Fig. 9 shows the frequency response of the filter for positive and negative frequencies around ω_{IF}. The whole design including complex filter with the auto tuning circuit, AGC, and pipe line ADC consumes 7.2mW from a 1.8V supply.

V. CONCLUSION

A low power base band circuit for low-IF Wireless PAN receiver has been presented in this paper. The power consumption of all components is less than 7.5mW, while the image rejection ratio at the filter is more than 55db. Also, the ADC used to convert the base band signal to digital has the SFDR of 61dB and the INL & DNL of 0.9LSB, 0.5LSB respectively. All these have been achieved through the new OTA structure in the active complex filter and using averaging and double sampling techniques in the A/D converter reducing the active area and power consumption.

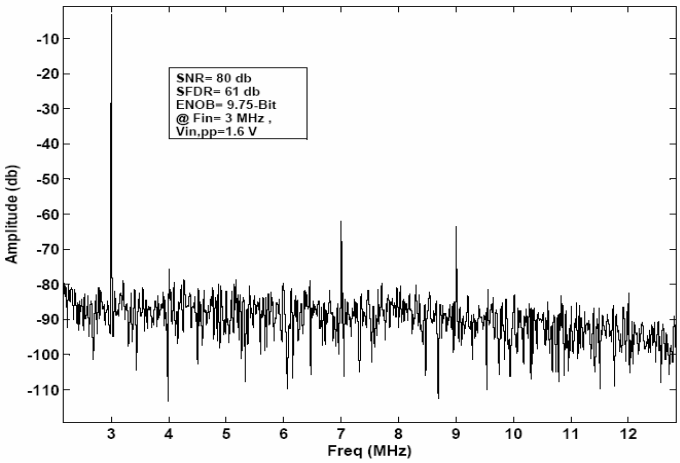


Fig. 8. FFT plot of ADC output.

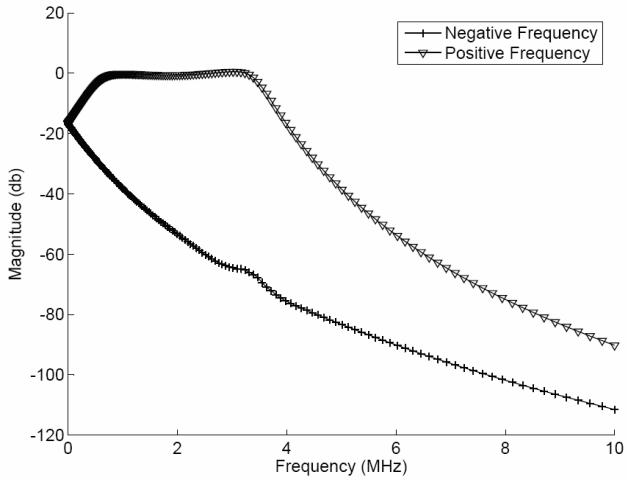


Fig. 9. Frequency response of the filter for positive and negative frequencies around ω_{IF}.

TABLE I
SIMULATION RESULTS OF THE PROPOSED FILTER

Parameter	Value
Supply voltage	1.8V
Band-with	3MHz
Central frequency	2MHz
Power consumption	720μW
Image rejection	55dB
Pass-band gain	0.5dB
Output noise	$130uV_{rms}$
Attenuation@ $f_c - 1.5MHz$	27dB
HD3@ $F_{in} = 2MHz, V_{p-p} = 0.2V$	45dB

TABLE II. SUMMARY OF ADC SPECIFICATIONS

Resolution	10 - Bit
Sampling rate	40MS/s
INL,DNL	0.9LSB,0.5LSB
SFDR	61dB
ENOB	9.75 – Bit
Power consumption	5mW

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