Design of a Low-Power High-Rate Ultra-Wideband Modulator for 5.8–10.6 GHz

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***Abstract*— A pulse modulator for ultra-wideband (UWB) transmitters is designed and simulated using 0.13-μm CMOS technology. 8-GHz carrier frequency is modulated into pulses with Gaussian envelop and 1-ns time-width to push the spectrum to 5.8–10.6-GHz band, and to satisfy FCC mask. By using 2-ns pulse-width, it is also possible to utilize the modulator at two sub-bands of 6–8 GHz and 8–10 GHz. The transmitter is low power since it employs a digital structure, and also supports high data rates due to using I/Q modulation. The architecture of modulator consists of Johnson counter, multiplier, current adder, and RF mixer. The key element in the design is ETSPC flip flops that fulfill high-speed and low-power requirements in precision timing. The power-speed trade-off is optimized by decreasing the size of the FFs, and using direct conversion structure for RF mixer. The power consumption of the modulator from 1.2-V power supply is as low as 4.5 mW for the rate of 2 Gchip/s at 8-GHz center frequency.**

I. Introduction

Ultra wideband (UWB) systems are categorized into pulse-based and carrier-based groups. Although pulse-based systems, due to carrier free and hence low complexity, are widely used, they are not as flexible as carrier-based systems, which shift the spectrum into higher frequency bands [1]–[3]. In [1] a 6.4-GHz sine wave is modulated in a Gaussian monocycle pulse to push the spectrum into higher frequency band and to meet Federal Communications Commission (FCC) mask efficiently. Although this is designed without using precise short-time delay elements, the transmitter is power hungry and has coexistence problem with 5-GHz WLAN systems. In [2], a UWB pulse modulator with triangular pulse shaping is implemented to attenuate the side-lobes. This structure is highly flexible in tuning the center frequency and band-width. Maximum pulse repetition rate is as low as 40 MHz with pulse position modulation (PPM). In [3], a 4-bit Johnson counter is used for producing eight different levels that modulates an 8-GHz clock in a cycle to cycle fashion. This system use I/Q modulation for chip rate up to 1 Gchip/s. However, the power consumption is high due to large number of components and circuit complexity.

Direct sequence approach can employ at least 1.5-GHz band-width in the 3.1–5.1-GHz range, and 3.7-GHz band-width in the 5.8–10.6-GHz range with wavelets tailored to occupy desired spectrum in an efficient manner [4]. This paper presents a 5.8–10.6-GHz CMOS UWB modulator that allows ultra high data transmission rate (e.g., 2 Gchip/s) at low power dissipation. The modulator is based on direct sequence spread spectrum (DSSS) technique [5]. We improve the design in [3] by decreasing the components and optimizing the circuits to minimize the total power dissipation. Also, by modifying the number of FFs, we design the modulator for two sub-bands of 6–8 GHz and 8–10 GHz using 2-ns pulse-width at the cost of extra power and circuit complexity. We use a Gaussian pulse shape due to superior spectral characteristic and simpler implementation in digital modulator.

The reminder of the paper is organized as follows. Section II describes the main architecture of digital modulator. Section III gives the schematic of the main circuit blocks. Section IV presents the simulation results. Finally, Section V concludes the paper.

II. Transmitter Modulator Architecture

The digital Gaussian pulse with 1-ns time-width modulates the 8-GHz clock to cover frequency band from 5.8–10.6 GHz. In order to align the phase of the Gaussian pulse and 8-GHz clock, the Gaussian pulse is generated by 8-GHz clock in the Johnson counter. The data TX_I and TX_Q, which are out of alignment by 0.5 ns, perform $\pi/2$ shift in binary phase shift keying (BPSK) modulation, each with a chip rate of 1 Gchip/s. The modulator performs pulse shaping on each bit to decrease the power spectral density (PSD) to satisfy FCC mask, and to increase the total transmit power by flattening the spectrum of transmit signal.

The modulator block diagram, as shown in Fig. 1, contains an 8-GHz Johnson counter, four digital multiplier, one current adder for each I and Q paths, and a double-balanced mixer for up-conversion. The output of mixers I_OUT and Q_OUT are added up and transmitted to the antenna. Johnson counter consists of four DFFs with 8-GHz common clock that produce four 1-GHz outputs $Q1$–$Q4$, each shifted by 125 ps. The constant phase differences between outputs $Q1$–$Q4$ are used to construct eight different levels in a cycle to cycle fashion that can emerge stairs of a Gaussian pulse envelop. DFFs in this circuit must have small rise (fall) time and equal delay between outputs in order to obtain a precise Gaussian pulse. The Johnson counter generates the signals and their complementary values. To account for the sign of the register

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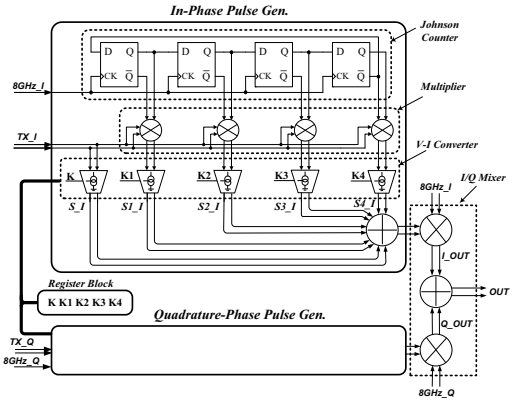

Fig. 1. Block diagram of improved pulse modulator.

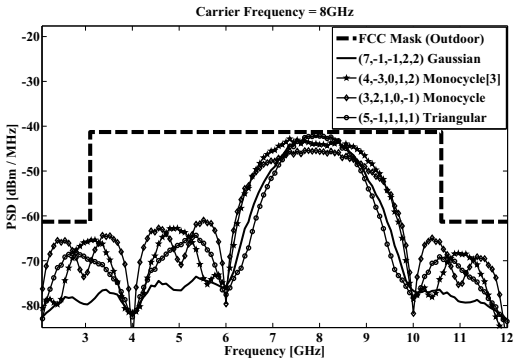

Fig. 2. Comparison of power spectral characteristic for four pulses.

values, we employ the signal (e.g., Q) for positive values and the signal complement for negative values as input in digital multiplier. This technique decreases the number of components compared to that in [3]. These outputs are multiplied by ± 1 (in digital multipliers) depending on the polarity of the TX_I and TX_Q to emerge a BPSK modulation on Gaussian pulse. TX_I and TX_Q add directly DC offset to the pulse shape. The current inputs of the adder related to register values are summed in each 125 ps to produce stairs of Gaussian envelop. Suppose the register values are {+7, -3, +1, +2, +4} [3], so we choose TX signal along with $\overline{Q}1, Q2, Q3$, and $Q4$ that are added in current mode with weight values {7, 3, 1, 2, 4}, respectively. This emerges the stairs that generates the Gaussian monocycle envelop corresponding to level values {-3, -1, 3, 11, 17, 15, 11, 3}.

A. Pulse Shapes in Digital Modulator

Register values have been demonstrated in Fig. 2 for four pulses with 1-ns time-width. The spectral characteristic of Gaussian pulse satisfies FCC mask efficiently. The implementation of modulator with similar register values results in higher linearity. Therefore, we use Gaussian pulse with register values {+7, -1, +1, +2, +2} due to lower circuit complexity, minimum side-lobes, and better spectrum.

III. Main Circuit Block Design

This section explains the techniques to meet power and speed requirements in designing the circuits for main blocks of the modulator.

A. Johnson Counter Structure

The 8-GHz Johnson counter, shown in Fig. 3, consists of four DFFs, which need low power design to reduce the total system power dissipation. High speed DFF can be designed using source-coupled logic, however, the power dissipation can be high [6]. In this paper, we design DFF using extended true single phase clock (ETSPC) logic due to extremely low power dissipation and simplicity. The potential advantage of TSPC logic is appreciable when the circuit size and the parasitic interconnect capacitances are taken into account [7]. The size

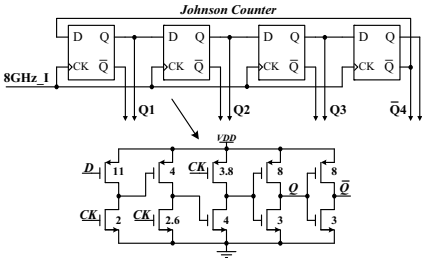

Fig. 3. 8-GHz Johnson counter.

of the FFs can be very close to minimum feature size. ETSPC has no stacked MOS structures slowing the switching speed, and the transistors are free from body effect and glitch [7]. Therefore, a very good speed-power trade-off can be achieved. If outputs of Johnson counter in I-path are $\overline{Q}1, Q2, Q3$, and $Q4$, we use their complementary in Q-path to obtain 0.5-ns shift between TX_I and TX_Q. Note that, we will need only one design for two Johnson counters.

B. Digital Multiplier

The structure for digital multiplier is the Gilbert cell shown in Fig. 4. Matching at input and output is potentially an important advantage of this design due to lower input parasitic capacitors, and minor effect on the speed of FFs. This structure is differential current mode logic (CML) [8], and exhibits high speed and low noise. Tail current source is removed in the multiplier to improve the output swing and linearity.

C. Current Adder and RF Mixer

A current adder is employed to sum outputs of digital multiplier, and to emerge stairs corresponding to register values (see Fig. 5). The current adder differential pairs are parallel to each other to satisfy register values by current weights. The adder converts input digital voltages to current outputs for RF mixer. Thus, there is no need for a voltage to current converter to accommodate a large input voltage signal [9]. Also, it adjusts the necessary gains for each current, and

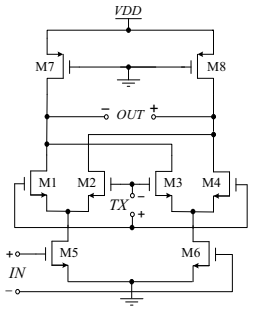

Fig. 4. Digital multiplier based on Gilbert cell.

sends emerged current to mixer without using any amplifier. Therefore, the circuit has only a few components, and exhibits a better linearity compared to that in [3].

Mixers in UWB systems can be implemented with either direct conversion or heterodyne structures. The direct conversion approach has several advantages, including high integration, low-power and low-cost despite its inherent drawbacks (I/Q mismatch, DC offset and $1/f$ noise) [9]. For low-power implementation, we employ the direct conversion I/Q mixer architecture. In UWB systems, the Gilbert cell is widely used to design active mixers. Further, the double balance topology is preferred due to rejection of local leakage signal, low even-order distortion, high conversion gain, and a very high integration size. Fig. 5 shows the full I/Q double balance mixer that merged with the current adder. I (Q) base-band voltage signals are first converted into a current signal and then summed by the current adder. The resulting signal is modulated and up converted into RF frequency by the mixer. To provide a flat gain from 5.8–10.6 GHz, two small on-chip inductors (e.g., 4 nH) on the source of transistors $M9, M10$ are used to tune out the parasitic capacitances of switching transistors $M1$–$M8$.

The precise construction of Gaussian pulse is affected by system linearity. A trade-off exists between linearity and power dissipation at low supply voltage. To increase the linearity in mixer, the sources of adder differential pairs are connected to ground [9]. By increasing the transconductance current, we achieve higher gain and linearity at the cost of high power dissipation.

IV. Simulation Results

A UWB pulse modulator is designed and simulated using 0.13-μm CMOS technology with 1.2-V power supply. Fig. 6 shows timing chart of the pulse modulator. The pulses are similar to fifteen order derivative of Gaussian pulse, since it is approximated with eight levels. Fig. 7 illustrates the simulated spectrum that meets FCC rules, without any additional filtering. Also, the spectrum spreads flat over a wide range centering at 8 GHz. As shown in Fig. 6, emerging BPSK modulation introduces spikes on I_OUT and Q_OUT. This will also appear in composite output signal (OUT) due to abrupt change of mixer current, which can disturb the output spectrum by increasing the side-lobes. The spikes can

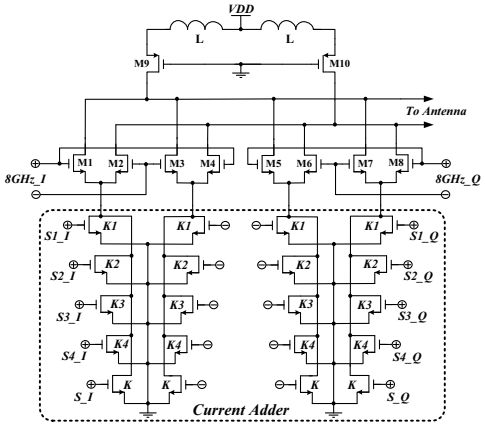

Fig. 5. I/Q double balance mixer and current adder.

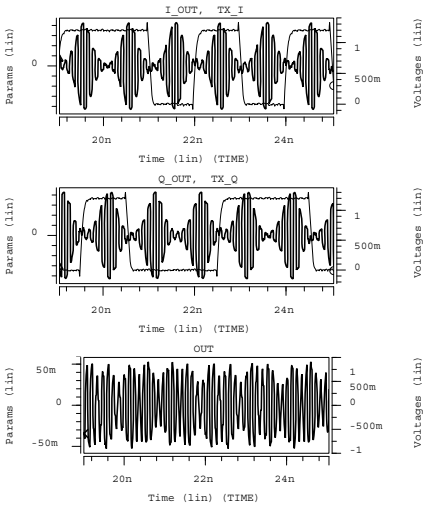

Fig. 6. Timing chart of the Gaussian pulse modulator contains I_OUT, Q_OUT, and OUT respectivly.

be reduced by equalizing the propagation delay of input signals of the multiplier.

By using 7 and 9 DFFs, it is possible to modulate a 2-ns Gaussian pulse into 7 and 9-GHz clock frequency, and to push the spectrum into 6–8-GHz and 8–10-GHz frequency sub-bands, respectively. The PSD of both modulators is shown in Fig. 8.

A. Effect of Parameter Variation on Spectrum

Since timing of DFFs has a major impact on signal spectrum, it is important to test the variation of power spectrum due to parameters variation. The dependence on V_T is compensated by the use of differential structures [2]. As shown in Fig. 9 by Monte Carlo simulation, the dependence of spectrum to $\pm 10\%$ width variations of the transistors in DFFs is negligible. The circuit performance metrics are summarized in table I, and compared to the state of the art. The pulse modulator in this paper is promising a low-power and high-rate transmitter.

TABLE I
COMPARISON WITH STATE OF THE ART

Reference	[1]	[2]	[3]	This work	This work
Technology	0.18-μm	0.18-μm	0.18-μm	0.13-μm	0.13-μm
Power Supply	1.8 V	1.8 V	1.8 V	1.2 V	1.2 V
Status	Measured	Measured	Measured	Simulated	Simulated
Side-lobe Rejection	–	$>$ 20 dBc	$>$ 20 dBc	$>$ 25 dBc	$>$ 25 dBc
Modulation	BPSK	PPM	I/Q	I/Q	I/Q
PRF / Chip Rate	–	40 MHz	1 Gchip/s	2 Gchip/s	1 Gchip/s
Band width	7 GHz	0.5–2 GHz	1.9 GHz	3.8 GHz	1.9 GHz
Carrier Frequency	6.4 GHz	4–8 GHz	4 GHz	8 GHz	7 GHz, 9 GHz
Power Consumption	153 mW	2 mW	105 mW	4.5 mW	5 mW, 12 mW

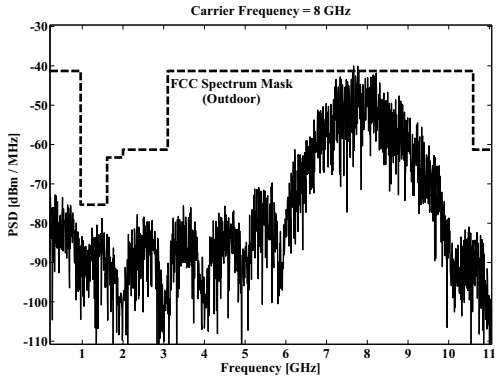

Fig. 7. The PSD of Gaussian pulse that modulates the 8-GHz clock frequency.

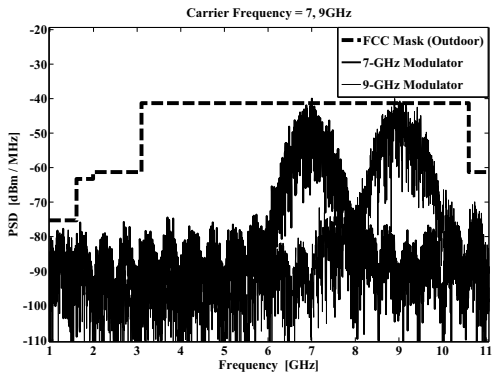

Fig. 8. The PSD of Gaussian pulse that modulates the 7 & 9-GHz clock frequency.

V. CONCLUSION

A fully integrated UWB carrier-based modulator is designed and simulated with 0.13-μm CMOS. The rate of 1-ns time-width pulse generator with I/Q modulation is as high as 2 Gchip/s, and the power dissipation is as low as 4.5 mW from a 1.2-V power supply. Moreover, the modulator has been designed and simulated for two sub-bands of 6–8 GHz and 8–10 GHz using 2-ns pulse-width. The simulation results indicate significant performance improvement by employing Gaussian envelop under low power and transmitter simplicity requirements. Also, Monte Carlo simulation indicates that the performance change of the modulator due to process variations is negligible. This work proves the potential of UWB for low power, ultra high data transmission rate communications.

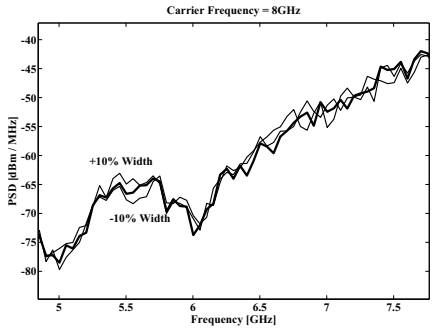

Fig. 9. Spectrum of Gaussian pulse train for $\pm 10\%$ variation of transistors width in DFFs.

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